Modeling of PMOS NBTI Effect Considering Temperature Variation

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Abstract

Negative bias temperature instability (NBTI) has come to the forefront of critical reliability phenomena in advanced CMOS technology. In this paper, we propose a fast and accurate PMOS NBTI model, in which the temperature variation and the ratio of active to standby time are considered in both stress and relaxation phases. A PMOS V_{th} degradation model and a digital circuits' temporal performance degradation estimation method are developed based on our PMOS NBTI model. The simulation results show that: 1) our dynamic NBTI model without temperature variation is as accurate as previous models, the error is less than 2.3%*; 2) the analysis error of PMOS V_{th} degradation may reach up to* 52.6% *without considering temperature variation; 3) for ISCAS85 benchmark circuits, the error of worst case performance degradation analysis is about on average* 52.0%*; 4) the ratio of active to standby time has a considerable impact during the performance degradation analysis.*

1 Introduction

As semiconductor manufacturing migrates to more advanced technology nodes, negative bias temperature instability (NBTI) is becoming one of the major reliability concerns. NBTI significantly shifts the threshold voltage V_{th} on the order of $20-50$mV for devices operating at 1.2V or below [1]. Previous research showed that V_{th} shifts due to NBTI is expressed as a power-law time dependence [2, 3], and this aging-induced parameter variation has a negative impact on circuit performance. After the aging time of 10^6s arising from NBTI, the circuit performance degradation can reach up to 15% [4].

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The NBTI occurs when the PMOS transistor is negative biased, in particular at elevated temperature. This phenomenon can be classified as static NBTI and dynamic NBTI. Static NBTI (i.e. under constant voltage (DC) stress condition) leads to a severe V_{th} shifts, while the mechanism was described in [5]. However, because of associated recovery phenomena the dynamic NBTI (i.e., under AC stress), a less severe parameters' shifts over long time compared with that under DC stress condition were observed and described in [6–10].

Recently, NBTI models are developed to analysis the reliability and delay degradation problems in large-scale digital circuit [11–15]. Based on these circuit degradation models, NBTI-aware design techniques were investigated in [14, 15]. An analytical model for evaluating dynamic NBTI effect was proposed in [16], and the effect of various process and design parameters were described in [17].

In previous analytical NBTI models [16, 17], the circuit temperature was considered to be constant during the circuit operation. However, when the circuit switches between active and standby mode, the circuit temperature varies periodically between high temperature and low temperature. Therefore, we propose an analytical model for dynamic NBTI effect considering the temperature variation on account of the switch of circuit operation modes: active and standby mode.

Our contribution in this paper distinguishes itself in the following aspects:

- We propose an analytical model to estimate PMOS NBTI effect under AC stress condition. Our model is faster than the model in [16], while remains the same accuracy. Furthermore, two factors, a) the temperature difference between circuit active and standby mode; b) the time ratio of circuit active and standby mode, are first considered in both stress and relaxation phases during our NBTI analysis.
- Based on our novel NBTI model, we propose a PMOS V_{th} degradation model and study the impact of NBTI on the temporal performance degradation in combinational

circuits considering both the temperature variation and ratio of active to standby time.

The rest of the paper is organized as follows. In Section 2, we first review previous NBTI models and present our improved analytical NBTI model. Then, in Section 3, we give out the V_{th} degradation model, and the circuit delay estimation method. The simulation results of a single PMOS transistor and the ISCAS85 benchmark circuits are shown and analyzed in Section 4. Finally, Section 5 concludes the paper.

2 NBTI Model

A shift in the threshold voltage ΔV_{th} of the PMOS transistor is proportional to the interface trap generation due to NBTI, which can be expressed [15] as

$$\Delta V_{th} = (1+m)\frac{qN_{it}(t)}{C_{ox}} \tag{1}$$

where m represents equivalent V_{th} shifts due to mobility degradation, q is the electronic charge, C_{ox} is the gate oxide capacitance, and $N_{it}(t)$ is the interface trap generation, which is the most important factor in evaluating performance degradation due to NBTI.

2.1 Previous NBTI Models

The interface trap generation is often described by a reaction-diffusion (R-D) model [3],

$$\frac{dN_{it}}{dt} = k_f(N_0 - N_{it}) - k_r N_{it} C_H(0,t) \tag{2}$$

$$\frac{dN_{it}}{dt} = -D_H \frac{\partial C_H}{\partial x}\bigg|_{x=0} \tag{3}$$

$$\frac{\partial C_H}{\partial t} = D_H \frac{\partial^2 C_H}{\partial x^2} \tag{4}$$

where the mobile diffusing species are assumed to be neutral H atoms, and N_0 is the concentration of initial interface defects. The parameters k_f and k_r are constant dissociation rate and self-annealing rate, respectively. When the device is in recovery phase, k_f becomes zero, and k_r is unchanged. The parameter C_H is the concentration of H atoms, and D_H is the corresponding diffusion coefficient.

In this model, the interface trap generation (ΔN_{it}) under DC stress condition is expressed as [3]

$$N_{it}(t) = 1.16\sqrt{\frac{k_f N_0}{k_r}}(D_H t)^{1/4} = At^{1/4}. \tag{5}$$

Kumar et al. proposed an analytical NBTI model [16] to handle multi-cycle AC stress condition; and assuming the PMOS transistor is under AC stress with duty cycle of c and the period of τ, the interface trap generation after $n+1$ cycles of AC stress can be evaluated by a recursion formula below,

$$N_{it}[(n+1)\tau] = \frac{\beta N_{it}(n\tau)}{1+\beta} + \frac{N_{it}^0}{1+\beta}\left[c + \left(\frac{N_{it}(n\tau)}{N_{it}^0}\right)^4\right]^{1/4} \tag{6}$$

and the initial condition is

$$N_{it}(\tau) = \frac{c^{1/4}}{1+\beta} N_{it}^0 \tag{7}$$

where $N_{it}^0 = A\tau^{1/4}$, and $\beta = \sqrt{\frac{1-c}{2}}$.

2.2 Our improved dynamic NBTI Model without temperature variation

Though the model proposed by Kumar [16] is accurate, the computing process may be slow because of the recursion process in Eq. (6). We use a different approach to derive the model under AC stress.

If the period τ is small enough (i.e., at a frequency more than several KHz magnitude), the traps created at the stress and relaxation phases in one cycle can be expressed as

$$\Delta N_{it} = k_f(N_0 - N_{it})(c\tau) - k_r N_{it} C_H(0,t)(c\tau) \tag{8}$$

$$\Delta N_{it} = -k_r N_{it} C_H(0,t)(1-c)\tau \tag{9}$$

Thus, the above two equations can be averaged, giving [10]

$$\frac{dN_{it}}{dt} = c \cdot k_f(N_0 - N_{it}) - k_r N_{it} C_H(0,t). \tag{10}$$

Contrasting with Eq. (2), the interface trap generation can be expressed as

$$N_{it}(t) = 1.16c^{0.5} \cdot \sqrt{\frac{k_f N_0}{k_r}}(D_H t)^{1/4} \tag{11}$$

where $c^{0.5}$ describes the impact of AC stress on NBTI.

In order to eliminate the error in Eq. (11), the exponent of c should be modified. We use a linear function to replace the exponent 0.5, and the function can be determined by fitting technology. Hence, the interface trap generation can be described as

$$N_{it}(t) = 1.16 \cdot c^{0.5+0.24c-0.23} \cdot \sqrt{\frac{k_f N_0}{k_r}}(D_H t)^{1/4}. \tag{12}$$

The comparison between Kumar's [16] and our model is shown in Figure 1. The multi-cycle NBTI model under AC stress condition proposed in this paper is as accurate as Kumar's model, the error is less than 2.3% ($3.70 \times 10^{12}\text{cm}^{-2}$ of our model, and $3.62 \times 10^{12}\text{cm}^{-2}$ for Kumar's model in Figure 1). Since there is no recursion process in our model, our method is faster than Kumar's.

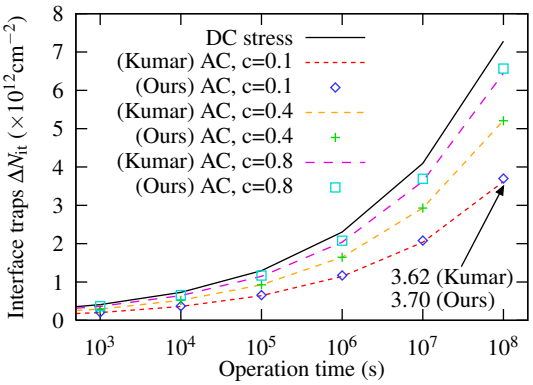

Figure 1. Comparison between Kumar's and our model

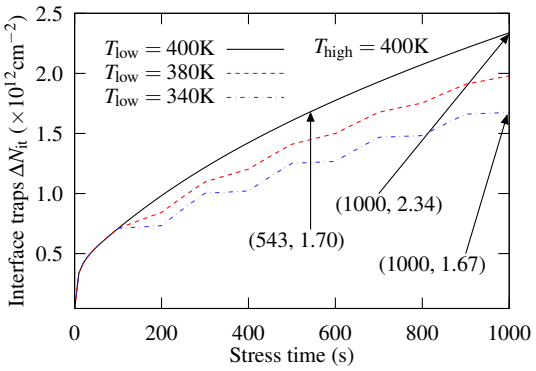

Figure 2. Impact of temperature variation in stress phase

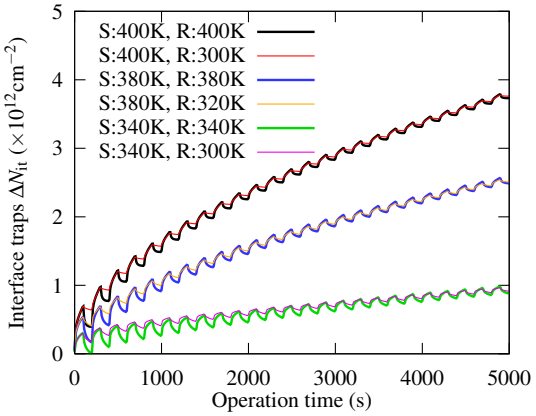

Figure 3. Impact of temperature variation in relaxation phase

2.3 NBTI analysis with temperature variation

During circuit operations, the circuit switches between active and standby modes, so that the temperature changes relevantly. Previous NBTI models [16,17] only consider the situation that the temperature is a constant (which is around 400K). Actually the circuit temperature varies when the circuit switches between active and standby mode. Therefore the NBTI model should be modified to consider the temperature variation. Assuming the device operation temperature changes between T_{high} and T_{low} frequently, the interface trap generation due to NBTI is different from the case under a constant high operation temperature condition.

- First, we consider the impact of temperature variation in stress phases. The temperature variation has a significant impact on the diffusion coefficient of H atom (D_H) in Eq. (4). In this paper, a triangle diffusion profile [3] is used. The effect of H atom diffusion under T_{low} lasting for a stress time of t_{low}, equals to the effect under T_{high} for a stress time of t_{high}, if $\sqrt{D_{high}t_{high}} = \sqrt{D_{low}t_{low}}$ (D_{high} and D_{low} denote diffusion coefficients under high and low temperature, respectively). Because the diffusion coefficient is proportional to $\exp(-\frac{E_a}{kT})$, the ratio of D_{low} to D_{high} can be expressed as

$$\mu = \frac{D_{low}}{D_{high}} = \exp\left[\frac{E_a}{kT_{high}}\left(1 - \frac{T_{high}}{T_{low}}\right)\right] \quad (13)$$

Therefore, the equivalent stress time can be expressed as

$$t_{eq} = t_{high} + \mu t_{low} \quad (14)$$

where the total stress time t can be divided into two parts: t_{high}, the stress time at high temperature, and t_{low} the stress time at low temperature. Figure 2 shows the numeric simulation result of this law. We take $T_{high} = 400$K, $T_{low} = 340$K as an example. The ratio μ is 0.0857 when E_a is set to 0.48eV. Hence, the equivalent stress time t_{eq} is 543s (Figure 2) when $t_{high} = t_{low} = 500$s. Figure 2 shows that the interface trap generation is 1.67×10^{12}cm^{-2}, and the equivalent trap generatin at high temperature is 1.70×10^{12}cm^{-2}, where the error is 1.8%. If the temperature is considered to be kept at high temperature constantly, the interface trap generation is 2.34×10^{12}cm^{-2}, and the error is 40.1%.

- Second, a totally different phenomenon in relaxation phases is observed from numeric simulation. Under AC stress condition, if temperature variation only occurs in relaxation phases, the overall interface trap generation is not affected. This phenomenon is shown in Figure 3. Though the temperature variation indeed affects the trap generation in a single cycle, the overall trap generation remains the same as that at a constant temperature.

2.4 Our PMOS NBTI model during real circuit operations

In previous section, we analyze the impact of temperature variation on the interface trap generation. In real circuits, the situation is much more complex. In this paper, we make an assumption that the circuit switches between

active and standby modes periodically, and the PMOS transistor in the circuit is under AC stress in active mode, while in standby mode, it is under constant DC stress or in relaxation. We denote the ratio of the active to standby time as R_{AS}, the temperature of active mode is denoted as T_{act} (corresponding to high temperature T_{high} in previous section), and the temperature of standby mode as T_{stdby} (corresponding to T_{low}). The interface trap generation is modeled as follows:

a) If the PMOS transistor is in relaxation phase in standby mode, the interface trap generation is not affected by the temperature variation according to Section 2.3, which can be described as

$$N_{\mathrm{it}}(t) = 1.16 \cdot \gamma^{0.5+0.24\gamma-0.23} \cdot \sqrt{\frac{k_{\mathrm{f}} N_0}{k_{\mathrm{r}}}} (D_{\mathrm{act}} t)^{1/4}$$
$$\gamma = \frac{cR_{\mathrm{AS}}}{R_{\mathrm{AS}}+1} \tag{15}$$

where D_{act} is diffusion coefficient in active mode, and here c is duty cycle of stress in active mode.

b) If the PMOS transistor is under DC stress in standby mode, the stress time in standby time should be transformed using Eq. (14). Therefore, the interface trap generation is described as

$$N_{\mathrm{it}}(t) = 1.16 \cdot \gamma^{0.5+0.24\gamma-0.23} \cdot \sqrt{\frac{k_{\mathrm{f}} N_0}{k_{\mathrm{r}}}} (D_{\mathrm{eff}} t)^{1/4}$$
$$\gamma = \frac{cR_{\mathrm{AS}} D_{\mathrm{act}} + D_{\mathrm{stdby}}}{R_{\mathrm{AS}} D_{\mathrm{act}} + D_{\mathrm{stdby}}} = \frac{cR_{\mathrm{AS}} + \mu}{R_{\mathrm{AS}} + \mu}$$
$$D_{\mathrm{eff}} = \frac{R_{\mathrm{AS}} D_{\mathrm{act}} + D_{\mathrm{stdby}}}{R_{\mathrm{AS}}+1} = \frac{R_{\mathrm{AS}} + \mu}{R_{\mathrm{AS}}+1} D_{\mathrm{act}} \tag{16}$$

where

$$\mu = \frac{D_{\mathrm{stdby}}}{D_{\mathrm{act}}} = \exp\left[\frac{E_{\mathrm{a}}}{kT_{\mathrm{act}}}\left(1 - \frac{T_{\mathrm{act}}}{T_{\mathrm{stdby}}}\right)\right]. \tag{17}$$

3 V_{th} and circuit delay degradation model

Previous section describes the analytical model of interface trap generation due to NBTI considering the temperature variation between active and standby mode in real circuits. In order to evaluate the temporal performance degradation due to NBTI, the threshold voltage degradation model and circuit delay model are described in the following subsections.

3.1 PMOS V_{th} degradation model

A predictive compact model for NBTI is developed in [17]. The dependence of NBTI on key process (such as L, V_{th}, and T_{ox}) and design parameters (such as V_{dd}) are captured in this model. From Eq. (1), the model in [17], and our NBTI model Eq. (15)-(17) proposed in previous section, the degradation of threshold voltage is given by

$$\Delta V_{\mathrm{th}} = K_V \cdot \gamma^{0.5+0.24\gamma-0.23} \cdot \lambda t^{1/4} + \delta_V$$
$$\gamma = \begin{cases} \frac{cR_{\mathrm{AS}}}{R_{\mathrm{AS}}+1}, & \text{under relax in standby} \\ \frac{cR_{\mathrm{AS}}+\mu}{R_{\mathrm{AS}}+\mu}, & \text{under stress in standby} \end{cases}$$
$$\lambda = \begin{cases} 1, & \text{under relax in standby} \\ \left(\frac{R_{\mathrm{AS}}+\mu}{R_{\mathrm{AS}}+1}\right)^{\frac{1}{4}}, & \text{under stress in standby} \end{cases} \tag{18}$$

where K_V and δ_V are the parameters extracted from [17], and μ is the ratio of D_{stdby} to D_{act} describing by Eq. (17).

3.2 Gate and circuit delay degradation analysis

In this paper, the delay of a gate v can be approximately expressed as [15]

$$d(v) = \frac{C_{\mathrm{L}} V_{\mathrm{dd}}}{I_{\mathrm{d}}} = \frac{K}{(V_{\mathrm{gs}} - V_{\mathrm{th}})^{\alpha}}$$
$$K = \frac{C_{\mathrm{L}} V_{\mathrm{dd}}}{\mu C_{\mathrm{ox}} W_{\mathrm{eff}} / L_{\mathrm{eff}}}. \tag{19}$$

The shift in the transistor threshold voltage ΔV_{th} can be derived using Eq. (18). Hence, the delay degradation $\Delta d(v)$ for gate v can be derived as

$$\Delta d(v) = \frac{K}{(V_{\mathrm{gs}} - V_{\mathrm{th}} - \Delta V_{\mathrm{th}})^{\alpha}} - \frac{K}{(V_{\mathrm{gs}} - V_{\mathrm{th}})^{\alpha}}$$
$$= \left((1 - \frac{\Delta V_{\mathrm{th}}}{V_{\mathrm{g}} - V_{\mathrm{th}}})^{-\alpha} - 1 \right) d(v). \tag{20}$$

We use Taylor series expansion on the right side of Eq. (20), neglecting the higher order terms, giving that

$$\Delta d(v) = \frac{\alpha \Delta V_{\mathrm{th}}}{V_{\mathrm{gs}} - V_{\mathrm{th0}}} \times d(v) \tag{21}$$

where V_{th0} is the original transistor threshold voltage and $d(v)$ is the original delay of gate v.

4 Simulation results

In this section, we present the simulation results in order to validate the NBTI model. Firstly, a single PMOS transistor is used to evaluate the NBTI effect considering temperature variation. Secondly, ISCAS85 circuits are used as the benchmark. In this paper, the standard cell library is constructed using the PTM 90nm bulk CMOS model [18]. $V_{\mathrm{dd}} = 1.0$V, $|V_{\mathrm{th}}| = 220$mV are set for all the transistors in the circuits.

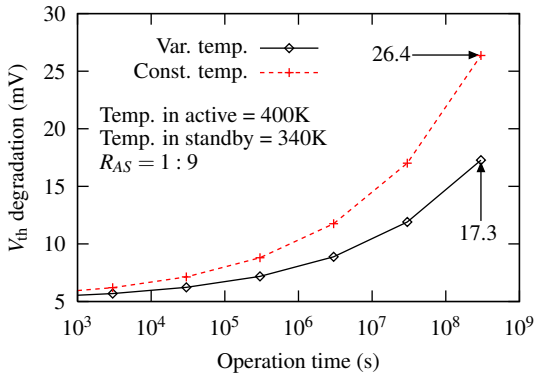

Figure 4. NBTI effect under variable temperature vs. constant temperature

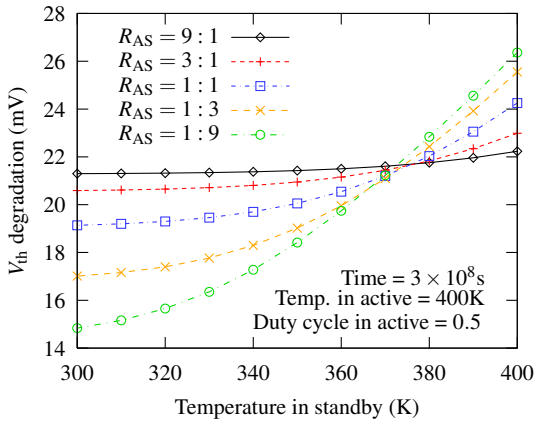

Figure 5. Impact of temperature in standby on V_{th} degradation

4.1 Single PMOS device NBTI analysis

The V_{th} degradation of the PMOS transistor in the circuit is shown in Figure 4. The ratio of active to standby time is set to 1 : 9, and duty cycle in active mode is 0.5. We can see that after 3×10^8s (about 10 yr), the V_{th} degradation is 17.3mV considering temperature variation. If the temperature is considered to be constant in the evaluation, the degradation can reach up to 26.4mV, and the error is 52.6%.

The temperature in the standby mode and the ratio of active to standby time have considerable impact on the V_{th} degradation, which is shown in Figure 5 and 6. Table 1 shows the threshold voltage degradation ΔV_{th} with different ratios of active to standby time. From these figures and table, we can conclude that 1) a lower standby temperature leads to a smaller NBTI effect on the V_{th} degradation; 2) if the ratio of active to standby time is smaller, which means a longer standby time during the circuit operation, the impact of the standby temperature variation on the V_{th} degradation is larger.

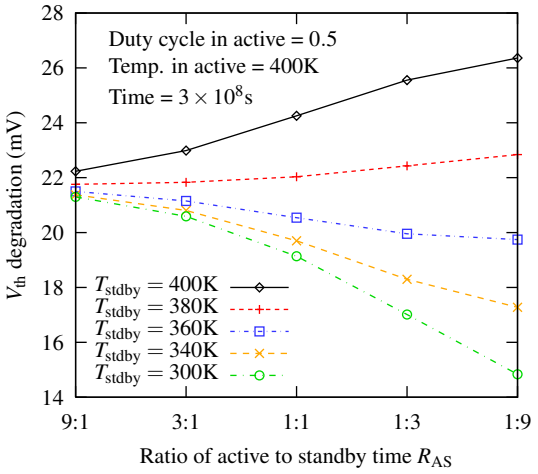

Figure 6. Impact of R_{AS} on V_{th} degradation

Table 1. ΔV_{th} under different R_{AS} (mV)

R_{AS}	9 : 1	3 : 1	1 : 1	1 : 3	1 : 9
$T_{stdby} = 400K$	22.2	23.0	24.3	25.6	26.4
$T_{stdby} = 340K$	21.4	20.8	19.7	18.3	17.3

4.2 Performance degradation analysis in digital circuits

Fig. 7 shows the performance degradation of ISCAS85 c432 benchmark with different ratios of active to standby time. The circuit delay degradation is much less than the V_{th} degradation under a same standby mode temperature. And the standby mode temperature difference leads to considerable circuit delay difference.

Table 2 shows the result of the circuit delay degradation analysis. In order to investigate the worst case circuit degradation (denoted as Max. Δdelay in Table 2), we set the internal inputs of all the PMOS transistors to logic 0 during the

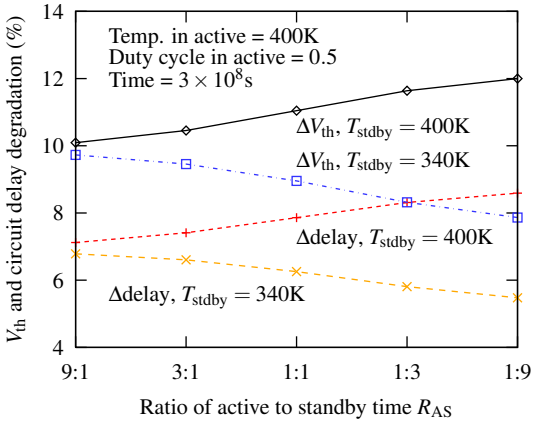

Figure 7. Impact of R_{AS} on V_{th} and circuit delay degradation

Table 2. Delay degradation of ISCAS95 benchmark circuits under NBTI

ISCAS85 Circuits	Nominal delay (ns)	(400K) Max. Δdelay (%)	Max. Δdelay	Min. Δdelay
c432	2.69	8.59	5.48	4.39
c499	1.99	8.67	5.75	4.74
c880	2.29	8.70	5.84	4.79
c1355	2.39	8.63	5.60	4.57
c1908	2.46	8.61	5.54	4.45
c2670	2.99	8.68	5.80	4.77
c3540	3.48	8.64	5.65	4.63
c5315	2.94	8.62	5.57	4.58
c6288	8.54	8.78	6.15	5.09
c7552	2.30	8.61	5.53	4.53
Average	N/A	8.65	5.69	4.65

standby mode. The inputs are set to logic 1 to investigate the best case circuit degradation (denoted as Min. Δdelay in Table 2). The ratio of active to standby time is set to 1 : 9. The Max. Δdelay is around 5.69% of the original circuit delay when $T_{\text{stdby}} = 340K$, and Min. Δdelay is around 4.65%. If the temperature variation is not considered, the Max. Δdelay is around 8.65% (corresponding to the third column in Table 2), which leads to a error of 52.0%.

5 Conclusion

In this paper, we propose an analytical model of temporal performance degradation due to PMOS NBTI effect under AC stress condition. The model is as accurate as previous models, while the speed is faster. We demonstrate that the temperature variation due to the change of circuit operation mode (active and standby mode) can have significant impact on PMOS NBTI effect: if the temperature variation is not considered, for single PMOS transistor analysis, 52.6% error can be reached, while for ISCAS85 circuits analysis, the error can be up to 52.0%. Therefore, we propose an analytical model that considers the temperature variation, such that a more accurate performance degradation estimation can be performed. We also study the impact of the ratio of active to standby time on PMOS and circuit performance degradation due to NBTI.

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