

A Series Chain-Link Modular Multilevel DC-DC Converter For High Voltage and High Power Applications

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Abstract—In high voltage and high-power applications, many modular multilevel DC-DC converter topologies have been proposed for DC voltage scaling applications. In most of those proposed a three phase transformer is required. The construction of a three-phase transformer at high power and high voltages can be challenging. For example, in multi-terminal HVDC applications, several hundred kilo volts of isolation may be required. Additionally, a high number of submodules is required in most of the high voltage modular multilevel DC-DC converters. In this paper, a new modular multilevel DC-DC converter is proposed for high voltage applications, which aims to significantly reduce the number of submodules and achieve a more compact stored energy distribution. Furthermore, a number of lower voltage rated transformers are used to replace a single high voltage component. A simulation system for a 10MW, 20kV-20kV Series Chain-Link DC-DC converter, simulated in PLECS to verify the proposed topology.

Index Terms—High voltage DC-DC power converter, DC transformer for HVDC, modular multilevel converter (MMC)

I. INTRODUCTION

Modular Multilevel Converter schemes for high voltage and high power DC-DC conversion have been intensively addressed by the researchers in recent years to firstly, fulfil the requirements of high voltage DC transmission systems where isolating systems at the same or different voltages are crucial [1], [2]. Secondly, high voltage and high power DC-DC converters have been studied in literature to integrate large scale renewable energy, wind farms and solar power stations, into HVDC systems where in some cases high voltage gain DC-DC converters are required [3]–[5].

In the last decade several high voltage multilevel converters have been proposed and the most promising topologies for the mentioned applications that can be found in the literature are the following: Alternate Arm AAC-DC-DC converter, sinusoidal operation MMC-DC-DC converter, trapezoidal operation MMC-DC-DC converter, Controlled Transition Bridge converter and high gain MMC-DC-DC converters for interfacing some renewable energies with HVDC systems [3], [5]–[8].

In HVDC systems and high voltage DC networks such as, multi-terminal HVDC systems, the voltage levels are hundreds of kilo volts and the power rating is several hundreds

of MW. For all of the aforementioned modular multilevel topologies either one three phase transformer or one single phase transformer is required. Building a cooling system at a high voltage and high power rating is challenging since the performance of the cooling system is important for prevention of the lifetime reduction of a transformer and this system also impacts the cost and the size of the transformer [9]. There are other reasons which make building a transformer at a rating of hundreds of kilo volts may not be practical, however, they will not be discussed further since it is not the main aim of this paper. In addition to the MMC based DC-DC converters there are a number of non MMC based DC-DC converter structures in literature. The cascaded multi DAB converter was proposed in [10] for HVDC applications. However, it may be practically difficult to implement as a result of the non modularity of the structure and the requirement of a high number of elementary cells to reach the required high voltages. Each of these cells comprises a low voltage single phase transformer and either a full-bridge or half-bridge converter. Accordingly, the MMC structures are more preferable for HVDC applications. Moreover, for such high voltage and high power applications and due to device voltage ratings, several hundreds to a few thousands of submodules (SM), based on system voltage rating, are required in building each of the proposed high voltage modular multilevel DC-DC converter topologies. Therefore, developing a modular multilevel DC-DC converter that requires firstly, lower voltage and power rated transformers instead of a single high voltage and high power transformer and secondly, a significant reduction in the required submodules as compared to other proposed topologies are the main reasons for proposing a series connected chain-link DC-DC converter (SCC-DC-DC).

II. PRINCIPLE OPERATION OF SCC-DC-DC CONVERTER

Fig 1 presents four phases of the proposed SCC-DC-DC converter with a fixed DC source on both sides of the converter. A 1:1 (n :turn ratio=1) single phase, medium frequency transformer is considered in the AC link for each phase. Each phase consists of two chain-links; a primary chain-link and a secondary chain-link, and each chain-link consists of a series

connection of half bridge submodules. This series connection produces $\frac{1}{N_{phase}}$ (N_{phase} is the number of the phases) of DC side voltage and an AC voltage. Considering each side of the converter, the sum of the AC chain-links voltage must be zero, therefore the chain-links AC voltage are shifted by $\frac{2\pi}{N_{phase}}$ degrees considering the phases from 1 to N_{phase} as shown in Fig. 1. However, for an even number of phases, operation can be set up where half of the phases can have same AC voltage but out of phase by 180° with the other half. In each phase, L_{kP} and L_{kS} represent the primary leakage inductance and secondary leakage inductance of the transformer in addition to the tank inductance, respectively. C_{bP} and C_{bS} are the primary and secondary DC blocking capacitors, respectively and they block the DC voltage produced by the primary and secondary chain-links, respectively. The applied voltage on the transformer will be only AC on both sides. As a result, only AC current passes through the transformer and by imposing the AC voltage of the chain-link of one side (primary or secondary) of the converter and controlling the amplitude and the phase of the AC voltage of the chain-link of the other side of the converter, power flow can be controlled. Additionally, the chain-link current comprises the DC current and the AC current which is circulating between primary and secondary chain-links in each phase. The proposed SCC-DC-DC converter is derived from [11] which has been proposed for HVDC grid interconnection. In [11] the AC link tank comprises passive components, inductors and capacitors, and a full-bridge based chain-link in order to have full control of the power factor whereas in the SCC-DC-DC the control of reactive power is not required and therefore the full-bridge chain-link can be eliminated.

Considering operation of SCC-DC-DC shown in Fig. 1, assuming a lossless converter and a unity transformer turn ratio, the primary and secondary chain-link voltages, V_{ChP_i} and V_{ChS_i} , can be expressed as shown equation 1 and equation 2 respectively where M_{index} is the modulation index, ω is the angular frequency, V_{DCP} and V_{DCS} are the primary and secondary DC link voltages, respectively and $i = 1, \dots, N_{Phase}$ indicates the phases. Moreover, \hat{V}_{ChS_i} and θ are the amplitude of secondary AC voltage and the voltage angle respectively and these are controlled to manage the transfer of the power flow. The chain-link currents can be expressed using equation 3 where primary, P, and secondary, S, are represented by x and \hat{I}_{ac_i} represents the amplitude of AC link current.

$$V_{ChP_i}(t) = \frac{V_{DCP}}{N_{Phase}} (1 + M_{index} * \sin(\omega t + \frac{\pi i - \pi}{2})) \quad (1)$$

$$V_{ChS_i}(t) = \frac{V_{DCS}}{N_{Phase}} + \hat{V}_{ChS_i} * \sin(\omega t + \frac{\pi i - \pi}{2} + \theta) \quad (2)$$

$$I_{Chx_i}(t) = I_{DCx} + \hat{I}_{ac_i} * \sin(\omega t + \frac{\pi i - \pi}{2}) \quad (3)$$

The number of submodules in one chain-link, N_{SMx_i} , and the total number of required submodules, N_{SM_T} , in the SCC-DC-DC converter can be calculated as shown in equation 4 where V_{SM} represents the nominal voltage of submodule. In

comparison to a three phase MMC-DC-DC converter proposed in literature [3], [6], [8], the SCC-DC-DC requires only 33% of the submodules which are required for MMC-DC-DC converter. The total number of submodules in the MMC-DC-DC converter can be calculated as shown in equation 5. Furthermore, the number of the phases in the SCC-DC-DC can be increased as required and by increasing the number of the phases, the number of single transformer increases whilst the total number of submodules in the SCC-DC-DC will remain the same, keeping V_{SM} fixed. Additionally, increasing the number of phases will lead to a reduction in the DC current ripple- further explanation is given in the simulation section. Accordingly, building high voltage DC-DC converters with several single transformers can overcome the challenge of building one three phase high voltage transformer and overcome the cooling challenging due to lower voltage rating and power transformer rating. For providing high voltage gain, the chain-links of one side of the converter can be connected in parallel however, this will not be considered in this paper.

$$N_{SMx_i} = \frac{2 * V_{DCx}}{N_{phase} * V_{SMx}}$$

$$N_{SM_T} = N_{phase} * (\frac{2 * V_{DCP}}{N_{phase} * V_{SMP}} + \frac{2 * V_{DCS}}{N_{phase} * V_{SMS}}) \quad (4)$$

$$= \frac{2 * V_{DCP}}{V_{SMP}} + \frac{2 * V_{DCS}}{V_{SMS}}$$

$$N_{SM_MMC_T} = 6 * (\frac{V_{DCP}}{V_{SMP}} + \frac{V_{DCS}}{V_{SMS}}) \quad (5)$$

III. ENERGY STORAGE ANALYSIS OF SCC-DC-DC

In this section some considerations are given to select the optimum resonant tank and chain-link energy storage. The chain-link energy variation, $\Delta e_{Chx}(t)$, can be derived by integrating the instantaneous chain-link power, $P_{Chx}(t)$, over the fundamental period as described in equation 6. The instantaneous stored energy in the chain-links, $E_{Chx_i}(t)$, can be described as in equation 8 considering ideal energy sharing between the submodules within the corresponding chain-link where C_{SM} is the SM capacitance. Based on the expressions (6) and 8 the peak to peak energy variation can be limited by choosing a desired C_{SM} value where δ_{pp} is the per unit peak to peak energy variation normalised with the nominal V_{SM} . Knowing the required C_{SM} and the equation of the energy variation of the chain-link, the per phase stored energy, E_{Ch_i} can be approximated as presented in equation 9.

$$\Delta e_{Chx_i}(t) = \int P_{Chx_i}(t) dt = \int V_{Chx_i}(t) I_{Chx_i}(t) dt \quad (6)$$

$$E_{Chx_i}(t) = \frac{1}{2} C_{SMx} N_{SMx} V_{SMx}(t)^2 \quad (7)$$

$$C_{SMx} \geq \frac{\Delta e_{pp_Chx}}{N_{SMx} V_{SMx}^2 \delta_{pp}} \quad (8)$$

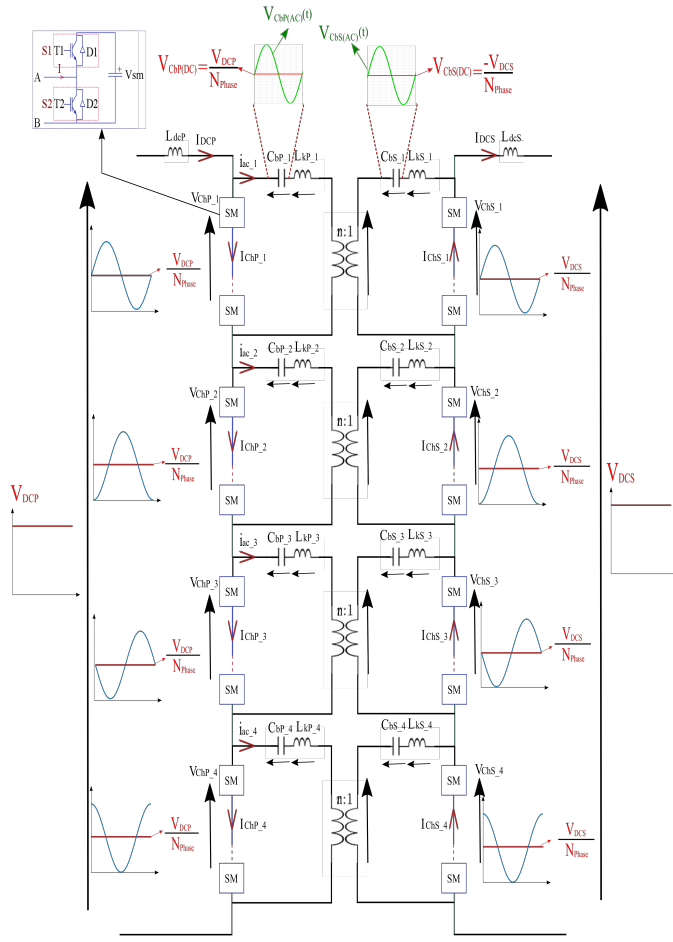


Fig. 1. SCC-DC-DC Converter

$$E_{Ch_i} \approx \frac{\Delta e_{pp_ChP} + \Delta e_{pp_ChS}}{2\delta_{pp}} \quad (9)$$

Moreover, in order to evaluate the energy requirements of the tank, the peak voltage of the DC blocking capacitor, $V_{C_{bx_i}}$, is derived as in expression 10 where $X_{C_{bx}} = \frac{1}{\omega C_{bx}}$ is the impedance of the DC blocking capacitor. The stored energy for the per phase resonant tank, E_{CL_i} can be described as in expression 11.

$$V_{C_{bx_i}} = \frac{V_{DCx}}{N_{phase}} + i_{ac_i} * X_{C_{bx}} \quad (10)$$

$$E_{CL_i} = 0.5 * C_{bP} * V_{C_{bP_i}}^2 + 0.5 * C_{bS} * V_{C_{bS_i}}^2 + 0.5 * i_{ac_i}^2 * (L_{kP} + L_{kS}) \quad (11)$$

In literature, generally the capacitance time constant, H , is used to express the required energy storage and its unit is ms . The energy requirements, H , for SCC-DC-DC is presented in the expression 12 where S is the apparent power of the converter.

$$H = \frac{N_{phase} * (E_{CL_i} + E_{Ch_i})}{S} \quad (12)$$

Assuming a unity transformer turns ratio, Fig. 2 shows the per phase AC equivalent circuit of the SCC-DC-DC where L_k is the equivalent tank inductance, $L_k = L_{kP} + L_{kS}$, and C_b is the equivalent tank capacitance, $C_b = \frac{C_{bP}}{2} = \frac{C_{bS}}{2}$. In order to show the optimum operating point where the minimum energy storage is required further considerations are required. The frequency factor, $K_f = \frac{f_o}{f_r}$, where f_o is the operating frequency and f_r is the resonant frequency between L_k and C_b . The factor $Z_b = \frac{L_k}{L_s}$ where L_s is the series inductance of the single phase transformer, assuming a 10% impedance. Assuming $\delta_{pp} = 0.1PU$, $M_{index} = 1$ and by changing the factors K_f and Z_b with small steps from 0.55 – 1.6 and 1 – 20, respectively, the required per unit $H_{PU} = \frac{H}{H_b}$ is found at each point as presented in Fig. 3 where $H_b = \frac{1}{f_o}$ is the base capacitance constant. The optimum operating region is between $K_f = 0.75 - 1.25$ and $Z_b = 7 - 20$ where the H_{PU} is between 6.14 – 6.3 PU . However, operating at or below the resonant frequency of the LC tank makes the control over the AC current difficult. Therefore operating above resonance frequency is preferred and the $K_f \geq 1.15$ the minimum H_{PU} is obtained when $Z_b = 16$.

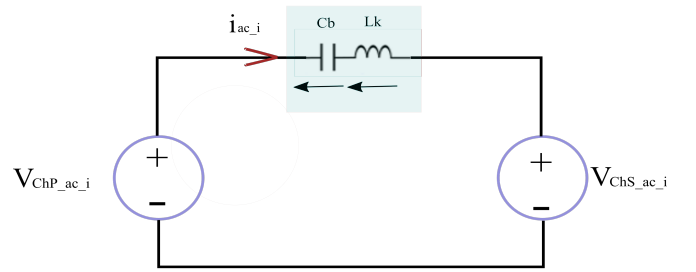


Fig. 2. Per phase equivalent circuit

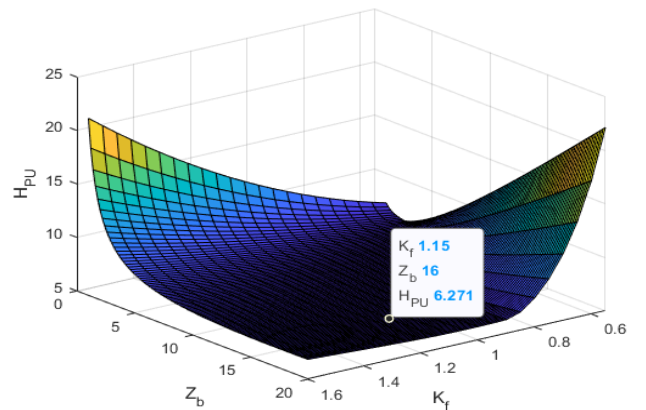


Fig. 3. Energy storage requirement analysis

In addition to a huge reduction in number of SMs, 66%, and considering the same power rating the sinusoidal operation of SCC-DC-DC converter has less semiconductor losses in comparison to the sinusoidal operation of the MMC-DC-DC

converter due to the absence of the second harmonic in the chain-link circulating current and the presence of resonant tank which filters ripple in the AC current of the SCC-DC-DC. Regarding the energy storage, in literature the SMs capacitor energy storage for the MMC-DC-DC converter has been presented (excluding arm inductors and the effect of circulating current) and it requires around 75% of the energy storage required for the SCC-DC-DC. However, if the 12 arm inductors of the MMC-DC-DC and the second harmonic in the chain-link circulating current are considered, the required H_{PU} for the MMC-DC-DC will be higher than 75% of the required H_{PU} for the SCC-DC-DC.

IV. CONTROL STRUCTURE OF SCC-DC-DC

This section shows the control schematic of the SCC-DC-DC converter and the control loops that are necessary for the operation of the SCC-DC-DC are shown. The non-linear differential function that describes the behaviour of each chain-link voltage can be linearised and approximated to the average voltage of the chain-link by using the transfer function 13 which describes the relation between the power and the average of the $\sum V_{SMx}$ of the chain-link, $V_{SMx_{eq}}$. The power is imposed at the primary side of the SCC-DC-DC converter and per phase energy control is designed at the primary side to control the energy of each chain-link and provide the desired AC power reference for the inner per phase AC current control loop as shown in Fig. 4-a by using a PI compensator where Mea represents the measured values and Ref represents the reference values.

$$G_E(s) = \frac{V_{SMx_{eq}}(s)}{P_{Chx}(s)} = \frac{1}{sV_{SMx}C_{SMx}} \quad (13)$$

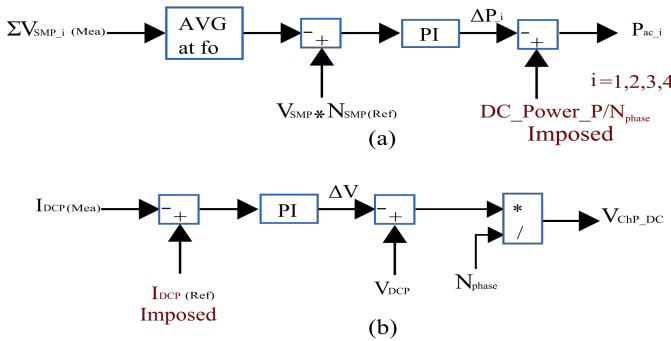


Fig. 4. (a) Primary energy control (b) Primary DC current control

The DC current controller is based on the transfer function shown in 14 which describes the relation between the DC current and the total DC voltages of the chain-links. Considering the primary side of the converter, $I_{DCP}(Ref)$ is imposed and by using a PI compensator the DC current is controlled and the DC component of the primary chain-links voltage reference is obtained as shown in Fig. 4-b.

$$G_{DCx}(s) = \frac{1}{sL_{DCx}} \quad (14)$$

The per phase AC link equation, 15, can be derived from Fig. 2 which was presented in previous section where only the AC voltage of the chain-links are considered since the DC voltages are perfectly blocked by C_{bP} and C_{bS} as previously explained. The per phase AC current control loop is the inner loop of per phase primary energy controller therefore it must be suitably "faster" than the outer energy control loop. A PR compensator with a complex zero at the resonant frequency of the AC resonant tank is designed to control the AC current and provide the AC voltage component of the secondary chain-link voltage references, $V_{ChS_{ac_i}}$, where the primary AC component of the chain-link voltage reference, $V_{ChP_{ac_i}}$, is imposed as shown in Fig. 5. a complex zero is used to cancel the effect of the complex poles of the resonant tank on the AC current response since the complex poles are close to the operating frequency due the design analysis with regards to the optimum energy requirements.

$$V_{ChS_{ac_i}}(t) = V_{ChP_{ac_i}} - \frac{1}{C_b} \int i_{ac_i}(t) - L_k \frac{di_{ac_i}}{dt} \quad (15)$$

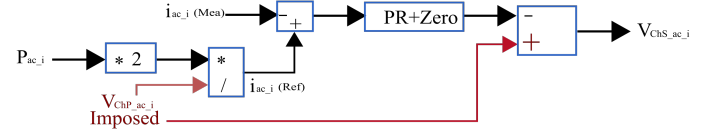


Fig. 5. Per phase AC link current control

For the secondary side of the converter, the total energy of the chain-link is controlled using a PI compensator as shown in Fig. 6-a and the same transfer function as in expression 13 describes the plant of the system. The total energy control of the secondary side of the converter provides the $I_{DCS_{ref}}$ to the inner DC current controller. Based on the same transfer function as in 14 a PI compensator is designed for the inner DC current loop to control the secondary DC current and provide the DC component of the secondary chain-links reference as shown in Fig. 6-b.

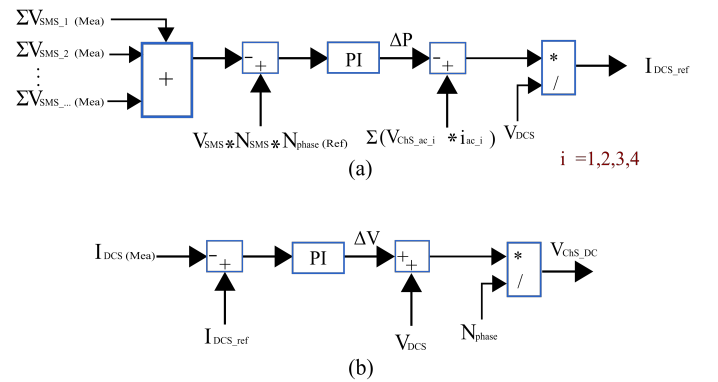


Fig. 6. (a) Secondary energy control (b) Secondary DC current control

The per phase energy controller at the primary side of SCC-DC-DC keeps the energy stored at each chain-link of the

primary side balanced during converter operation. However, having only the total energy controlled at the secondary side of SCC-DC-DC can result in the stored energy fluctuating between chain-links during operation. In order to maintain energy balance between the chain-links of the secondary side of SCC-DC-DC another control element is required. The energy balancing controllers shown in Fig. 7 provide the desired voltages that need to be added or subtracted to the reference of the chain-link voltages to equalize the energy storage of the secondary chain-links.

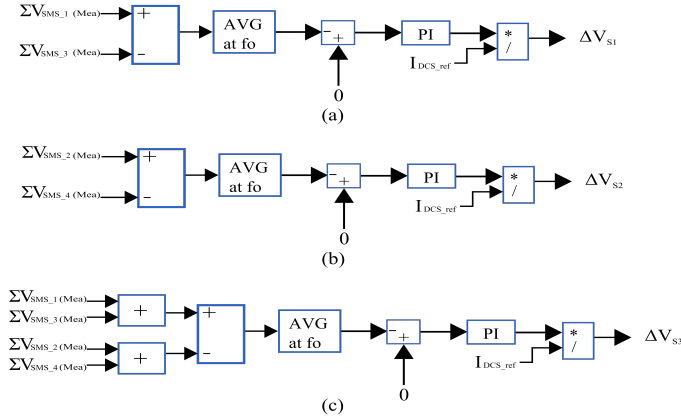


Fig. 7. Energy balancing between secondary chain-links

Fig.8-a and Fig.8-b,c show the per phase reference of the primary chain-links and the reference of the secondary chain-links, respectively. The chain-links reference will be then compared with the carrier to provide the PWM signals to the SMs semiconductor devices of the chain-links.

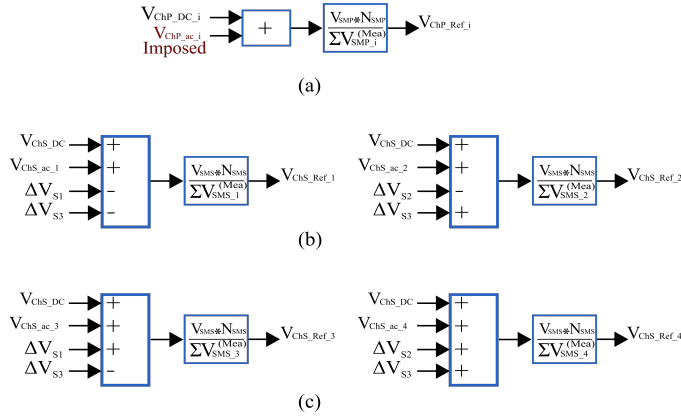


Fig. 8. (a) per phase primary chain-link reference voltage (b,c) secondary chain-links reference voltage

V. SIMULATION RESULTS

In order to validate the proposed topology, A 10MW, 20kV-20kV four phase SCC-DC-DC converter model has been developed using PLECS where the $V_{Chx_ac_i}(t)$ are shifted by $\frac{\pi i - \pi}{2}$. The four phase SCC-DC-DC parameters are shown in Table I. Fig 9 shows the AC current and the

passive components of the resonant tank voltages of phase A when the imposed DC power is changed from 10MW to 8MW. It can be observed from Fig. 9-b,c that the C_{bx} blocks the V_{DCx}/N_{phase} . The capacitor SMs voltage control and balance of the primary and secondary chain-links at the nominal value (1kV) with 10% peak to peak ripple are presented in figure 10.

TABLE I
CIRCUIT PARAMETERS

Circuit Parameter	Value
Primary DC Link Voltage (V_{DCP})	20kV
Secondary DC Link Voltage (V_{DCS})	20kV
AC Link Frequency (f_o)	250Hz
Transformer Turn Ratio (n)	1
Modulation index M_{index}	0.95
Submodule Capacitor (C)	5mF
Submodule Capacitor Nominal Voltage (V_{sm})	1kV
Primary Submodule Number per phase (N_{SMP})	10
Secondary Submodule Number Per phase (N_{SMS})	10
Transformer Leakage Inductance ($L_{kP} = L_{kS}$)	4.6mH
Capacitance of Blocking Capacitor ($C_{bP} = C_{bS}$)	0.23mF
DC inductance ($L_{dcP} = L_{dcS}$)	1.3mH

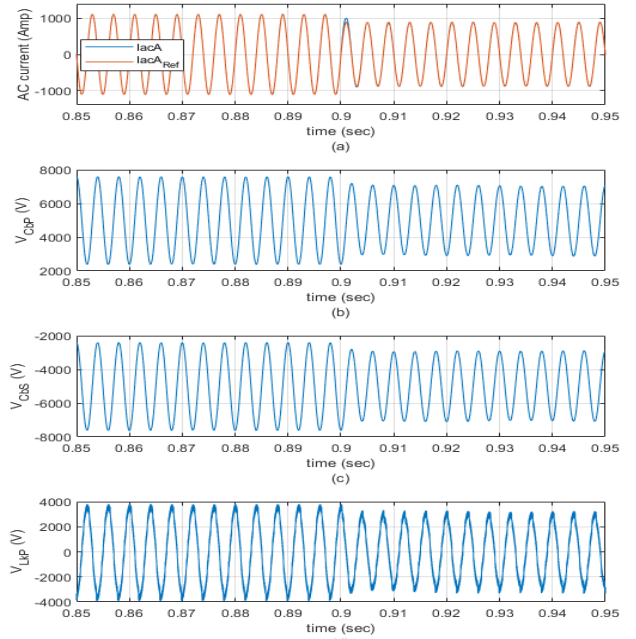


Fig. 9. (a) AC current response (b) Primary blocking capacitor voltage (c) Secondary blocking capacitor voltage (d) Primary inductor voltage

Furthermore, two operation methods have been tested to show the primary DC current response where as previously explained in the first operation method $V_{Chx_ac_i}(t)$ are shifted by $\frac{\pi i - \pi}{2}$. The second method is applicable only to a converter with even phases where the chain-link voltages for half of the phases (1 and 2) have the same phase, shifted by π with respect to the other half (phases 3 and 4) and this will be similar to two phases. Considering the same change in power,

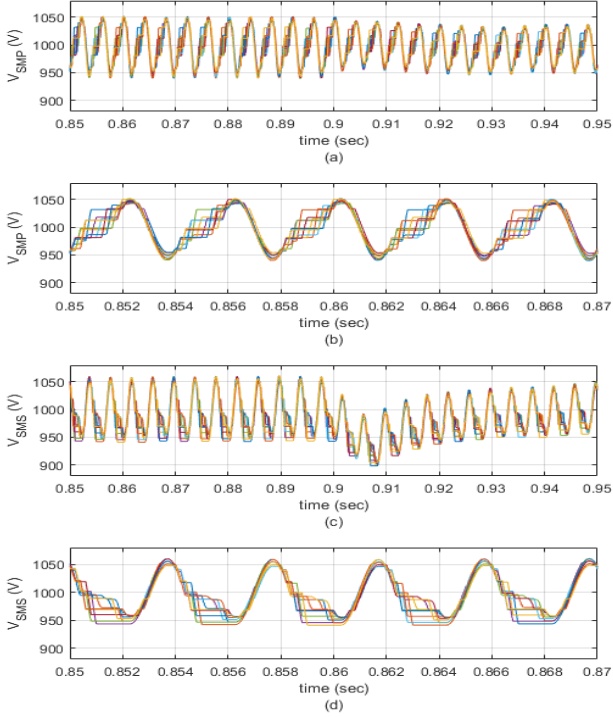


Fig. 10. (a) Primary SMs voltage (b) A small portion of primary SMs voltage (c) Secondary SMs voltage (d) A small portion of secondary SMs voltage

Fig. 11-a shows the DC current response for both operations where identical control schemes and converter parameters are chosen. It is clear that in Fig. 11-b the DC current of method 1, I_{dcP1} , has a small peak to peak ripple at $4 * f_o$, however, the method 2 DC current, I_{dcP2} , has higher peak to peak ripple at $2 * f_o$. The reason for this is the harmonic order ripple in $\sum V_{Chx_ac_i}(t)$ where in second operation there is a second harmonic ripple in $V_{Chx_ac_i}(t)$ whereas in first operation the harmonic order ripple, Hr_{or} , in $V_{Chx_ac_i}(t)$ depends on the number of the phases, $Hr_{or} = N_{phase} * f_o$. Consequently, with the first operational conditions, as the number of the phases increases the frequency of the ripple increases, and this provides the possibility to operate the converter at higher δ_{pp} . As a result, this reduces the energy storage requirements for the converter. More mathematical analysis about the effect of increasing N_{phase} on the transformer losses, converter losses and energy requirements are the subject of future work.

VI. CONCLUSION

This paper proposed a SCC-DC-DC converter for high-voltage, high-power applications. The proposed topology is based on firstly, connecting chain-links in series to reduce the number of submodules and secondly, using a reasonable number of single phase transformers instead of one three phase transformer to overcome the associated high voltage and cooling system challenges. This paper has also shown the optimum

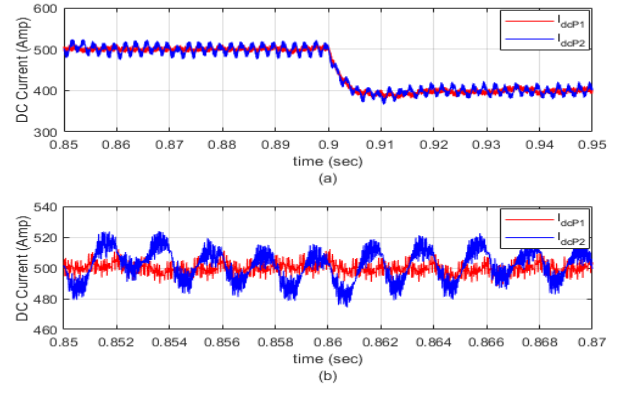


Fig. 11. (a) Primary DC current (b) A small portion of primary DC current

design region considering the energy storage requirements of the chain-links and resonant tank elements. The structure of the energy control loops, DC and AC control loops that are required to operate the SCC-DC-DC converter were presented in this paper. PLECS results show the effectiveness of the proposed topology and validate the control schemes for the proposed SCC-DC-DC converter.

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