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Research on Design Method of Low Voltage ESD Protection for Chips based on CMOS Technology

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Abstract

As integrated circuit technology continuously evolves towards nanometre scales, the susceptibility of chips to Electrostatic Discharge (ESD) under low voltage conditions has significantly increased, posing greater challenges for ESD protection design. Traditionally, ESD protection strategies have centred on high-voltage applications, employing complex and cumbersome circuits and components to enhance tolerance. However, these methods often underperform in low-voltage CMOS processes due to excessive leakage currents, increased chip area, and an inability to meet the requirements of low power consumption and high integration of devices. This study introduces a novel universal framework for low-voltage ESD protection design methods applicable to various CMOS technology standards. The framework not only compares the merits and demerits of existing mainstream ESD protection devices, ESD testing methodologies, and ESD protection networks, but also introduces an innovative analytical paradigm to holistically consider the interplay among these three facets within low-voltage ESD protection design, thereby offering fresh insights for theoretical and practical research. This universal architecture, while ensuring compatibility, also demonstrates exceptional efficiency, which represents it can be easily and swiftly applicable to different CMOS technology standards.

Keywords

CMOS; ESD; Full Chip ESD Protection.

1. Introduction

As semiconductor technology rapidly advances, the continual miniaturisation of integrated circuits (ICs) has necessitated the trend towards low-voltage operations for enhanced energy efficiency and reduced power consumption. However, this progress concurrently heightens the susceptibility of ICs to ESD, particularly under varied CMOS process standards and amongst diverse design and operational conditions. An ESD event can generate peak voltages of several thousand to tens of thousands of volts in an exceedingly brief duration, typically within a few nanoseconds. Such elevated voltages, accompanied by substantial currents, can inflict catastrophic damage upon unshielded microcircuits. Therefore, the exploration of a universal ESD protection framework, adaptable across a multitude of standards, becomes paramount to ensure the robustness and reliability of ICs operating under low-voltage CMOS technologies.

While numerous ESD protection schemes have been proffered by scholars, many are not conducive to CMOS processes under low-voltage conditions. They either fail to provide sufficient protection at reduced voltages or adversely affect the performance of chips. In summation, a comprehensive review and comparison of existing strategies are instrumental in laying the groundwork for subsequent design proposals for low-voltage ESD protection in CMOS processes.

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Through a critical analysis of extant ESD protection technologies, this study in its second methodological section particularly examines various prevalent ESD protection components, including Diodes, MOSFET, SCR, and their enhanced variants, delving into their fundamental operating mechanisms as well as the advantages and disadvantages associated with their application. Subsequently, the third section shifts the discourse to typical ESD testing methods, proffering and comparing three models utilised for evaluating the effectiveness of ESD protection mechanisms, such as the HBM&MM, CDM, and TLP testing methods. Finally, the fourth section, ESD Protection Network, builds upon the research conducted in the previous sections, introducing two fundamental architectures of local protection networks and the construction process of an full chip protection network.

2. Related Work

2.1. CMOS

Dennard et al. [1] elucidated the scaling principles for MOSFE, laying a robust foundation for smaller model of CMOS devices, whilst maintaining their performance in 1974. Subsequently, in the 1990s, the focus shifted towards reducing power consumption. Chandrakasan et al. [2] were pioneers in this regard, proposing innovative low-power CMOS design techniques that significantly influenced subsequent low-power integrated circuit designs. As technology scaled down to the nanometre regime, conventional planar CMOS faced physical limitations, necessitating the advent of multi-gate transistor structures. At this moment, Doyle et al. [3] marked a significant milestone in this domain with the introduction of the FinFET structure, demonstrating superior performance at nanometre technology nodes. Meanwhile, material innovations played a crucial role, with Robertson [4] exploring the use of high dielectric constant (High-K) materials as gate dielectrics to mitigate leakage currents and enhance transistor performance. In the last 12 years, 3D integration technology emerged as a new frontier, offering a path to continue CMOS scaling and integration. Xie et al. [5] provided a comprehensive review of 3D integration technology, elucidating its development and application in CMOS technology.

2.2. ESD

From 1982 to 1993, Duvvury and Amerasekera [6] have pioneered the discourse on the physical mechanisms underpinning ESD phenomena in CMOS devices, introducing an innovative protective structure, which led them to publish a groundbreaking paper. Sequentially, Hun-Hsien Chang et al. [7] introduced a novel ESD protection strategy, which significantly enhanced the ESD tolerance of CMOS circuits through dynamically adjusting the gate voltage of transistors during ESD events. It increased the capability to withstand ESD stress for transistor, laying a robust foundation for advancing the ESD robustness in cutting-edge CMOS technologies. In 2005, Ming-Dou Ker et al. [8] presented an enhanced SCR device for CMOS ESD protection, incorporating a dummy-gate structure to hasten turn-on speed . This seminal work not only bolstered protection efficacy but also laid groundwork for subsequent advancements in the field. In 2017, Wang's team [9] introduced a pioneering function-based technique for verifying on-chip ESD protection circuits in BGA pad-ring arrays, significantly enhancing integrated circuit robustness and setting a new standard in the field.

2.3. Simulation Tool

In 1975, SPICE (Simulation Program with Integrated Circuit Emphasis) created by Dr. Nagel [10] brought a transformative approach to integrated circuit design, enabling the simulation of circuit performance across varied conditions, which facilitated design optimization and reduced the dependency on laboratory testing, subsequently expediting electronic product development. Progressing to 1981, Silvaco's Atlas [11] emerged as a sophisticated device

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simulation tool, allowing for the precise prediction of semiconductor device performance, thereby enhancing design accuracy and profoundly influencing semiconductor device design and microelectronics technology. In 1997, TCAD [12] from Synopsys suite marked a significant stride in semiconductor process simulation, aiding in the optimization of process parameters, enhancing manufacturing controllability, and improving yield, which greatly impacted the simulation for ESD protection in CMOS circuits.

3. Methodology

3.1. Overview

In the rigorous investigation of ESD protection for CMOS integrated chips employed across a myriad of electronic devices and systems, Section II assumes the pivotal task of thoroughly analysing the characteristics and functions of ESD protective devices. It elucidates their role in safeguarding chips from the impacts of ESD incidents, thereby laying the cornerstone for low-voltage ESD protection design. Subsequently, Section III compares three typical ESD testing methodologies. It not only contributes to the establishment of a robust analytical framework but also ensures that the protective designs withstand stringent testing conditions, validating the feasibility of low-voltage ESD protection design methodologies. Finally, Section IV proffers comprehensive approaches to the development and assessment of ESD protection strategies, meeting the efficiency requirements for various protective needs and solidly grounding the subsequent research on low-voltage ESD protection design for CMOS circuit chips.

3.2. Characteristic analysis of ESD protection device

3.2.1. Diode

In fact, PN diodes have the simplest structure in ESD protection devices. It means that no additional manufacturing steps are required to create this diode, while the parasitic effect is smaller than other protective devices [13]. Figure 1 shows the structures of typical diode-based non self-protecting ESD strategy. The most classic of these, N+/P-well diodes, are often used to protect against ESD events between I/O and VSS pins, because P-well is usually connected to VSS, while

P+/N-well diodes are commonly used between I/O and VDD.

In the field of ESD protection, semiconductor diodes emerge as a fundamental and important component that exhibits unique electrical properties in both forward and reverse bias configurations. The diode always displays without snap-back, ensuring predictable performance when forward-biased, which allows conduction to begin at an approximate threshold, usually around 0.6V to 0.7V. After this threshold is reached, the diode displays minimal resistance, promoting a large amount of current flow, and the voltage difference between its two ends is negligible. The inherent low resistance allows the diode to maintain a significant current, ensuring its robustness against potential thermal degradation. In contrast, in the reverse bias setting, the diode also maintains its non-snap-back behavior. However, it experiences avalanche breakdown, which is characterized by an exponential surge in current when subjected to a reverse voltage that exceeds its inherent threshold. Therefore, the applied voltage must exceed the breakdown threshold inherent in the diode to conduct in this state. In addition, the diode inherently exhibits higher resistance within this reverse-biased avalanche domain, thus limiting its ability to adapt to large currents. Overall, the forward working diode is an ideal ESD protection device, and the reverse bias diode cannot withstand large ESD current.

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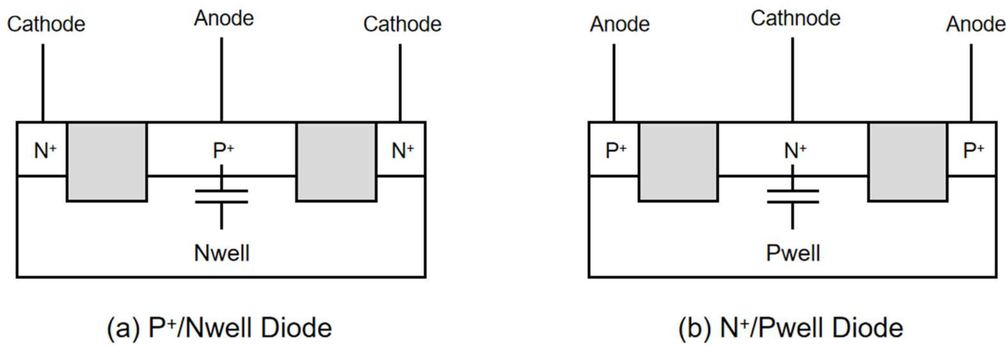

Fig.1 Two common diode structures

3.2.2. MOSFET

Metal-Oxide -Semiconductor Field Effect Transistor (MOSFET) is also one of the most widely used ESD protection devices due to its good process compatibility and simple structure. Another advantage of using MOSFET as protective devices in circuits is that no additional process steps are added due to the ubiquity of it in integrated circuits. Actually, there are two kinds of Gate-to-Grounded NMOS (GGNMOS) and Gate-to-Drain PMOS (GDPMOS) [14]. It can be seen from Figure 2 that two structure diagram of these devices respectively.

In examining the electrical response of the GGNMOS structure under forward ESD stress, it is discerned that the influence of a high electric field results in the generation of electron-hole pairs within the depletion region of the N-P reverse-biased junction between the drain and the substrate. Holes migrate to the substrate as electrons flow towards the drain, inducing a voltage drop across the parasitic resistance of the substrate. Upon this drop approaching approximately 0.7V, the forward-biased PN junction between the source and the substrate becomes activated, leading to the injection of electrons from the source into the drain via the channel, a process analogous to the conduction of an NPN transistor. If this parasitic NPN transistor possesses adequate gain, it can autonomously provide biasing for the base current. The device ceases to rely on an external voltage for base current provision once this mechanism is initiated, resulting in a decline from breakdown voltage to holding voltage, manifesting a negative resistance behaviour. This transition, commonly termed as snap-back, witnesses the ensuing holding current predominantly supplied by this parasitic transistor. However, as the ESD current amplifies, the self-heating effect of the device elevates its internal temperature beyond the melting point of silicon, precipitating thermal failure of the device, known as secondary breakdown, at which juncture the current is termed the failure current.

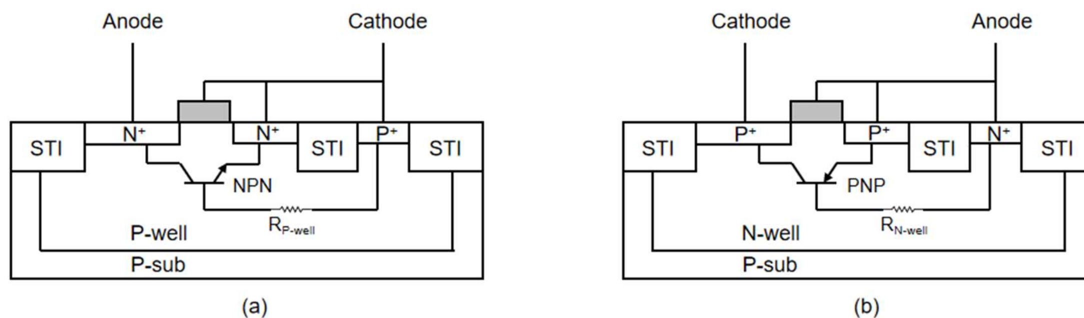

Fig.2 (a) Structure diagram of GGNMOS ; (b) Structure diagram of GDPMOS

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3.2.3. SCR

Compared to the conventional MOSFET structures, the architecture of Silicon-Controlled Rectifier (SCR) is inherently more intricate, as shown in the Figure 3, affording a broader spectrum for design alterations and optimisations. Notably, the switching characteristic of SCR to transform from high resistance state to low resistance state makes them viable candidates for certain high-power applications [15]. Yet, their typical characteristics of elevated triggering voltages coupled with diminished holding voltages have limited their direct incorporation in ESD protective schemes. Contemporary semiconductor advancements have steered circuit architectures, particularly core circuits, towards adoption of reduced operational voltages. As a result, the latching phenomenon attributed to low holding voltage of SCR isn't as formidable as a design challenge in previous iterations of semiconductor design. The current paradigm places an emphasis on methodologies to attenuate the triggering voltage of SCR. Several augmented SCR configurations have been proposed to meet these exigencies, such as Low-Voltage Triggered SCR (LVTSCR), optimised for reduced triggering voltages through doping concentration variations; Diode-Triggered SCR (DTSCR), characterised by additional diodes for expedited triggering; native-NMOS-triggered SCR (NANSCR), utilized native NMOS transistors to trigger the SCR action. The quintessence of these explorations lies in achieving an equilibrium amongst triggering and holding voltages, and energy dissipation capabilities. With the rapid evolution of semiconductor methodologies, it will be anticipated the emergence of more refined SCR configurations in subsequent technological epochs.

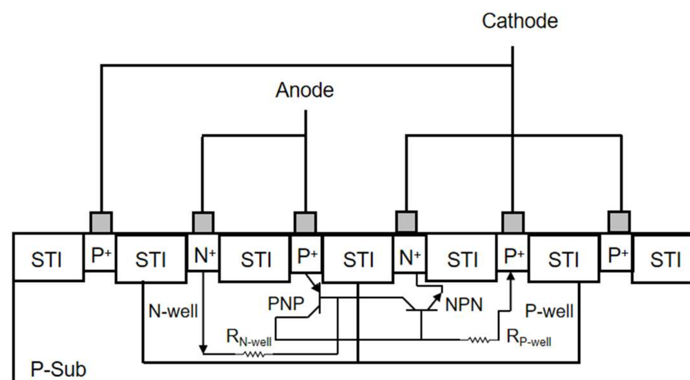

Fig.3 Cross-section of SCR device

(1) Low Voltage Triggered SCR (LVTSCR)

The Low-Voltage Triggered Silicon-Controlled Rectifier (LVTSCR) is emblematic of the pioneering SCR configurations tailored specifically for ESD protection. Its architecture is underscored by the integration of a GGNMOS, signifying a synergistic fusion of MOSFET and SCR attributes. This composite design culminates in a significant attenuation of the triggering voltage, thereby aligning the initiation voltage of SCR closely with that of the GGNMOS, given equivalent process parameters [16]. The main difference between LVTSCR and ordinary SCR in device structure is that N+ doping strategically positioned at the nexus of the N-well and P-well. The purpose of this design is oriented towards inducing avalanche breakdown more earlier in this region, thus triggering device actuation at more subdued voltages. Furthermore, introducing a gate intermediary to the N-well contact and the bridging element, which is seamlessly interfaced with the cathode, results in forming an NMOS integrated in the SCR device. This innovation recalibrates the device's activation voltage from its original N-well to P-well

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reverse breakdown sample to the triggering mechanism of GGNMOS. Such a modification optimally minimises the actuation voltage, ensuring agreement with the stipulated design benchmarks.While the LVTSCR configuration offers substantial benefits for ESD protection, it is not without its shortcomings. Specifically, the integration of GGNMOS, although reducing triggering voltages, can introduce unwanted leakage currents and potentially compromise long-term device reliability, especially under recurrent stress conditions.

(2) Diode-Triggered SCR (DTSCR)

The traditional SCR structure mainly aims to solve two problems: 1. How to raise the too low maintenance voltage (Vholding) to avoid the latch effect caused by ESD device opening. 2. How to reduce the high trigger voltage of SCR (Vtrigger) to prevent the failure of ESD protection.

The diode-chain triggered silicon-controlled rectifier (DTSCR) was proved to be a protective device suitable for low voltage working environment in nanoscale processes due to its low parasitic capacitance and adjustable trigger voltage [17]. When an ESD pulse comes, the trigger current will flow from the anode into the SCR device, then through the P+/Nwell parasitic diode and two diodes, and finally out of the cathode. The turn-on voltage of the diode string is determined by the number of diodes in series, so the number of series diodes can vary according to the voltage environment where the DTSCR is located, which means that DTSCR has the advantage of a certain degree of variability. However, the inevitable close contact of the diode string with the SCR leads to the introduction of parasitic effects and parasitic structures in reality, which can delay the switching on of the DTSCR and manifest itself in the occurrence of overshoot and multi-triggering.

(3) Native-NMOS-triggered SCR (NANSCR)

The Native-NMOS-triggered SCR (NANSCR) was proposed for more effective ESD protection under micrometer chip to quickly release ESD current and greatly improve the resistance of the components against ESD stresses [18]. The drain of the native NMOS in the NANSCR is directly coupled to the anode pad, while the drain of the NMOS in the LVTSCR is located at the n-solder well junction of the SCR device. Meanwhile, the gate of the native NMOS is connected to the negative bias circuit (NBC) to turn off the NMOS, while the gate of the NMOS in the LVTSCR is connected to the VSS to ensure that the LVTSCR turns off. Compared to the high maintenance voltage of traditional LVTSCR components, NANSCR can operate under conditions much closer to the normal pressure state, which ensures that its protection conditions are not too harsh. It is experimentally verified that a NANSCR with a 1.6 V hold voltage can be designed to avoid the latch-up problem of 1.2 V CMOS integrated circuits. The component is suitable for large CMOS integrated circuits with multiple power supply pins.

3.3. Typical ESD Test Methods

In the realm of ESD testing, three primary methods are widely used: Human Body Model (HBM) and Machine Model (MM), Charged Device Model (CDM), and Transmission Line Pulse (TLP). The HBM and MM tests replicate the static discharges that can occur when electronics come into contact with humans or machinery. The CDM test reflects the discharges from electronics that have accumulated charges during their manufacturing, transportation, or assembly. The TLP test uses specific pulse voltages to simulate actual ESD events, enabling a direct measure of a component's electrical characteristics and aiding in the design of ESD protection strategies. It is essential to repeatedly test a product under the same system to ensure reliability and consistency in results, simulating the impact phenomenon that may be encountered in the real process and actual use.

3.3.1. HBM and MM tests

The observed phenomena are notably similar in the study of ESD under the Human Body Model (HBM) and Machine Model (MM). Both models can be evaluated using the same equipment and

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test pin configurations, primarily utilising the Zapmaster test platform. Test pin configurations typically comprise combinations such as I/O pin to power pin, I/O pin to I/O pin, and power pin to power pin. Additionally, testing can be categorised based on voltage polarity, encompassing both positive and negative voltage scenarios. Further details on these methodologies are provided below.

(1) I/O pin to power pin

Considering the different situations of positive and negative voltages, as shown in Figure 4a, four distinct paradigms are elucidated: PD (positive to VDD) and ND (negative to VDD) where electrostatic stresses are applied using VDD as the reference; and PS (positive to VSS) and NS (negative to VSS) where VSS serves as the reference. ESD current is channeled via the I/O terminal, exiting through the VDD/VSS terminal while ancillary terminals remain floated during evaluations, thus emulating genuine electrostatic discharge events. The stability of a device under such conditions is often gauged by the I-V curve, which is a graph describing current-voltage relationships. Consistent curves before and after testing indicate the stability of devices, while significant drift indicates potential hazards. Generally, these modes ensure resilience against diverse electrostatic discharges, promising device longevity and reliability in real-world deployments.

(2) I/O pin to I/O pin

It is imperative to float the VDD and VSS terminals when conducting tests between I/O terminals. Given the possible variations of positive and negative voltages, the I/O terminal under examination should be subjected either to a positive or a negative voltage. Meanwhile, it is of paramount importance to ensure that all remaining I/O terminals are grounded. Such a test scenario is depicted in Figure 4b.

(3) Power pin to Power pins

There are principally two modalities when conducting ESD tests between power terminals: the positive mode and the negative mode, as depicted in Figure 4c. It is essential to ensure all I/O terminals remain in a state of floatation during the evaluation. In the positive mode, the ESD current flows into the VDD, establishing a pathway to the grounded VSS. The metric for ascertaining the success hinges upon any deviations observed in the post-test I-V curve. The negative mode operates on a similar principle, albeit with the application of opposing ESD stresses.

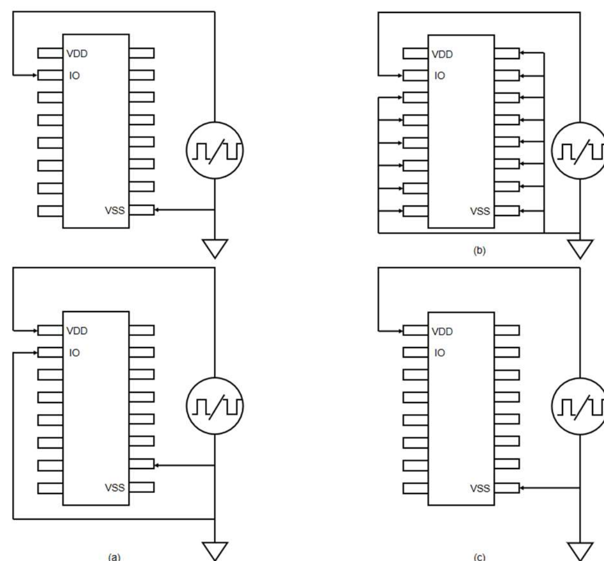

Fig.4 Test schematic (a) Between I/O and VDD/VSS pins ; (b) Between I/O and I/O pins ; (c) Between power and power pins

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3.3.2. CDM Test

The ESD mechanisms intrinsic to the Charged Device Model (CDM) stand in contrast to those of the HBM and MM. This difference inherently shapes the methodologies adopted for their respective testing. The CDM employs the specialized system of Orion Robotic to focus on individual terminal assessments within semiconductor chips. The procedure is inherently twofold. In the initial phase, a charge is applied to the substrate in IC, effectively storing an electrostatic voltage therein. It is indispensable to integrate the voltage in series with a high-resistance component because of potential damage to the IC. Notably, the pre-existing connection between the substrate and the VSS terminal for those chips featuring a P-type substrate allows direct charging through the VSS, as demonstrated in Figure 5. Following this preparatory phase, the subsequent testing step involves systematically grounding each of the additional terminals. It ensures a thorough assessment of ESD for devices.

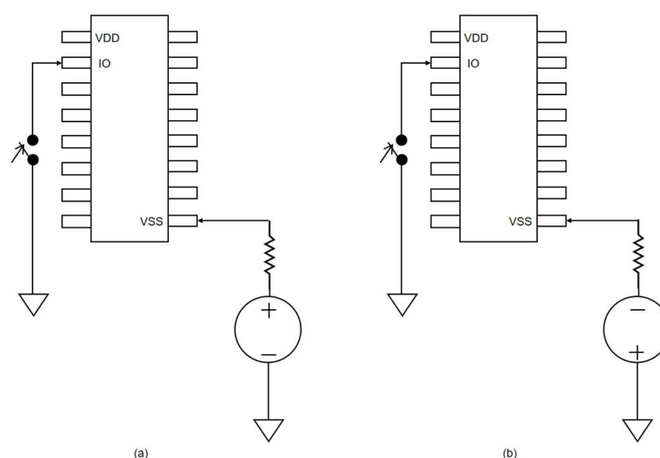

Fig.5 CDM test methods. (a) Positive ESD pulse; (b) Negative ESD pulse

3.3.3. TLP Test

Transmission Line Pulse (TLP) testing, first introduced by Maloney and Khurana at Intel for ESD studies [19], has become an industry standard for analyzing specific ESD devices. It offers consistent, reliable, and repeatable voltage waveforms, greatly assisting in pinpointing device failures. The principle of it is simulating real-world HBM waveforms by equating the energy of a 100ns TLP pulse with a 150ns waveform of the same peak current.

In practice, a pulse generator releases surges across a Device Under Test (DUT), and tools like oscilloscopes capture the device's electrical behaviour, yielding transient waveforms. Data points from the 70%-90% segment of this waveform shape the I-V curve. The system measures the leakage current after applying voltage across the DUT to determine its viability. Testing involves releasing increasingly intense pulses and stops once a significant shift in the leakage current curve is observed. This moment produces a comprehensive I-V curve. The critical failure current value where a noticeable change occurs, termed It2, serves as a measure of the device's robustness, representing a vital piece of data.

3.3.4. Comparative Analysis

Upon a thorough analysis, it becomes patently clear that ESD evaluations rooted in the HBM, MM, and CDM frameworks predominantly subscribe to a pass-through modality. Such methodologies primarily ascertain the threshold of ESD vulnerability, thus demarcating whether a semiconductor device can effectively tolerate a designated test voltage. Unfortunately, they offer little insight into dynamic performance alterations or supplementary test metrics throughout the evaluation. In contrast, the TLP test emerges as a notably sophisticated tool, elucidating a full range of pivotal ESD parameters, encompassing the trigger

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voltage (Vt), the intrinsic on-resistance (Ron), the holding voltage (Vh), the characteristic snapback voltage (Vs), and the critical failure current (It2). Such intricate parameters, in essence, furnish a comprehensive characterisation of ESD paradigm for a device. As a result, TLP analysis has been recognised as an indispensable instrument for refined ESD modelling in the field of research.

3.4. ESD Protection Network

ESD protection in CMOS integrated circuits necessitates a approach to safeguard sensitive components from potential irreversible damage resulting from external ESD events, such as human body discharges. It is imperative to provide a path with minimal impedance for ESD current, allowing it to swiftly traverse from input/output terminals to the ground, bypassing delicate transistors. Distinct strategies, including the placement of localised ESD protection near specific I/O pins or modules and a comprehensive chip-level ESD network especially when multiple power domains are present, are paramount. Every I/O terminal needs to be properly protected, and at the same time, validation with appropriate ESD test models such as human body models (HBM), machine models (MM), and charged device models (CDM) is critical. Furthermore, the nuances of different fabrication technologies and dimensions necessitate tailored ESD mitigation approaches.

3.4.1. Local ESD Protection Network

In the context of on-chip ESD protection design, factors such as chip dimensions and pin count hold substantial influence. Therefore, the architecture of on-chip local ESD protection networks will vary with distinct design parameters. Two predominant paradigms emerge in this domain: the power rail ESD local protection and the PAD-oriented ESD local protection. The former emphasises the deployment of protection mechanisms between the power rail and the ground, facilitating a rapid conduit for ESD currents to the ground or power rail, thereby bypassing internal circuitry. It favoured for its capability in efficiently diverting sizable ESD disturbances without disturbing regular circuit operations, commonly incorporating diodes, SCR, and specific MOS configurations. Conversely, the PAD approach, as delineated by its nomenclature, prioritises the safeguarding of the input/output pads of CMOS integrated circuits, positioning protective apparatus to the PAD to guarantee instantaneous intervention during ESD incursions. Such a strategy ensures immediate mitigation of any ESD event at the PAD level, avoiding its potential penetration into the interior circuitry. Diodes, SCR, and specialised MOS structures remain prevalent in this strategy, albeit with nuanced design alterations. Ultimately, the election between these paradigms stems from the specific requirements of chips, with each methodology proffering unique merits, swayed by the chip's intended utilisation, architectural considerations, and anticipated ESD challenges.

(1) Power rail ESD local protection

In the realm of ESD protection design based on power rails, it is distinctive that all protective elements, in conjunction with power pins, are connected to a unified power rail and ground rail. Such an architectural preference ensures that, in the event of an ESD disturbance between any two arbitrary pins, a direct dissipation pathway for the current is invariably present, facilitating rapid redirection of the ESD current into the ground or power rail, thus bypassing potential detrimental effects to the sensitive regions of CMOS integrated circuit. It provides a low-impedance conduit for all possible ESD currents, essentially preventing unintentional current passing through and subsequent damage to other parts of the CMOS integrated circuit.

(2) PAD-oriented ESD local protection

Within the domain of ESD protection architectures, the PAD-oriented methodology emerges as notably effective in scenarios characterised by a restricted quantity of chip pins or when there exists an urgency for the economisation of chip surface area. This paradigm, by its very design ethos, offers a targeted safeguarding mechanism for the I/O pads, ensuring that ESD

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disturbance at the PAD interface are swiftly attenuated, thereby forestalling potential intrusions into vulnerable regions of chips.

3.4.2. Full Chip ESD Protection Network

The traditional model focusing solely on local ESD protection for singular power supply configurations is increasingly superseded in the evolving landscape of semiconductor technology. There is a conspicuous amplification in chip complexity, resulting a propagation of IP modules. The combination of diverse circuitries, namely digital, analogue, RF, and high-voltage integrated variants, onto one cohesive chip substrate has become a recurrent mode. Notably, while digital modules exhibit a preference for reduced supply voltages to reduce power dissipation, their analogue counterparts often necessitate elevated supply voltages to optimise operational alacrity. This dichotomy results in a distinct shift towards multi-power domain designs in contemporary chip architectures. Given this various backdrop, ESD protection strategies necessitate not merely fortifying localised networks but also particularly orchestrating inter-domain protective measures, ensuring immunity from potential adverse ESD disturbances.

It could be observed in Figure 6 that an archetypal ESD protection topology tailored to cater to the complexity of mixed-signal circuits, encompassing a multifaceted array of power domains. This configuration distinctly splits into four salient power rails: VDDL, VSSL, VDDH, and VSSH. When considered the confines of a 0.18um CMOS technological paradigm, VDDL emerges as a 1.8V supply dedicated to the core digital apparatus, while VSSL delineates the corresponding ground. Meanwhile, VDDH and VSSH are designated as the supply and ground for digital entities integrated with a thick oxide construct. Besides, AVDD1 and AVDD2 differentiate the 1.8V and 3.3V allocations, respectively, and AVSS1 and AVSS2 are the power supply ground, purposed for the core analogue components and their thick oxide counterparts. Within the schematic under scrutiny, the numerically annotated rectangles represent distinct ESD protective network, with potential configurations spanning both bidirectional and unidirectional modalities. For example, entities noted as '1' and '2' are primarily tailored for I/O protective measures, whilst the entity labelled '3' is specifically designated for the safeguarding of interconnectivities between power rails. It warrants emphasis that the presented protective topology is symbolic. Therefore, inherent flexibility exists for either expansion or diminution of the protective constituents based on specific protective requirements.

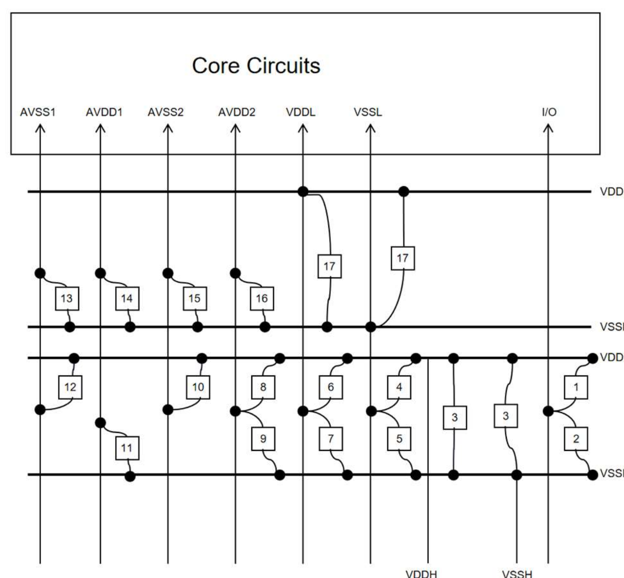

Fig.6 ESD protection network based on multiple power domain

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4. Conclusion

In this study, a new universal framework for low-voltage ESD protection design, suitable for a variety of CMOS technology standards, has been proposed. By comparing current mainstream ESD protection devices, ESD testing methodologies, and ESD protection networks, the framework constructs a foundational structure from basic protection to validation of design feasibility to enhancement of protection efficiency, emphasising its effectiveness and reliability under low-voltage operating conditions. Given the trend of IC technology towards lower power consumption and higher energy efficiency, ESD protection strategies adaptable to varying process standards are particularly crucial. This framework not only meets such demands but also accommodates the complexity and diversity of design. Through an in-depth analysis of protective components such as Diodes, MOSFET, SCR, and their enhanced variants, combined with testing models like HBM&MM, CDM, and TLP, this study establishes an empirical foundation for verifying the effectiveness of ESD protection mechanisms, whether through local or whole-chip protection networks. It also fully considers the demands in integrated circuit design for compactness and low power usage, aiming to achieve the optimal balance between the two. Thus, it ensures the safety of chips during ESD events while maintaining their compactness and energy efficiency. In summary, this universal architecture not only offers an innovative approach to low-voltage ESD protection but also paves the way for adaptation to future standards, anticipated to bring long-term benefits to the semiconductor industry.

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