

Article

Control of Power Electronics through a Photonic Bus: Feasibility and Prospects

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Abstract: The ubiquitous diffusion of Power Electronic Converters (PECs) in many fields of application including traction and energy conversion is suggesting the possibility of new and better integration of advanced power conversion and ICT services. This work investigates the possible advancements in the use of optical fibers for control of PECs, using Plastic Optical Fiber. The optical communication link connects the switching control to the converter control, following the line of separation between the expertises of the power electronic engineer and the control engineer. Control wise, the PEC becomes a black box compatible with any off-board controller, now immune from the Electromagnetic Interference (EMI) produced by the power switches. The redundant optical link is ready for the high switching (and sampling) frequencies possible with the use of SiC power semiconductor devices (100 kHz+). Distributed control of multiple PEC units and advanced telemetry for diagnostics and prognostics are targeted. A proof-of-concept demonstrator is presented and tested. Moreover, the possible evolution towards a power electronic cloud with remote management and orchestration is described.

Keywords: Plastic optical fiber, power electronics, remote control, SiC power devices

1. Introduction

Power electronic converters (PECs) are assuming a fundamental role in the modern society. Their growing diffusion is driven by the progress of transportation electrification (electric vehicles, more electric aircraft) and the new needs of energy grids (distributed generation from renewable sources calling for distributed power electronics, as well as EVs charging infrastructures and energy storage needed to handle the grid stability). The scaling demand for power conversion triggered the development of new devices such as SiC power mosfets that were considered too costly and unreliable until very recently.

This work deals with advancements in the use of optical fibers for control at switching level of PECs made with SiC power devices, aiming at the definition of a serial communication standard for the control of the PEC using Plastic Optical Fiber (POF).

In the literature, optical fibers are applied to PECs in different suboptimal ways, such as to command the gate drivers of the power devices, to sense their junction temperature, or to supply the gate drivers through power over wire in high voltage applications [1],[2],[3]. In all the reported cases, the optical link is used in "one signal per fiber" manner. In the late '90s the US Office of Naval Research promoted the standardization of PEBBs (Power Electronic Building Blocks) for shipboard power electronics [4], later adopted by ABB and other industrial players for medium and high power converters [5]. The PEBBs are "power processors" including power hardware and sensors, with minimal digital intelligence on board dedicated to hardware protection, execution of switching commands and serial communication with an external controller. The serial communication from the PEBB to the converter control unit is often realized with plastic optical fibers (POF): the dedicated communication

36 protocol PESNet was developed, running on a 125 Mb/s serial communication line implemented on a
37 Hard Clad Silica optical fiber [6]. The control architecture of PEBBs was formalized in [7], for 1MW+
38 power electronics. In turn, the main focus of the PEBB projects was on standardization of the power
39 blocks, pursuing a system-level approach to the design of power electronic converters rather than on
40 exploiting the advantages of optical communications. The efforts on the communication link were all
41 in the direction of composing multiple blocks to make one single PEC, i.e. synchronization between
42 modules, fault tolerance and plug-and-play features [8],[9]. Dealing with industry applications, the
43 most significant result of the PEBB approach is the AC 800PEC controller from ABB, capable of
44 controlling up to 36 synchronized PEBBs via the proprietary optical PowerLink protocol, with a cycle
45 time of 25 μ s. This was released one decade ago and was meant for rapid prototyping of PECs, and
46 takes advantage of model-based design in Matlab/Simulink and Matlab embedded coder. A good
47 review of communication protocols for PECs is in this recent publication [10]. Moreover, Aurora
48 8B/10B by Xilinx is used for hardware in the loop (HiL) testing of a PEC controller [11].

49 Despite the cited examples, the use of optical fibers in PECs control remains limited in everyday
50 power electronics, missing to catch the new opportunities arising from higher demand and new power
51 devices. This work proposes an original protocol for real-time control of PECs using POF. In accordance
52 with [7], the optical communication link is placed between the switching control (on board of the PEC)
53 and the converter control (off the PEC), on the line of separation between the expertises of the power
54 electronic engineer and the control engineer. In this way, the digital hardware on board of the PEC
55 is minimized and purposely designed to be EMI-immune and reusable for any PEC structure, in
56 standardized manner. Therefore, any real-time controller can be associated to the PEC via the optical
57 communication, not subjected to the EMI produced by the power switches nor to any related design
58 restriction.

59 One discontinuity with the past is that the priority here is to optimize the use of optical
60 communication for one single PEC, targeting the exploitation of new SiC power modules. These power
61 devices permit higher switching frequencies at the cost of more severe electromagnetic interference
62 (EMI). The keys to make this idea successful are that the communication protocol must be:

- 63 • as fast as possible, to minimize the overhead time required by data transmission and decodification;
- 64 • as simple as possible, foreseeing its implementation on a low-cost, dedicated integrated circuit.

65 Short overhead time permits to push the switching (and control sampling) frequency to the higher
66 limits possible with SiC power MOSFETS (100kHz +). Room for more data permits more feedback
67 data signals to be added for PEC diagnostics and prognostics computed off board.

68 A proof-of-concept demonstrator was presented, capable of controlling a 100W-brushless
69 servomotor via a three-phase voltage source inverter [12]. The demonstrator utilizes a Xilinx Artix
70 FPGA and integrated optical transceiver for ease of development. The goal of this paper is to finalize the
71 approach towards a standardized, dedicated integrated circuit. As byproduct, this will be applicable
72 also to modular PEBBs, i.e. to the composition of multiple converter modules as building blocks,
73 for example in multi-level converter architectures with distributed control. Although not explicitly
74 optimized for, the proposed protocol is already capable to manage 10+ devices in real-time using
75 time-division multiplexing, with a distance of 40m between each node.

76 One foreseeable application is in the field of real-time hardware for development of PECs control.
77 Key players in this field [13] would benefit from a standardized optical interface for commanding
78 PECs, both for rapid prototyping and HiL.

79 Moreover, the proposed technology will enable power electronic clouds of power electronic
80 systems that will possibly benefit of a software-defined remote management and orchestration.
81 Telemetry data from the power electronic cloud will be exploited together with aggregated data
82 from users for a holistic optimization.

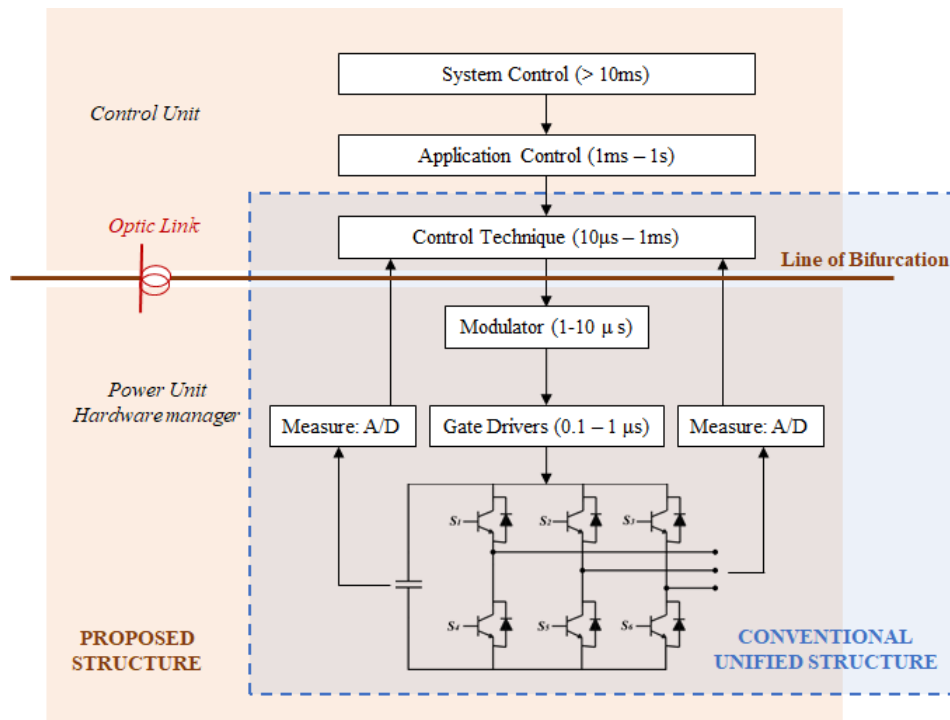


Figure 1. Common control layers for a PEC. Conventional and proposed solutions are highlighted.

83 2. Data Communication in Power Electronic Converters

84 Data communication in a PEC has been formalized in [7] as reported in Fig.1, following the
 85 organization by layers typical of data networks (e.g., ISO/OSI). The system control defines the
 86 objectives of the power electronic system and directs the functioning of application control layer
 87 towards that end. The converter layer subsystems that fall beneath the application control layer can
 88 be mimicked by a controlled current or a voltage source. The converter control layer implements the
 89 functions by determining the voltage references to be sent to the modulator (if any) of the switching
 90 control layer. The bottom-most hardware control layer manages the power devices.

91 A pertinent example is a wind farm where the power system operator (system control layer)
 92 dictates the required active and reactive power injection into the grid. The application control layer
 93 decides upon the working of each individual wind turbine (converter control layer) considering the
 94 optimum efficiency, reliability and maintenance.

95 It is emphasized that the latter two layers – switching and hardware control layer – are
 96 independent of the final application and are common for any PEC. This forms the basis of the replicable
 97 and modular PEBBs with minimum on-board intelligence to implementing switching control functions
 98 and a communication link to an external controller which, in turn, facilitates distributed control
 99 architecture and remote processing. A conventional PEC has a Microcontroller Unit (MCU) on-board
 100 for converter control, as depicted in Fig. 1. In the proposed structure, instead, the PEC ends with
 101 a switching controller, called hardware manager in [8], and delegates the converter control to an
 102 off-board control unit upstream via the optic link.

103 3. Photonic bus: Implementation and protocol

104 The photonic bus connects the Control unit and several PECs configured in a daisy chain through
 105 a bus made of a fiber pair. In the following, downstream refers to the command flow going from the
 106 control unit to the PECs while the upstream refers to the data stream from PECs to the control unit.

107 As commercially available fibers and transceivers are targeted, a pair of optic fibers are employed
 108 – one fiber for up-streaming and the other for down-streaming – to connect the Control unit to the first

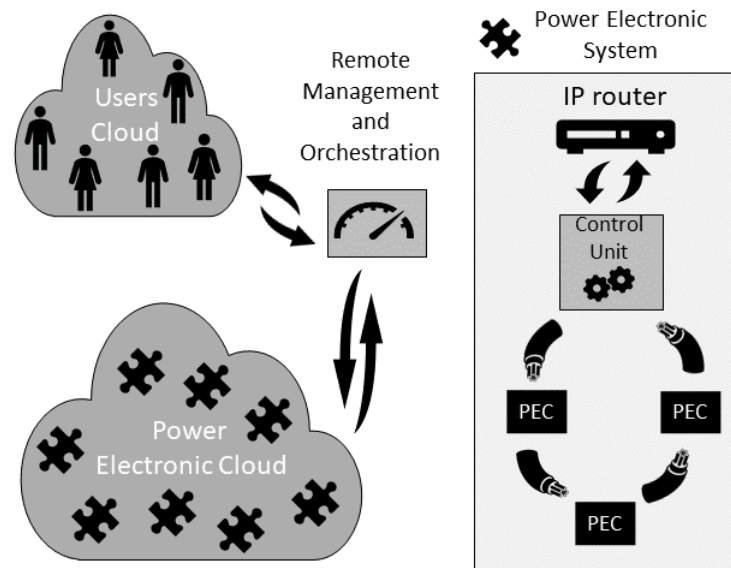


Figure 2. The daisy chain control scheme (right inset) as an element of the power electronic cloud

109 PEC, and each PEC to the following one. Such fiber pairs are widely commercially available from
 110 the main plastic optical fibers manufacturers and are directly compatible with transceiver optlocks.
 111 Couplers/splitters have been developed for plastic optical fibers as well, thus allowing the use of a
 112 single fiber carrying both upstream and downstream transmission, but they are not common as they
 113 introduce a distance penalty due to their high attenuation.

114 The daisy chain of many PECs is built using two transceivers on each PEC. Both downstream
 115 and upstream messages are received, decoded and then forwarded to the next node, down the chain
 116 for downstream messages or towards the control unit for upstream messages. Each PEC has its own
 117 address in the bus, which is used to correctly receive messages from the control unit or to tag the
 118 upstream data sent by the node. Given this decode-and-forward point to point structure, no collision
 119 is expected to happen in upstream transmission.

120 Besides the enumerated advantages of the optic link, it facilitates the integration with cloud
 121 and thus follows the Internet of Things paradigm. As displayed in Fig. 2, the Control Unit can be
 122 connected to an IP router to enable networking among several power electronic systems within a
 123 Power Electronic Cloud distributed in the Internet, according to the paradigm of the Internet of Things.
 124 The daisy chain control bus, besides enabling a remotized control by the Control Unit, may transport
 125 telemetry data that can be conveyed through the Internet in upstream, or may deliver in downstream
 126 the commands coming from the Internet to each PEC. So, the power electronic systems are virtually
 127 placed within a cloud relying on the Internet data transport to connect systems one to each other. Such
 128 a paradigm may enable the implementation of software-defined remote management and orchestration
 129 aimed at optimizing management of different systems and orchestrating their collective effectiveness.
 130 Depending on the specific application, the orchestrator could also benefit from the data from a cloud
 131 of users that may greatly help in optimizing the overall effectiveness of the power electronic cloud. An
 132 application field for which this approach could be largely beneficial is the generation of electricity from
 133 renewable sources. In this case, the power electronic systems are electricity generators – solar cells,
 134 wind turbines, etc – and the users are families and companies delivering data on power consumption.

135 3.1. Description of the protocol

136 Figure 3 describes the timing organization of the sampling and switching task. The switching
 137 frequency of the power devices dictates the sampling and switching period of the PEC. This is marked
 138 as T_{PWM} in Fig. 3 although not necessarily meaning that all PECs use Pulse-Width-Modulation. Typical

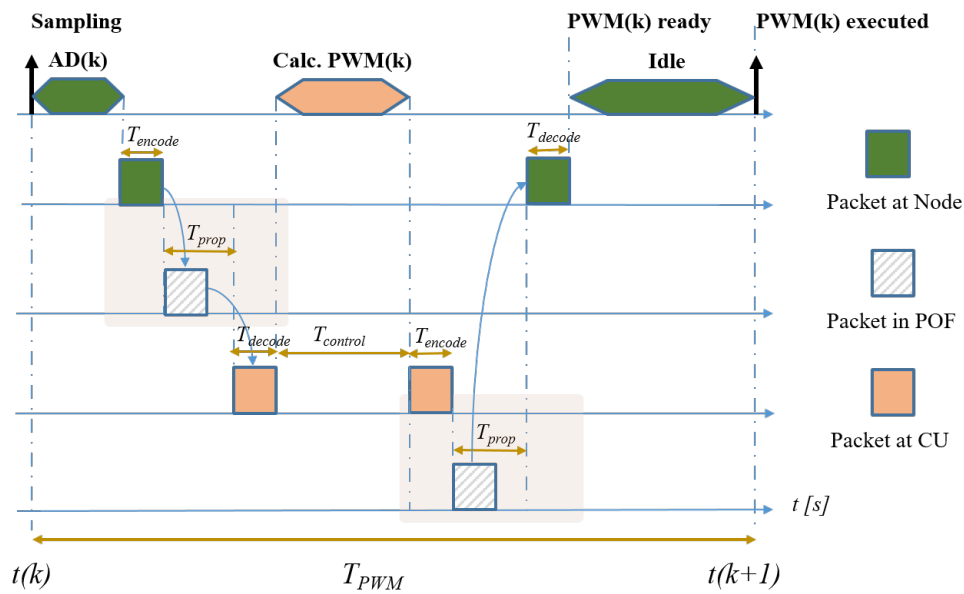


Figure 3. Timing diagram of the proposed optical link.

139 switching frequencies are in the order of 10 - 20 kHz, but the use of SiC power semiconductors is
 140 pushing these numbers higher, to 100 kHz and more in some cases.

141 At $t(k)$, the current flowing in the inverter legs is sampled by the ADC converters on the power
 142 unit (node) and is ready to be transmitted to the control unit; the time needed to transmit (T_{encode}) and
 143 receive the packet (T_{decode}) is the time needed to perform the parallel to serial and serial to parallel
 144 conversion of the 66bit words used by the 64/66b line protocol used, plus the protocol encoding
 145 and decoding overhead and the latency introduced by the clock and data recovery logic. T_{prop} is the
 146 propagation time of the light along the optical fiber; some time ($Calc.PWM(k)$) has to be reserved to
 147 the algorithm execution in the control unit microcontroller, while some idle time at the end of the cycle
 148 is needed to ensure that the new PWM values are correctly updated before the next cycle starts.

149 The overall Transmission time is defined as one-way total time to pass the data packet from one
 150 node to the other.

151 3.2. Transmission Overhead

152 Respect to a standard PEC control scheme, having the MCU on board, the optical communication
 153 introduces a time overhead equal to two transmission times. It is thus important that the transmission
 154 time is as negligible as possible, respect to the switching period. A transmission time in the order of
 155 $1\mu s$ is considered negligible. Figure 4 shows the ideal protocol performance, obtained considering
 156 only the bitrate of transmission and the propagation time of light in the plastic fiber, without taking in
 157 account implementation dependent latency overheads.

158 Our transmission protocol is based on 132bit packets, encoded as a couple of consecutive 66b
 159 words: the first word is tagged as /START (Block field type 0x78), while the second is tagged as /STOP
 160 (Block field type 0xFF), so each packet is able to carry up to 14 bytes of payload. The 66b sync header
 161 is always set to "10", i.e. control + data words.

162 Of these 14 bytes, the first byte contains the node address in the daisy chain (destination in the
 163 downstream from control unit to power node, or source node in the upstream from the nodes to the
 164 control unit), while the last byte is used to read/set discrete I/O pins present on the node itself. The
 165 remaining 12 bytes are organized as six 16 bit words; they contain ADC sampled data in the upstream
 166 channel and PWM duty-cycle values for the downstream. Further extensions of the size of the packet
 167 must consider the rules of the line protocol, so they can be done adding 64 bit data words (66 bits

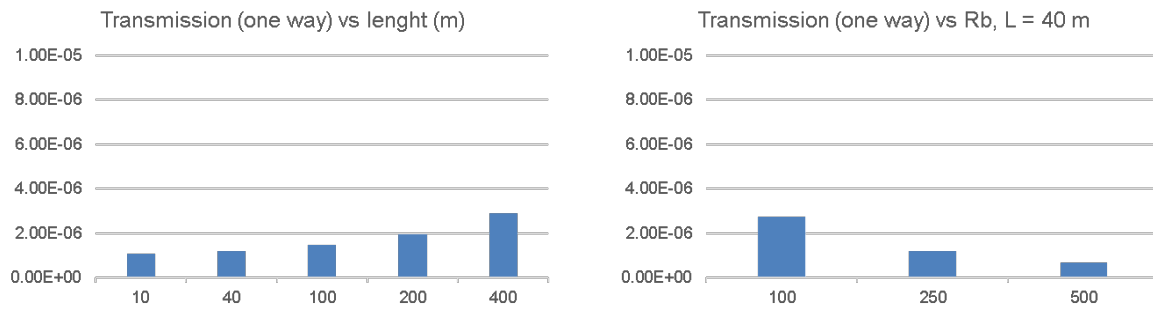


Figure 4. Sensitivity of transmission time to line length, bit rate and number of 16-bit words

168 when coded, marked with header 0 1) between Start and Stop frames. When data packets are not
 169 transmitted, the channel is filled with /IDLE words (Block Field 0x1e), as shown in Fig.5.

170 4. Proof-of-Concept Demonstrator

171 When building the proof of concept, in addition to the timing requirements explained in the
 172 previous section, the total cost and the relatively short fiber distance requirements are also considered.
 173 The system cost and ease of use constraints promoted in choosing an integrated, tool-less transceiver
 174 solution commercially available: the optolock design allows for establishing a connection by just
 175 cutting the fiber ribbon with a pair of scissors and locking it into the correct position. As short distances
 176 are targeted, POF optical bandwidth does not deteriorate received data; hence, it is not necessary to
 177 reconstruct the transmitted waveform using A/D conversion and filtering implemented in Digital
 178 Signal Processing [14].

179 The fiber itself is a simple PMMA Poly Methyl Meta Acrylate plastic fiber, standardized as A4a.2;
 180 it has a large core diameter (980 μm) covered with a thin (10 μm) layer of cladding, so it can be
 181 deployed without using specialized tools, but it has two main disadvantages, a large attenuation
 182 (180dB/Km using red light at 650nm, such as the one used by the transceivers we have chosen) and a
 183 low bandwidth length product (about 40MHz per 100m), which limit the possible maximum length
 184 and the maximum data rate.

185 The strict real-time requirements impeded to relying on a Forward Error Correction code as the
 186 Reed Solomon 237,255 used in [14], limiting the link length to the 40m at 250Mb/s declared by the
 187 transceiver manufacturer. In order to successfully operate the optical channel, both DC balancing and
 188 an adequate data transition density are needed: these requirements are fulfilled by adopting a line

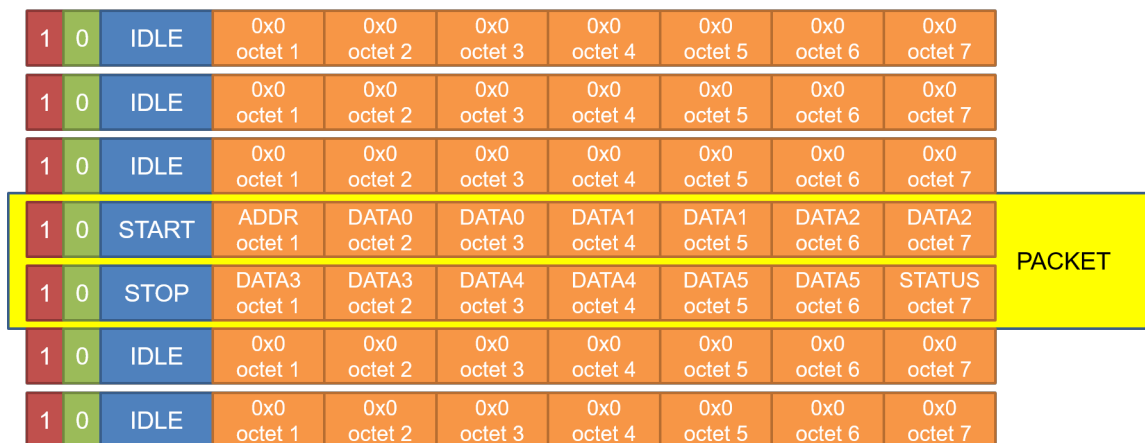


Figure 5. Example of packet flow.

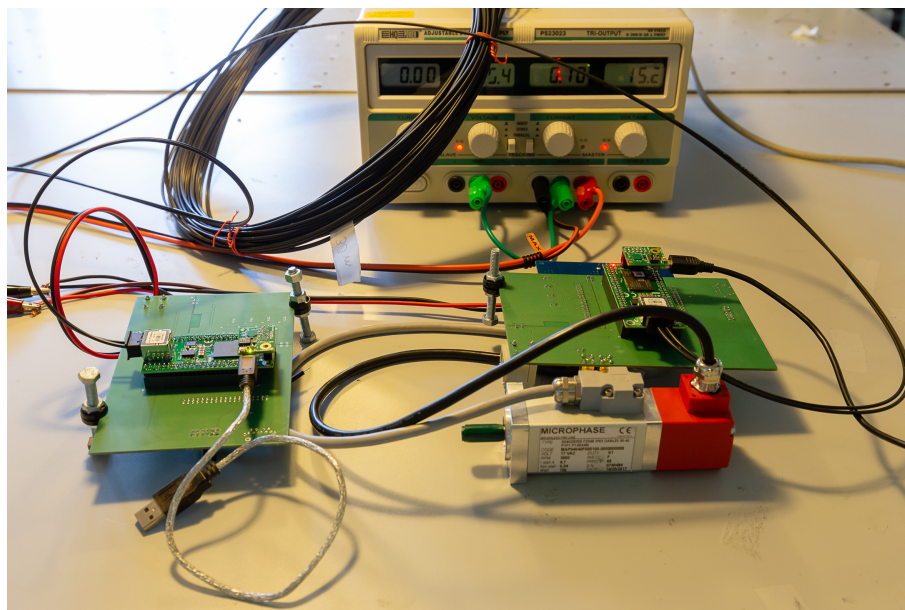


Figure 6. Demonstrator setup.

189 code such as the 64/66b. This line coding is widely adopted – e.g., in 10G Ethernet – because it requires
190 a 2 bit overhead over 64 bit words with a limited 3% overhead, and enables a more efficient data
191 transmission. Moreover, the transition density and the DC balancing are randomized by scrambling
192 the data and control words with a known polynomial before optical transmission.

193 On the power unit, i.e the remote node, a Finite State Machine takes care of handling PWM update
194 and ADC sampling. On the Control Unit, as soon as a packet is received, an interrupt is raised and the
195 microcontroller core can access those values on five registers, memory mapped on a known location
196 on the system AXI bus. Once the algorithm computation is completed, the updated PWM duty cycle
197 values are written on the registers of the transmit section and the downstream packet is ready to be
198 sent to the target node.

199 The first trials have been performed sharing a single clock all over the network to synchronize
200 transmitters and receivers. As a further development step, a clock and data recovery section has been
201 added to each of the nodes to take care of the small frequency differences among nominally equal
202 clock sources. Among all the possible clock and data recovery approaches, a fully digital solution able
203 to recover all the incoming bits is selected. Incoming asynchronous data stream is oversampled at
204 4X its nominal rate and the recovered bits are inserted in a FIFO, deep enough to account for small
205 clock variations and jitter. As it is typical for this solution, the receiver FIFO that moves data from the
206 asynchronous clock domain to the internal system clock can encounter an underflow (the clock on the
207 receiver is slightly faster than the transmitter) or an overflow condition. The control logic solves this
208 situation by adding/removing an IDLE word after the descrambling section of the 64/66b decoder.
209 This operation is safe because the optical bus is mainly filled with IDLE words with only occasional
210 data packets: as we are dealing with a real time control system, the performance bottleneck is not the
211 available bandwidth, but the total latency.

212 The remote node was built around a commercial mini-module with a Xilinx Artix FPGA, an
213 integrated optical transceiver and two 2.54 mm spaced expansion slots; and the two units are connected
214 by a 40 m POF pair and successfully managed to control a three-phase voltage source inverter, used
215 for vector control of a brushless servomotor. The servomotor is rated 100 W, 3000 rpm, and the PEC
216 is a X-Nucleo-IHM08M1, a 60 V dc input, 15 A ac output expansion board for STM32 Nucleo boards
217 by ST-microelectronics. The PEC and servomotor are purposely off-the-shelf equipment and of small
218 size, as the emphasis here is on demonstrating the real-time control capability via POF. A custom

Table 1. Power unit occupation

Resource	Utilization	Available	Utilization percent
LUT	8024	63400	12.6
LUTRAM	341	19000	1.8
FF	11084	126800	8.7
BRAM	8	135	5.9
IO	34	210	16.2
MMCM	1	6	16.6

Table 2. Control unit occupation

Resource	Utilization	Available	Utilization percent
LUT	13036	63400	20
LUTRAM	1047	19000	5.5
FF	14700	126800	11.5
BRAM	35.5	135	26.3
DSP	6	240	2.5
IO	24	210	11.4
MMCM	1	6	16.6

219 adapter board has been developed to connect the FPGA module to a ST expansion board and to a
 220 second optical transceiver to daisy-chain more units. In table 1 we report the occupation of the Artix
 221 100 device hosted on our minimodule: as the occupation is low, simpler (i.e. with smaller FPGA)
 222 mini-modules will be considered to lower the total remote module cost.

223 For the control unit, the first trial were performed with the same mini-module as the remote node,
 224 but this time instantiating a full Microblaze microcontroller with built-in floating-point unit running at
 225 100MHz. The control code has been written using standard C language, so it will be simply recompiled
 226 when targeting other cores; it has a small footprint (a few KB of RAM) and it can be executed from the
 227 embedded BRAM blocks present on the ARTIX device. The FPGA occupation reported by Vivado is
 228 presented in table 2.

229 The second set of trials will run on a commercial board with a higher performance Xilinx Zynq
 230 XC7Z010 FPGA: such a component is suitable to our prototyping purposes, having on board both
 231 FPGA resources (needed for the real time optical communication) and a real 600+MHz ARM A9 core
 232 with its embedded peripherals; the optical transceiver will be added on a custom board using an
 233 expansion connector.

234 Further work will see to the implementation of advanced control algorithms on this higher
 235 performance platform, enabling smarted power conversion, and the telemetry section needed to
 236 upload working data on a cloud data pool, making remote monitoring and fault analysis feasible.

237 5. Conclusions

238 The use of a plastic optical fiber bus in order to implement a remotized control of several
 239 power electronic converters has been proposed. This solution follows the recommendation [7] for a
 240 multi-layer structure in controlling PECs. In particular, the converter control and the preceding layers
 241 are assigned to a control unit while the switching and the hardware control layer forms the power unit,
 242 communicating through a fiber optic channel. For the optical bus, a daisy-chain structure has been
 243 proposed, enabling the connection of up to 10 PECs; each optical link can have a maximum length of
 244 40 meters. Each PEC can use a packet carrying 112 bits of payload for bidirectional communications,
 245 thus enabling control remotizing, telemetry and remote orchestration. These capabilities, together
 246 with the enforcement of the power electronic system with an IP router, may enable clouds of of power
 247 electronic systems according to the Internet of Things paradigm. Such a prospective can permit a

248 remote software-defined management and orchestration of many power electronic systems, taking
249 also advantage of data from the possible communities of users.

250 A proof-of-concept demonstrator has been implemented and presented, showing the feasibility of
251 such an optical control structure: the tests showed the implementability of such a communication bus,
252 proving the possibility of remotely controlling a motor with our communication bus. Further work is
253 carried on in optimizing the hardware and software layers, with the goal of bringing up a first internet
254 of power enabled distributed control device.

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