A Frequency Compensation Scheme for LDO Voltage Regulators

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***Abstract*—A stable low dropout (LDO) voltage regulator topology for low equivalent series resistance (ESR) capacitive loads is presented. The proposed scheme generates a zero internally instead of relying on the zero generated by the load capacitor and its ESR combination for stability. It is demonstrated that this scheme realizes robust frequency compensation, facilitates the use of multilayer ceramic capacitors for the load of LDO regulators, and improves transient response and noise performance. Test results from a prototype fabricated in AMI 0.5-μm CMOS technology provide the most important parameters of the regulator viz., ground current, load regulation, line regulation, output noise, and start-up time.**

***Index Terms*—Frequency compensation, linear regulators, low dropout (LDO) regulator, LDO stability, power management.**

I. Introduction

POWER management is a very important issue in portable electronic applications. The need for multiple on-chip voltage levels makes voltage regulators a critical part of an electronic system design. Portable electronic devices like cell phones require very efficient power management to increase the battery life [1] whereas high-speed microprocessors need stable voltages that can supply fast varying currents on the order of few amperes [1], [2]. Low supply voltage noise is also an important requirement for noise sensitive RF circuits that are integral parts of all portable electronic devices.

The choice of a voltage regulator for a given application offers numerous design tradeoff considerations. While switch mode regulators provide efficiencies that can reach more than 90% in many practical realizations, they are costly in terms of silicon area, and the magnetic elements are bulky and cause electromagnetic interference (EMI). Moreover, the output voltage ripple and output noise of switching regulators might not be acceptable for several applications such as critical RF circuits. On the other hand, linear regulators have very small output voltage ripple, are compact, have low output noise, and are stable with varying loads. However, linear regulators have lower efficiency that depends on the dropout voltage, which is defined as voltage difference between unregulated supply voltage and regulated output voltage. In many applications, a switching regulator is cascaded with a linear regulator to reduce the voltage ripple and improve the stability of the overall system [3], [5].

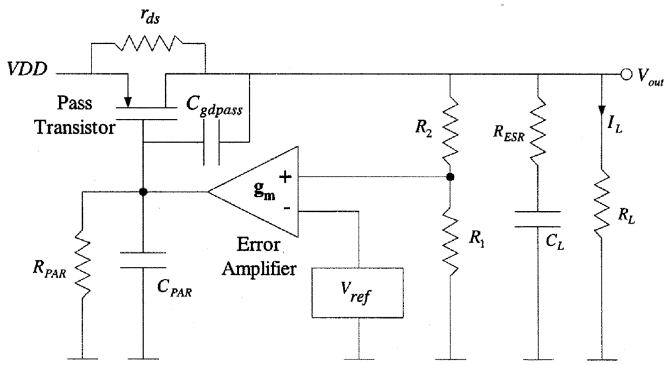

Fig. 1. Typical LDO voltage regulator.

The minimum permissible dropout voltage of a linear regulator defines the maximum achievable efficiency. The emphasis on efficiency has made low dropout (LDO) regulators the most popular class of linear regulators. But this increase in efficiency is achieved at the cost of a compromise in stability of the regulator. LDO regulators have high output impedance; this impedance, along with the load capacitance, creates a low frequency pole and decreases the overall phase margin. This paper gives an overview of stability problems in LDO voltage regulators, reviews some of the solutions that are being used to overcome this problem, and presents a modified LDO voltage regulator topology. Although the compensating circuit is very simple, the proposed topology successfully overcomes the problem of stability without significantly increasing the power consumption or die area. Both transient response and noise performances are also improved. Transistor level implementation of the design is realized in 0.5-μm digital CMOS process, fabricated through the MOSIS service, to demonstrate the feasibility of the proposed solution.

II. Stability of LDO Regulators

N-P-N regulators, the most widely used linear regulators prior to the popularity of LDO regulators, are stable for all loading conditions and do not require any capacitor at the output for stability purposes. The stability is an inherent property of these regulators due to the fact that the power transistor at the output stage (called as pass transistor) is an n-p-n transistor in emitter follower configuration, thus offering low output impedance across wide range of load currents. The *RC* time constant at the output is small due to the low output impedance. Unfortunately, in a LDO regulator (Fig. 1), a source follower cannot be used as the

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output stage since its gate requires higher output voltage from the previous stage, effectively increasing the voltage overhead.

The output node of an LDO regulator is typically the drain of a pMOS power transistor and the dropout voltage required in this configuration is the overdrive voltage required to keep the pMOS transistor in saturation region. The price we pay for the reduction in dropout voltage (compared to n-p-n regulators) is the potential instability of the regulator. The impedance seen from the drain of the pass transistor is high and is inversely proportional to load current. Hence, the pole at the drain of the pass transistor is heavily dependent on the load condition. The load current can range from few microamperes to hundreds of milliamperes.

A closer look of a typical LDO voltage regulator (Fig. 1) reveals the fact that there are two low-frequency poles that need to be taken into consideration in evaluating the frequency response of the LDO's closed-loop transfer function. One of the poles lies at the output of the regulator and the other one at the gate of the pass transistor. Owing to the large size of the pass transistor (6000 μm/1 μm in the design presented in this paper) and therefore, its huge input capacitance together with the high output impedance of the error amplifier, the pole at its gate is located at low frequencies. There are, at least, two additional parasitic poles present in the LDO regulator. The third pole is lumped to the noninverting terminal of the error amplifier as a result of the input stage parasitic capacitors. The error amplifier contributes with an internal pole since two-stage or cascode amplifiers are used to increase the amplifier's dc gain. The system is therefore potentially unstable. A solution to this problem is to introduce a zero that compensates the phase contribution of one pole to guarantee phase margin better than 45 degrees. In a conventional LDO voltage regulator, the electrostatic resistance of the output capacitor generates this zero [4]–[6]. The series combination of the output capacitor and its equivalent series resistance (ESR) generates a zero and gives the required stability. If the third and fourth poles are located beyond the unity gain frequency, the open-loop gain transfer function of a typical LDO regulator (Fig. 1) is given by the following expression:

$$H(s) \cong \frac{A_0\left(1+\frac{s}{\omega_{\rm ESR}}\right)}{\left(1+\frac{s}{\omega_{\rm P1}}\right)\left(1+\frac{s}{\omega_{\rm P2}}\right)} \tag{1}$$

where A_0 is the dc open-loop gain, and it is the product of dc gains of the error amplifier, pass transistor and feedback loop as follows:

$$A_0 = \left(g_m g_{m\ \rm pass} R_{\rm par}\left(r_{ds}||\left(R_1+R_2\right)||R_L\right)\right)\left(\frac{R_1}{R_1+R_2}\right). \tag{2}$$

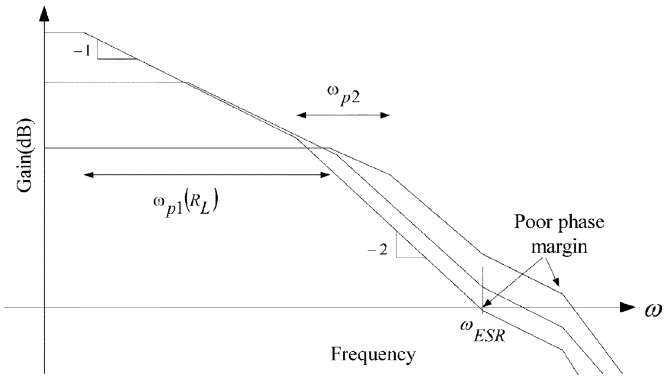


Fig. 2. Frequency response of a typical LDO regulator for different loads. For large current loads, R_L decreases and the pole's frequency increases.

If the gate-drain capacitance of the pass transistor ($C_{gd\ \rm pass}$) is small, the zero and poles are located at the following frequencies:

$$\omega_{\rm ESR} = \frac{1}{R_{\rm ESR}C_L} \tag{3}$$

$$\omega_{\rm P1} \approx \frac{1}{\left(r_{ds}||\left(R_1+R_2\right)||R_L\right)C_L} \tag{4}$$

$$\omega_{\rm P2} \cong \frac{1}{R_{\rm par}\left(C_{\rm par}+g_{m\ \rm pass}\left(r_{ds}||\left(R_1+R_2\right)||R_L\right)C_{gd\ \rm pass}\right)}. \tag{5}$$

The location of the zero $\omega_{\rm ESR}$ should be such that stability is assured for all loads. Fig. 2 shows the typical loop magnitude response of the regulator for various loads. The worst case for phase margin occurs at very high load impedances (small load currents) if the zero is located at very high frequencies. Also, for small load impedances (high load currents) the closed-loop unity gain frequency increases and the high-frequency parasitic poles become more important. Thus, there is no simple rule to decide the exact location of the zero. The design should be optimized depending on process technology, performance requirements and the range of operating conditions of the particular regulator. The fundamental requirements for stability are: 1) the zero must be located below the loop's unity gain frequency, and 2) all high-frequency poles must be located at least three times the unity gain frequency.

A more detailed analysis of the regulator's loop gain shows that a right-hand side zero ($\sim g_{m\ \rm pass}/C_{gd\ \rm pass}$) is also present; this zero however can easily be placed at very high frequencies. The Miller capacitor $C_{gd\ \rm pass}$ links the two dominant poles; it can be shown that the two dominant poles are located at the position shown by (6), at the bottom of the page. In this expression, we assume that $C_L \gg C_{gd\ \rm pass}$ and $R_{\rm LT} = r_{ds}||R_L||(R_1+R_2)$.

$$\omega_{\rm P1,2} \cong \frac{1}{2}\left(\frac{1}{R_{\rm PAR}\left(C_{\rm PAR}+C_{gd\ \rm pass}\right)}+\frac{1}{R_{\rm LT}C_L}+\frac{g_{m\ \rm pass}C_{gd\ \rm pass}}{\left(C_{\rm PAR}+C_{gd\ \rm pass}\right)C_L}\right) * \left(1\pm\sqrt{1-4\frac{\frac{1}{R_{\rm PAR}R_{\rm LT}\left(C_{\rm PAR}+C_{gd\ \rm pass}\right)C_L}}{\left(\left(\frac{1}{R_{\rm PAR}\left(C_{\rm PAR}+C_{gd\ \rm pass}\right)}+\frac{1}{R_{\rm LT}C_L}\right)+\frac{g_{m\ \rm pass}C_{gd\ \rm pass}}{\left(C_{\rm PAR}+C_{gd\ \rm pass}\right)C_L}\right)^2}}\right) \tag{6}$$

Notice in (6) that the term lumped to $g_{m\ \mathrm{pass}}$ ensures that the poles are always real. It is interesting to notice that Miller phase compensation schemes, typically used in linear opamp applications, do not improve the performance of the system since the dominant pole is located at the LDO output ($\sim$ 100 Hz–10 kHz) while the pole lumped to the gate of the pass transistor is around 20–50 kHz. The load capacitor is in the order of microfarads; hence, Miller on-chip capacitors have little effect on the first pole. The frequency of the second pole, located at the output of the error amplifier, reduces for large R_{LT} since the gain of the second stage, $g_{m\ \mathrm{pass}}R_{\mathrm{LT}}$, increases hence $C_{gd\ \mathrm{pass}}$ increases the effective load capacitance at the output of the error amplifier reducing the loop bandwidth.

The conventional phase compensation scheme that relies on the ESR compensation has several drawbacks in this aspect. The ESR of a capacitor is not properly specified in many cases and varies with temperature. The high-frequency bypass capacitors placed in parallel with the output capacitor form a pole with the ESR of the output capacitor further decreasing the phase margin. Moreover, the user is permitted to use ESR usually in the range of 0.05–10 Ω [4]. The use of ceramic capacitors that typically have ESR values less then 0.05 Ω makes the printed circuit board (PCB) design compact. Multilayer ceramic capacitors (MLCCs) of the order of few microfarads (Z5U class) are cheaper compared to tantalum alternative. However, most LDO voltage regulators oscillate with ceramic capacitor loads, as ESR value is less than the minimum required for generating the proper zero. On the other hand, the ESR compensation, as discussed in the next sections, increases the overshoot drastically if large resistors are used.

The problem of stability due to varying zero location can be overcome in several ways. The solution that uses a charge pump voltage booster [5] generates a voltage higher than the supply voltage and the error amplifier utilizes that voltage for driving a pass transistor in emitter (or source) coupled configuration. This configuration provides a low-output impedance, and therefore, isolates the output capacitor. The disadvantage of this circuit is the additional circuitry needed for the charge pump operation and the accompanying disadvantages in power consumption and noise performance. Also, due to higher voltages generated, this solution might not be well suited for advanced technologies. Another proposed solution to this problem is to use pole-splitting techniques (with the Miller capacitor across the gate and drain of the pass transistor) to have a single dominant pole at any load [6]–[9]; the Miller capacitor must be huge to be able to push the LDO output pole beyond the unity gain frequency. Also, the Miller capacitor, along with the C_{gs} of pMOS pass transistor, provides a direct path for the power supply spurs to reach the output. Therefore, the circuit has to be modified to have an extra buffer stage and this modification introduces additional parasitic poles. It will be explained in the following sections that an error amplifier with a buffer stage cannot effectively turn off the pass transistor during load transients. The topology presented in [10] creates the zero by using feedforward techniques but still Miller techniques are employed. A common-drawback of Miller compensation is that the pole of the first stage is pushed to low frequencies while the pole at the LDO output goes to higher frequencies. This approach is not effective for LDOs because the extremely large variations of the load impedance ($\sim$ 25Ω–2.5 kΩ) and the extremely large output capacitance; Miller compensation reduces both loop bandwidth and slew rate, and more power and area are needed.

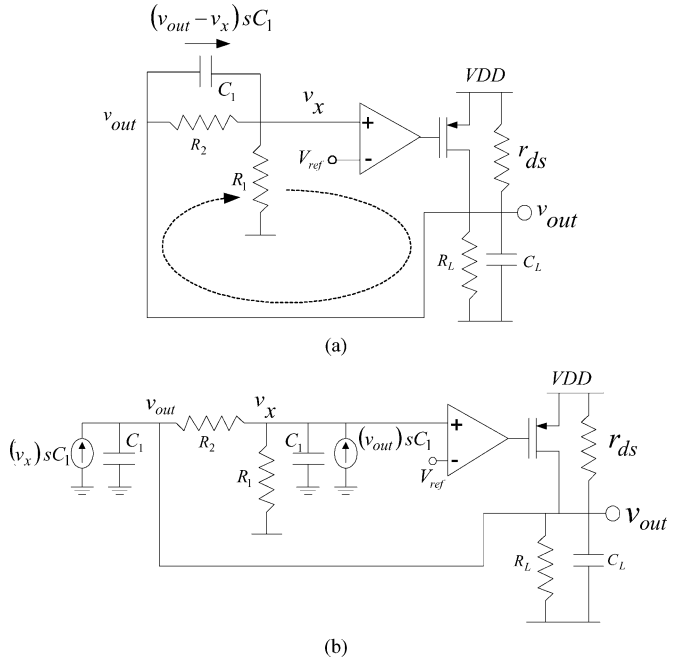


Fig. 3. (a) High-frequency bypass path in the feedback loop of LDO regulator. (b) Equivalent representation.

III. Capacitive Feedback for Frequency Compensation

The basic idea behind the capacitive feedback is to introduce a left hand plane zero in the feedback loop that would replace the zero generated by ESR of the output capacitor. We would then have the advantages of precisely controlling the zero location and minimize the overshoots. Prior art using the idea of capacitive feedback and internal zero compensation can be found in [11]–[13]. In [11], the goal was reached by adding a pole–zero pair with zero at lower frequency than the pole. This pole–zero pair improves the phase margin, but, a drastic improvement in phase margin can be obtained by adding only a zero. [12] presents a solution in which an internal zero is added by using a series resistor and capacitor combination connected to the output of error amplifier. In this solution, the resistor and capacitor pair would consume large silicon area as the zero should occur at very low frequencies to achieve the desired compensation. The capacitor added to generate the zero also reduces the frequency of the pole at the output of the error amplifier. The proposed method starts with the addition of a pole–zero pair as in [11] and proceeds toward eliminating the pole from the pole–zero pair.

To introduce capacitive feedback, a capacitor can be added to the original LDO configuration, [Fig. 3(a)] to provide a high-frequency bypass path for the loop gain. This capacitor produces a pole–zero pair in the open-loop transfer function as follows:

$$H(s)=\frac{A_0\left(1+\frac{s}{\omega_{Z1}}\right)}{\left(1+\frac{s}{\omega_{\mathrm{P1}}}\right)\left(1+\frac{s}{\omega_{\mathrm{P2}}}\right)\left(1+\frac{s}{\omega_{\mathrm{P3}}}\right)}. \tag{7}$$

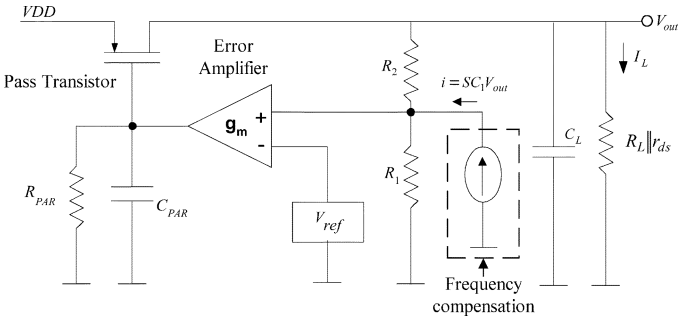


Fig. 4. LDO voltage regulator topology with proposed frequency compensation.

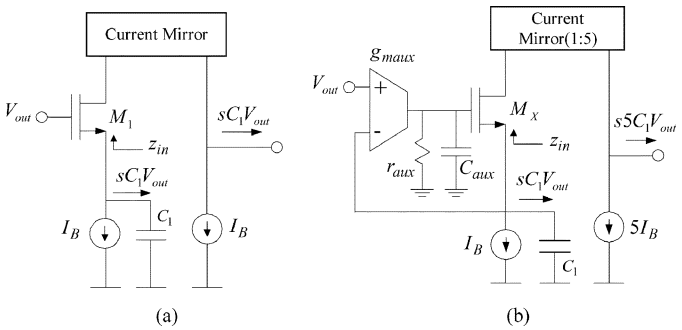


Fig. 5. Simplest realization of frequency dependent VCCS. (a) Simplest realization and (b) transconductance gain enhanced structure.

A_0, $\omega_{\rm P1}$, and $\omega_{\rm P2}$ are defined in (2), (4), and (5). ω_{Z1} and $\omega_{\rm P3}$ are given by

$$\omega_{Z1} = \frac{1}{R_2 C_1} \tag{8}$$

$$\omega_{\rm P3} = \frac{1 + \frac{R_2}{R_1}}{R_2 C_1}. \tag{9}$$

Although C_1 introduces the required zero, $\omega_{\rm P3}$ is not far away from the zero since R_2/R_1 is around 1.33. The topology has to be modified so as to eliminate $\omega_{\rm P3}$ without affecting the zero. Fig. 3(b) shows how the capacitor is split into two frequency-dependent voltage-controlled current sources (VCCS) and grounded capacitors. The capacitor C_1 and the VCCS connected to $v_{\rm out}$ do not significantly alter the voltage at that node since C_L is of several microfarads, whereas C_1 is on the order of few picofarads. It should also be noted that the capacitor connected to v_x is responsible for the additional pole $\omega_{\rm P3}$; therefore it is eliminated to arrive to the final configuration of Fig. 4. This configuration generates the required zero; the LDO becomes a two-loop system. The VCCS is a differentiator that increases the loop gain at high frequencies.

The loop gain transfer function of the regulator with this configuration has one zero and two poles given by

$$\omega_{Z1} = \frac{1}{R_2 C_1} \tag{10}$$

$$\omega_{\rm P1} = \frac{1}{(r_{ds} || R_L || (R_1 + R_2)) \left(C_L - \frac{C_1}{\beta} \right)} \tag{11}$$

where $\beta = 1 + R_2/R_1$ and $\omega_{\rm P2}$ is given by (4). The loop transfer function of the proposed regulator is similar to that of conventional regulator except that the product of C_1 and feedback resistor R_2 generates the left half plane zero instead of the output capacitor's ESR. It should be noted that the location of the pole $\omega_{\rm P1}$ is almost not altered by C_1 as it is primarily dependent on C_L. The designer can accurately control the frequency of the zero. Other advantages will be evident in the next sections. It would be of some interest to note that the proposed compensation scheme works only with low ESR capacitors as co-existence of VCCS generated zero and ESR generated zero at low frequencies might make loop gain undesirably high.

A. Design Considerations for the VCCS

The transistor-level design challenge lies in realizing the frequency dependent VCCS with minimum die area and minimum power consumption while retaining the VCCS characteristics up to crossover frequency of the loop transfer function. The simplest realization of this circuit is shown in Fig. 5(a). The bias current I_B can be selected to meet the objective of minimal standby current; the limit is however determined by the frequency of its parasitic pole determined by g_{m1}/C_1. The overall small-signal transconductance is given by (12)

$$\frac{i_{\rm out}}{v_{\rm out}} = \frac{sC_1}{1 + \frac{C_1}{g_{m1}} s}. \tag{12}$$

Hand calculations and simulated results show us that the parasitic pole occurs at around 400 KHz for $I_B = 0.5$ μA and $C_1 = 5$ pf. The current mirror introduces another parasitic pole but it is located at higher frequencies because of the small parasitic capacitors. To push the parasitic pole beyond 1 MHz for $C_1 = 25$ pf (required for the proper location of the zero), we need to improve the effective g_{m1}. Increasing the small-signal transconductance by increasing the bias current drastically increases the power consumption (g_m scales proportional to the square root of bias current). Therefore, alternate G_m enhancement techniques should be explored. The impedance $z_{\rm in}$ seen from the source of M1 is roughly equal to $1/g_{m1}$. Fig. 5(b) modifies the basic topology using an operational transconductance amplifier (OTA) in feedback for G_m enhancement. The effective transconductance G_m is given by the product of the voltage gain of the auxiliary OTA and the small-signal transconductance of M_x ($G_m = A_{\rm VOTA}\ g_{\rm mx}$). The impedance seen from the source of M_x is given by the following:

$$z_{\rm in} \cong \left(\frac{1}{g_{m\,\rm aux} g_{mx} r_{\rm aux}} \right) \left(\frac{1 + s(r_{\rm aux} C_{\rm aux})}{1 + \frac{C_{\rm aux}}{g_{m\,\rm aux}} s} \right) \tag{13}$$

where $g_{m\,\rm aux}$ is the small-signal transconductance of the auxiliary amplifier. The input impedance is very small at low frequencies, collecting all current generated by C_1. It is mandatory to reduce as much as possible $r_{\rm aux} C_{\rm aux}$ to extend the frequency capabilities of the circuit. At high frequencies, the input impedance increases up to $1/g_{mx}$; if $|z_{\rm in}| \ll 1/\omega C_1$ then, the circuit can properly drive C_1.

The transistor realization is shown in Fig. 6. The circuit consists of three parts. The first stage acts as a level-shifting buffer needed to down-shift the dc level which can be very close to the supply voltage due to LDO characteristics of the regulator. The next stage is M_x with G_m enhancing OTA in feedback. The third stage consists of a 1:5 current mirror and bias sources

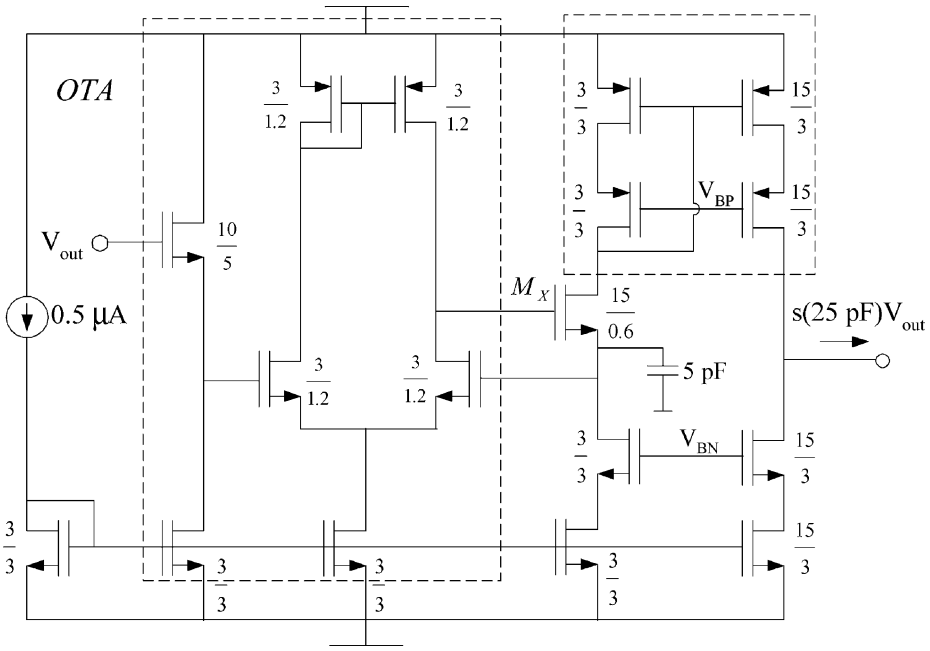


Fig. 6. Transistor level implementation of VCCS with G_m enhancement.

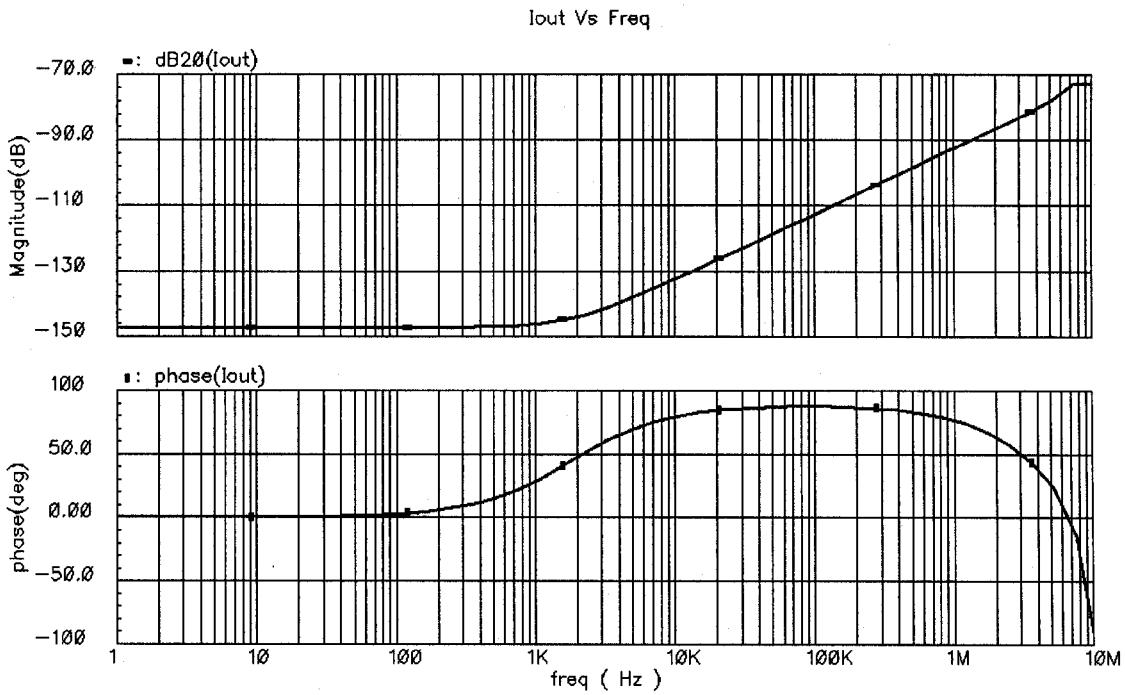


Fig. 7. Frequency response of the circuit shown in Fig. 6.

that together perform the function of pumping the ac current through output. We can take advantage of a multiplication factor in the current mirror to increase the effective capacitance from 5 to 25 pF. Cascode current mirror and cascode bias current sources (bias by proper dc voltages $V_{\rm BP}$ and $V_{\rm BN}$) are used such that offset current is not significant enough to upset the dc output voltage of the regulator. Transistor dimensions are such that $g_{m\ \rm aux}/C_{\rm aux}$ is beyond $2\pi\times$ 5 MHz. The total current consumed by this structure is 4 μA. The circuit simulation is plotted in Fig. 7. We notice that VCCS characteristics are retained up to a frequency of 5 MHz.

IV. System Level Design Considerations

The two other components of the LDO voltage regulator loop are the pass transistor and the error amplifier. The important design consideration for the pass transistor is the dropout voltage. Increasing the size of the pass transistor lowers the dropout voltage for a particular output current, but wider pass transistor introduces higher input capacitance making it difficult to meet stability and slew rate requirements. The design presented in this paper uses a pass transistor of 6000 μm/1 μm that gives a maximum output current of 100 mA with a dropout voltage of

0.5 V. Minimum length is not used as it makes the transistor output impedance unacceptably low at high load currents.

The error amplifier design demands careful attention to meet the required loop gain, transient response and stability. Ideal requirements of the error amplifier are: 1) high dc gain to ensure high loop gain (typically $> 60\,\mathrm{dB}$) for all loads; 2) low output impedance to keep the pole at the input of the pass transistor at high frequencies; 3) positive rail output to turn off pass transistor when the load turns off; and 4) internal poles at significantly higher frequencies compared to the cross over loop frequency. High output impedance of the error amplifier pushes the pole at the input of the pass transistor (ω_{P2}) to lower frequencies. ω_{P2} is pushed to higher frequencies by limiting the output impedance of the error amplifier; hence the use of a two-stage error amplifier is a must.

A. Load Regulation

Load regulation characteristics are not symmetrical for increase and decrease in load current. In the proposed circuit, when load current is increased instantaneously, the load capacitor supplies the extra current and the capacitor voltage drops. This drop in output voltage is sensed by the feedback circuit which in turn pulls down the gate of the pMOS pass transistor thus turning it on and supplying the output current needed by the capacitor and load impedance. Since the *compensating circuit is a differentiator*, it helps increasing the loop feedback for fast output variations. On the other hand, if ESR is used, the instantaneous current flows through the resistor increasing further the overshoots at the LDO output, especially if large ESR is used.

When the load current is decreased instantaneously, the extra current from the output of the pass transistor charges the output capacitor to a higher than nominal voltage. The feedback loop reacts by switching the error amplifier to positive saturation limit thereby turning off the pass transistor. The excess charge on the output capacitor is discharged through the feedback resistors; hence the discharge time is large because *R1* and *R2* are in the range of hundreds of kilo ohms. The positive saturation voltage of the error amplifier needs to be close to the supply voltage since we need to turn off the pass transistor, whose subthreshold current could be substantial owing to its large size. An error amplifier with nMOS output buffer stage does not have high positive saturation voltage. One of the solutions [8] is to use an nMOS buffer with a low V_t nMOS transistor available in some expensive processes. A simpler solution is achieved in the current design by eliminating the buffer stage; the amplifier structure is shown in Fig. 8. A two-stage amplifier is used in order to have enough voltage swing at the output. Minimum dimensions are used in most of the transistors in order to reduce the capacitance at the output of the first stage. The parasitic capacitors at the output of the first stage of error amplifier are in the range of 50 fF, leading to a parasitic pole around 5 MHz for the worst corner simulation. Since unity gain frequency of the loop gain is below 1 MHZ this parasitic pole does not affect the overall compensation scheme. The error amplifier dc gain is around 60 dB.

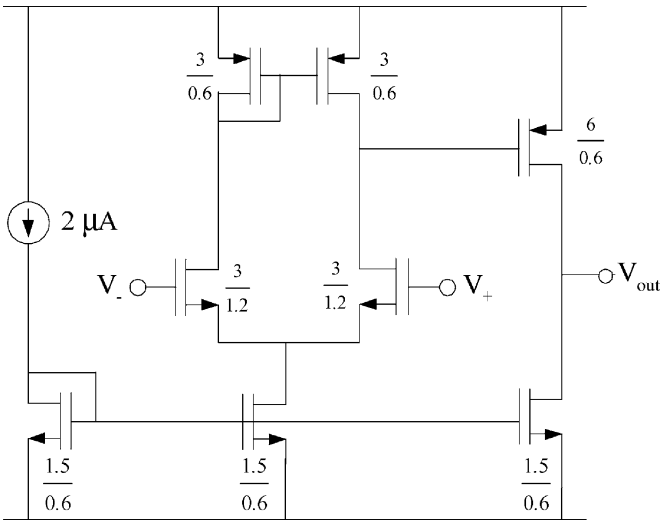


Fig. 8. Transistor level implementation of error amplifier.

B. Line Regulation

At low frequencies, line regulation (power supply rejection) of the regulator is determined by the loop dc gain. Since the introduction of VCCS does not change the loop gain, the power supply rejection of the regulator is not adversely affected by the proposed scheme. High-frequency line regulation is not degraded since VCCS does not add any significant parasitic capacitance from supply voltage to the output.

C. Start-Up Time

Start-up time of a regulator is important for the applications where power supervisory circuit frequently turns the regulator on and off. The proposed circuit has similar start-up time compared to the scheme with ESR generated zero, assuming that power supply is ramped up with a rise time of few microseconds. The speed limitation comes from the fact that the VCCS has an ideal behavior up to a few megahertz. For faster power-supply ramps, the start-up behavior could be slightly different for both cases depending upon high-frequency behavior of the VCCS.

D. Noise Response

Integrated output noise of the LDO regulator is the summation of the noise components due to reference voltage generator, error amplifier, pass transistor and the feedback resistors. In the proposed circuit, the output noise is reduced as noise gain from the reference voltage node (V_{ref}) to the output voltage node is reduced by VCCS zero. The zero is generated by additional circuitry (lumped to the VCCS) that is not in the direct path of the noise transfer function. Considering two cases where, in one case, the zero is generated by ESR and, in the other case, a zero of same frequency is generated by VCCS, the ratio of the noise transfer functions from reference voltage node (V_{ref}) to the output node are compared as follows:

$$\left|\frac{\dfrac{v_{\mathrm{out}}}{v_{\mathrm{ref\_proposed}}}}{\dfrac{v_{\mathrm{out}}}{v_{\mathrm{ref\_ESR}}}}\right| = \left|\frac{1}{1+\dfrac{s}{\omega_{\mathrm{ESR}}}}\right|. \tag{14}$$

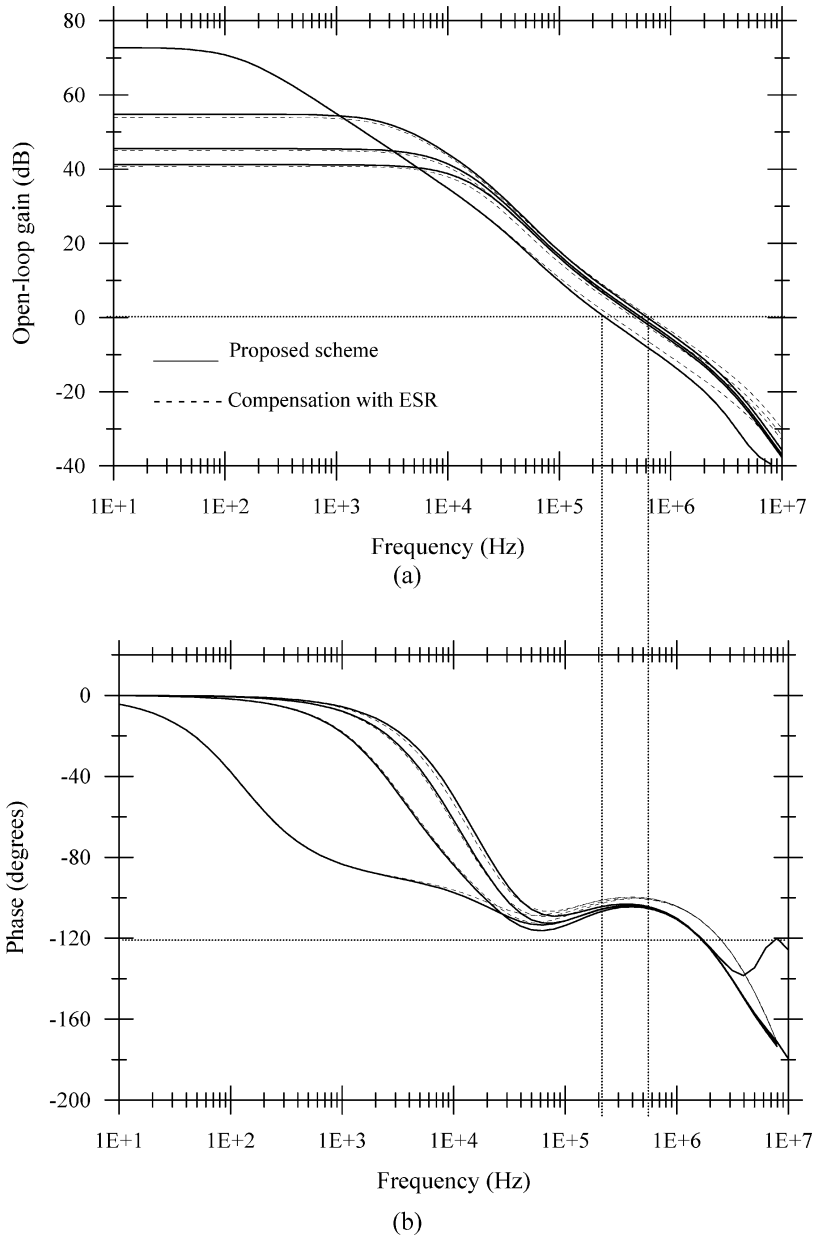


Fig. 9. LDO regulator open-loop gain. (a) Magnitude response. (b) Phase response. The load current is 1, 34, 67, and 100 mA.

The high-frequency noise due to the reference voltage generator, error amplifier, and pass transistor is therefore attenuated. Notice that the noise due to the VCCS is further attenuated by the intrinsic high-pass behavior of the topology, except for the noise contributions of the current mirrors.

V. Simulated and Experimental Results

The LDO regulator is tested for $R_1 = 120$ kΩ, $R_2 = 160$ kΩ, $V_{\rm ref} = 1.2$ V, $V_{\rm DD} = 3.3$ V and multilayer ceramic output capacitor $C_L = 2.2$ μF (Z5U class) with several bypass capacitors in the nF range placed in parallel to reduce high-frequency noise. The ESR of C_L is below 100 mΩ. The dc output voltage of the regulator is 2.8 V. The ground current consumed by the LDO regulator is 25 μA; 5 μA is consumed by the VCCS.

The LDO regulator was simulated and the open-loop gain results are shown in Fig. 9. The load current was changed from 100 mA ($R_L \sim 28$ Ω) to 1 mA ($R_L \sim 2800$ Ω) by using a nMOS transistor switch driven by an ideal voltage source; the setup is similar to the one used in [4]. The series resistance of ESR compensation is 2 Ω. The unity gain frequency is in the range of 250–650 kHz. The phase response is shown in Fig. 9(b); phase margin is better than 60° for all cases. Notice that the frequency response is quite similar for both topologies.

The integrated circuit micrograph of the regulator, designed in 0.5-μm CMOS technology and fabricated through the MOSIS educational program, is shown in Fig. 10. The pass transistor occupies most of the silicon area. C_1 and the VCCS do not contribute to a significant increase in the overall area. The regulator's output voltage as the load current is varied from 1 to 160 mA is shown in Fig. 11. For testing the LDO and external current mirror was used, and its output impedance is heavily dependent of the amount of current. Loop gain increases further

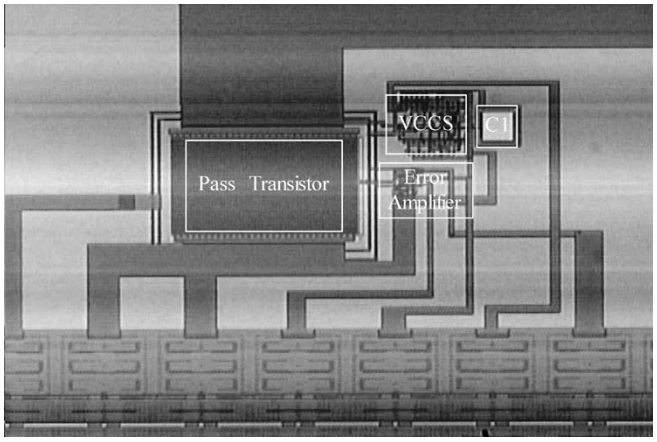


Fig. 10. Micrograph of the LDO voltage regulator.

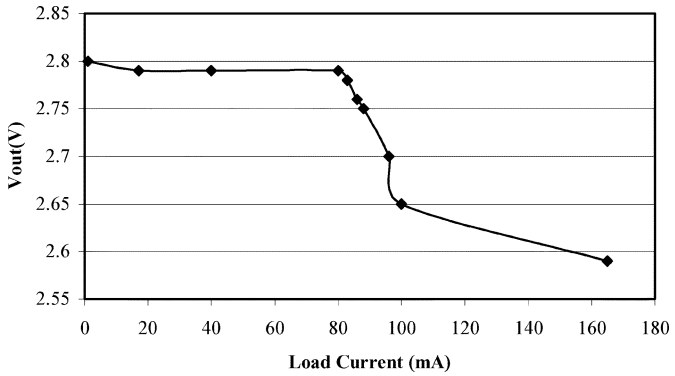


Fig. 11. Experimental LDO output voltage as function of the load current.

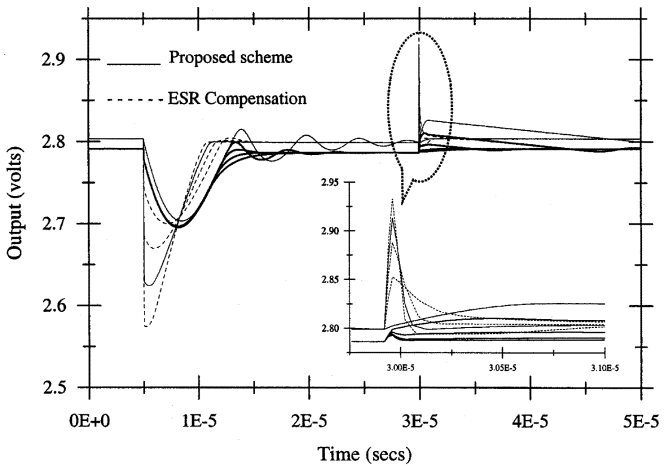


Fig. 12. LDO's transient response for load pulsed currents of 1 mA (0–5 μs and 30–50 μs) and 100 mA (5–30 μs). For the proposed scheme C_1 is 0.5, 2.5, 5, and 7.5 pF. For the ESR, the resistance is 0.1, 0.5, 1.5, and 2.5 Ω.

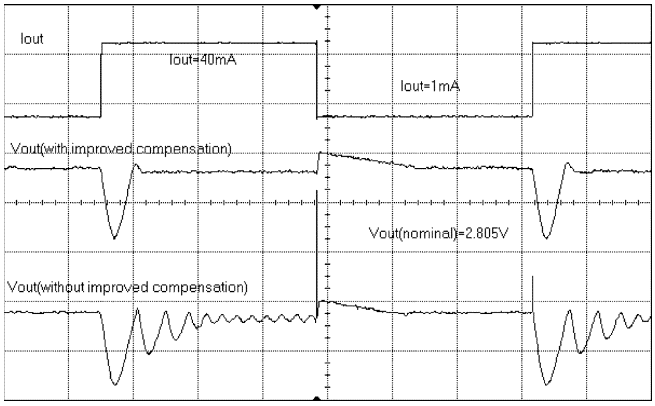


Fig. 13. Load regulation characteristics of the LDO regulator as output current is varied from 1 to 20 mA. (X-axis 50 μs/div, Y-axis 50 mV/div).

for very small currents (pass transistor go into subthreshold region and the output resistance of both pass transistor and load increase); error increases for large load currents leading to voltage deviations of around 10 mV for load currents greater than 20 mA. Another voltage drop in the output voltage occurs when the pass transistor goes into triode region thereby reducing the open-loop gain. The LDO's transient response for load pulsed currents of 1 mA and 100 mA has been extensively simulated. For the proposed scheme the compensating capacitor is varied from 0.5 to 7.5 pF (continuous curves). For the circuit using ESR, the resistance is varied in the range of 0.1–2.5 Ω (dashed curves); the results are shown in Fig. 12. For small ESR values, some parasitic oscillations are present due to the limited phase margin. For larger ESR, the oscillations disapear but the overshoot increases; clearly there is an unavoidable tradeoff between stability and overshoot. For the proposed scheme, the overshoot is little sensitive to the compensating capacitor. If the compensating capacitor is not large enough, some oscillations might appear in the transient response. Notice that the overshoot of the proposed scheme is less than 100 mV for all cases.

The load regulation has also been experimentally tested. To probe the effects of the proposed technique toward stability, load regulation characteristics are taken with and without VCCS enabled. The experimental results are presented in Fig. 13. As the load current is increased from 1 to 40 mA, the output voltage drops immediately since the output capacitor gets discharged. The feedback loop responds to this drop in output voltage and the circuit is supposed to adjust to new loading conditions with the output voltage coming back to the nominal voltage. However, since we are using a low ESR output capacitor, instability is introduced and causes sustained oscillations as seen in the lower trace of Fig. 13. These oscillations are suppressed by activating the compensation scheme as seen in the middle trace. The settling time of the circuit is not very fast when the load current drops from 40 to 1 mA; the output capacitor discharges through feedback resistors giving a simple *RC* circuit response.

The stability of the proposed scheme is fully tested by applying a pulsed signal ($\pm$20 mV) on top of the 1.2-V reference voltage as shown in the top trace of Fig. 14. The LDO with the phase compensation (middle trace) is stable showing that the phase margin is good enough. The test results are also taken without activating the frequency compensation scheme to prove that instability present in the circuit is removed when the compensation scheme is used (Fig. 14 bottom trace).

The response of the regulator circuit to voltage spikes in the power supply is shown in Fig. 15. Line regulation tends to be worse for small load currents since these conditions result in lower bandwidth, therefore the zero is closer to the loop unity gain frequency. The power-supply regulation for a load current

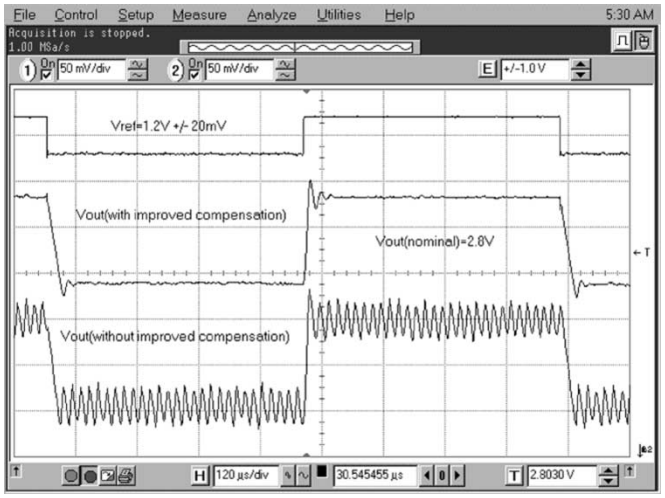


Fig. 14. Transient ouput voltage of the LDO regulator as $V_{\rm ref}$ is varied.

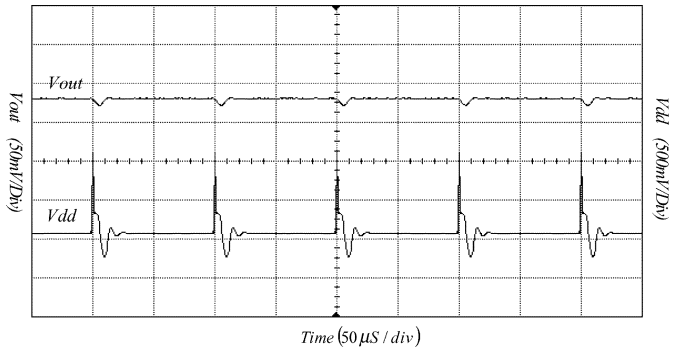


Fig. 15. Power-supply rejection of the regulator for 5-mA load current.

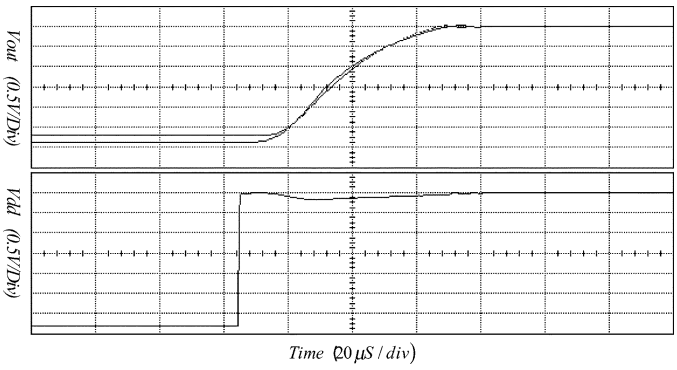
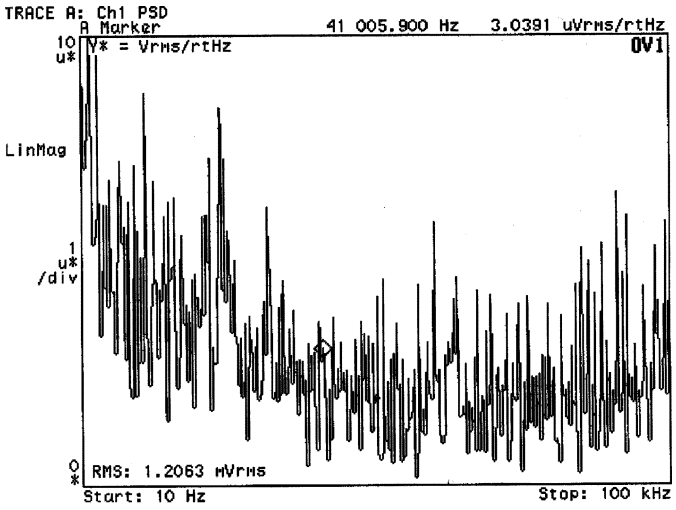
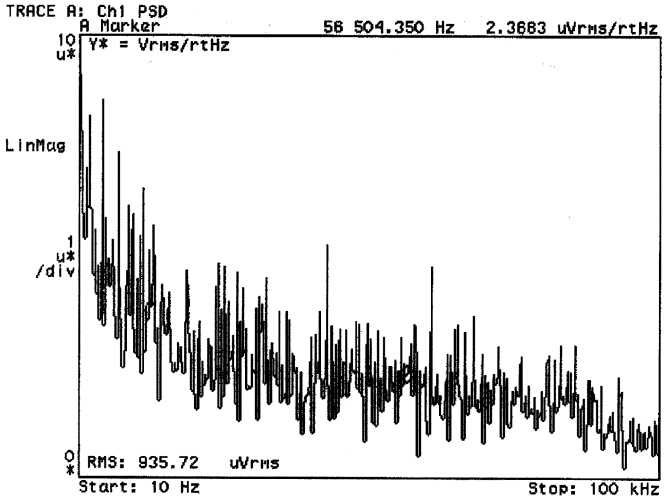


Fig. 16. Start-up time of the regulator for a load current of 5 mA.

of 5 mA is shown in Fig. 15. Supply spikes larger than 1 $V_{\rm p\text{-}p}$ produce output ripple below 100 $\rm mV_{p\text{-}p}$. The startup time of the regulator for load current of 5 mA is shown in Fig. 16. The two plots for $V_{\rm out}$ correspond to the regulator with ESR generated zero and the regulator with VCCS generated zero. The plots are similar as expected. Output power-spectral noise density (PSD) is shown for the case with ESR generated zero [Fig. 17(a)] and the case with VCCS generated zero [Fig. 17(b)]. The proposed topology is less noisy at high frequencies; the integrated noise (dc 100 kHz) has reduced from 1.2 mV from the ESR topology down to 936 μV.



(a)



(b)

Fig. 17. (a) Output spectral noise density of the regulator with ESR generated zero. (b) Output spectral noise density of the regulator with VCCS generated zero.

VI. Conclusion

This paper presented a novel LDO regulator topology aiming at more robust frequency compensation by getting rid of the dependence on ESR of the output capacitor. A detailed description of the implementation of the topology in CMOS technology is presented. Although the compensating scheme is very simple, the resulting structure provides better load regulation especially in turn-off transients. It is also proven that the topology does not consume significantly higher ground current nor die area compared to a conventional LDO regulator and does not adversely affect the power supply regulation or start-up time. The measured results show that output integrated noise is reduced compared to the conventional implementation ESR realization.

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