The current status and future prospects of SiC high voltage technology

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Abstract**—**This paper reviews the recent progress of SiC MOSFETs rated above 3.3kV. The static and dynamic performance of 3.3 and 6.5kV-rated MOSFETs will be evaluated and benchmarked against similarly rated state-of-the-art Si IGBTs. A numerical comparison between high voltage (15kV) SiC MOSFETs and IGBTs will also be provided. The paper will also attempt to comment on the future challenges facing high voltage (HV) devices in SiC technology.

I. INTRODUCTION

In recent years, Silicon Carbide (SiC) MOSFETs have provided a competitive alternative to the well-established Silicon (Si) IGBT technology in various low voltage applications. For the higher voltage ranges, in applications such as HVDC and FACTS, high voltage Drives, Traction Converters or high power Renewable Energy Conversion and Storage (see fig. 1), higher voltage MOSFETs (3.3kV to 6.5kV) have the potential to deliver similar improvements to those in the lower power ranges [1]. However, while HV SiC MOSFETs offer distinct benefits in terms of static and dynamic losses, their fault handling capability and long-term reliability are still somewhat short of the typical industry-required specifications. Moreover, the reliable operation of the body diode remains a question of concern.

This paper reviews the current status of 3.3 and 6.5kV-rated SiC MOSFETs. Both static and dynamic experimental results are presented. A numerical analysis of static losses for 15kV-rated SiC devices is also provided. The future prospects and challenges of high voltage devices in SiC technology are also briefly discussed.

II. HIGH VOLTAGE SIC MOSFETS

SiC MOSFETs have demonstrated that, in addition to drastically reduced switching losses, they can also offer low conduction losses for voltage ratings up to 10kV (fig. 2) [2]. In the lower voltage ranges (≤1.7kV), SiC MOSFETs specific on-resistance ($R_{on\text{-}sp}$) values are still quite far from the “ideal” unipolar limit, as here the inversion channel resistance is the dominant component of the static losses. For the ratings above 3.3kV, experimental $R_{on\text{-}sp}$ values sit much closer to the SiC unipolar limit, indicating that in these voltage regimes the static losses are dominated by the doping and thickness of the drift layer.

A. *Static behaviour*

The quality and stability of the SiC MOS interface have been one of the major factors limiting the overall performance of SiC MOSFETs. A commonly used process to improve the MOS interface behavior involves the use of N_xO annealing, which reduces the interface defect density (D_{it}) [3]. Fig. 3 shows the forward/backward sweep and frequency-dependent CV characteristics of an optimized SiC MOS capacitor. Compared to thermally grown SiO_2 films and N_2O annealed stacks, our developed deposited oxide process exhibits lower D_{it} values below $10^{12}cm^{-2}eV^{-1}$ (Fig. 4).

The output characteristics of a 3.3kV MOSFET with two different pitches, 14 and 26um, respectively, are shown in fig. 5, for V_{GS}=15V and T_j=125°C [4]. For benchmarking reasons, the output IV of Si IGBTs and BIGTs are plotted on the same figure [5]. As can be seen, at the I_{NOM} of 60A/cm^2, both MOSFET pitches provide lower static losses compared to the bipolar Si devices. For this design, at 125°C, both pitches deliver similar $R_{DS\text{-}on}$ values, as the JFET effect is stronger for p14. The MOSFET static behavior in the third quadrant is displayed in fig. 6. Reference curves for both Si PiN and BIGT diode are also shown. The body diode has a turn on threshold of -2.5V for negative V_{GS} values, but shows linear conduction for V_{GS}=15V. The high turn-on voltage of the MOSFET body diode makes it difficult to compete against the Si PiN in terms of static losses. The on-state drop seems to be independent of the pitch size, suggesting that the losses are controlled by the lifetime values in the epi layer.

Figure 7 shows the static characteristics of 6.5kV MOSFETs [6]. Several cell pitches are shown (p26, p14 and p12) and compared to a state of the art 6.5kV Si IGBT at T_j=125°C and V_{GS}=15V. The horizontal line indicates the rated current of 37.5A/cm^2 (I_{NOM}) of the IGBT. The SiC MOSFETs provide comparable (p26) or even higher (p14, p12) current densities compared to the Si IGBT. At the I_{NOM} values of the IGBT, the smaller pitch MOSFETs offer a substantial reduction in on state voltage (≈1V). The body diode characteristics, for different V_{GS} values, are shown in fig. 8. For reference, a Si PiN diode is also plotted. At the rated diode current of 75Acm^{-2}, the silicon diode provides the lowest voltage drop of 3.5V followed by p12 (3.8V), p14 (4.0V) and p26 (4.3V). A smaller cell pitch reduces the body diode on state by a 0.5V margin.

B. *Dynamic behaviour*

Surge current capability is an essential requirement in the specifications of the freewheeling diode. The surge event behavior of 4x 3.3kV MOSFETs connected in parallel is shown in fig. 9 (for V_{GS}=0V and V_{GS}=15V). A comparison with SiC JBS diodes (4x in parallel) and a Si diode is made on the same graph. As a pass criterion, each curve was measured twice and was not allowed to differ from the previous one. Compared to

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the Si diode (last pass not shown), the MOSFET body diode shows a positive temperature coefficient and has larger conduction losses. However, despite the inherent high built-in voltage and probably low plasma levels, the MOSFETs successfully demonstrate the required $10xI_{NOM}$.

The short-circuit waveforms, under nominal conditions of V_D=1800V and V_{GS}=15V, for 3.3kV MOSFETs with small and large pitches are pictured in fig. 10. The strong trade-off between static losses (high density of MOS cells) and short circuit capability is immediately evident, as designs with lower conduction losses (p14) cannot meet the required 10us industry standard. Optimizing the MOS cell density and adjusting the V_{th} values could help improving the aforementioned trade-off.

The use of the MOSFET body diode also offers benefits in terms of increased power density in a power module, as more chips would fit inside the module. The turn-off characteristics of a 3.3kV MOSFET body diode is analyzed in fig. 11. Compared to a SiC JBS diode, the body diode has a similarly fast response and only shows a moderate increase in the reverse peak current. Nevertheless, the reliability of HV SiC MOSFETs body diodes remains a concern and special buffers layers designs are needed to improve the V_F stability [7, 8].

The possibility of chip paralleling is a key aspect for achieving the high current levels required in high voltage applications. The turn-off characteristics 4x 6.5kV MOSFETs connected in parallel are indicated in fig. 12 at 125°C (V_D =3600V, I=40A; the inset shows the MOSFETs bonded onto a test substrate). Different dV/dt levels have been tested by changing the turn-off gate resistor. Although larger oscillations are observed for the faster switching case, the MOSFETs successfully turn-off the required I_{NOM} level.

Figure 13 depicts the short circuit waveforms of 4x 6.5kV MOSFETs connected in parallel, for a pitches p12 design, at Tj=125°C for V_D=3600V, V_{GS}=15V. The MOSFETs show a short circuit capability of about 5μs, with the saturation current reaching levels in excess of 600A. Assuming equal current sharing between the four chips, each MOSFET takes more than 150A, which is a remarkable performance for a relatively small $5x5mm^2$ device.

The Reverse Bias Safe Operating Area (RBSOA) capability of the 6.5kV MOSFETs mentioned above is plotted in fig. 14. The MOSFETs successfully turn-off 80A, with a DC-link voltage of 4.4kV, with no failures observed during the testing. This level of performance is similar to the one provided by the latest state of the art 6.5kV Si IGBTs [9].

III. FUTURE PROSPECTS OF SIC HV TECHNOLOGY

SiC unique material properties enable the possibility of designing very high voltage devices (>10kV) with acceptable losses [2, 10]. The simulated output IV of 15kV-rated MOSFETs and IGBTs are shown in fig. 15. A comparison to the series connection of 5x 3.3kV and 3x 6.5kV MOSFETs is made. The parallel connection of 2x 15kV MOSFETs is also indicated on the same graph.

A simplified summary of the devices shown in fig. 15 is presented in Table 1. While it is obviously difficult to identify a clear winner, the anticipated benefits of HV SiC devices in terms of reduced total losses as well as simplified topologies are evident [11]. However, challenges associated to the cost/Amp ratio, termination design, stable blocking performance, reliability and over-current capability still remain. Moreover, further advances in passivation materials and packaging technology would also be needed before HV SiC technology could be considered as a mature candidate in MW range applications.

IV. CONCLUSIONS

The performance of HV SiC MOSFETs has been reviewed with an emphasis on their dynamic and fault-condition operations. Using numerical results, an outlook into ultra HV SiC devices has also been presented. The benefits of ≥3.3kV SiC MOSFETs in terms of lower static and dynamic losses are substantial with a potentially strong impact on system performance. The road to market entry is, however, still paved with many challenges in terms of reliability, performance/cost ratio and, finally yet importantly, the continuous parallel developments made in Si technology.

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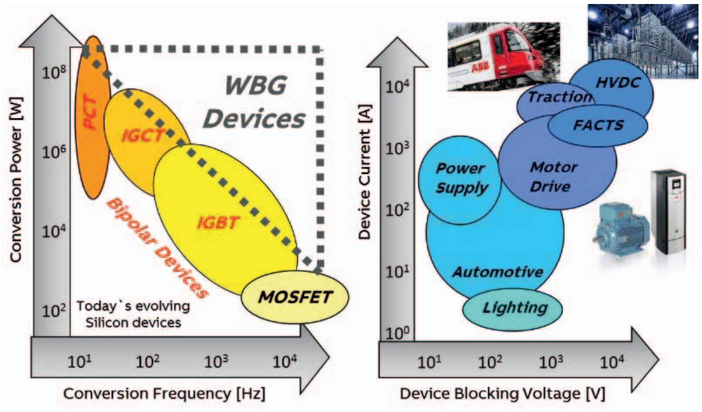

Fig. 1. SiC devices are targeting various applications in the high-power semiconductor market, which are currently served by a portfolio of silicon products.

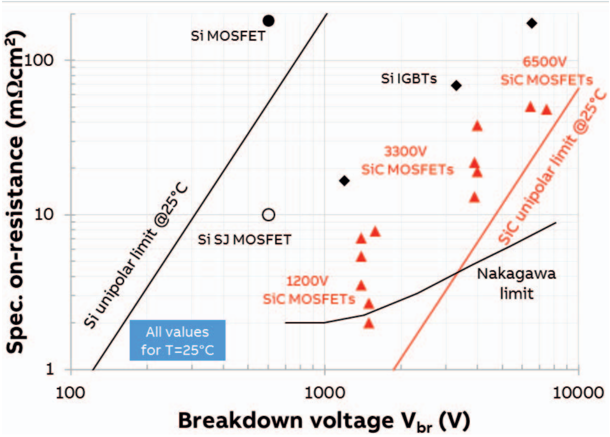

Fig. 2 Specific on-resistance of various Si and SiC devices at 25°C; the respective unipolar limits are also shown.

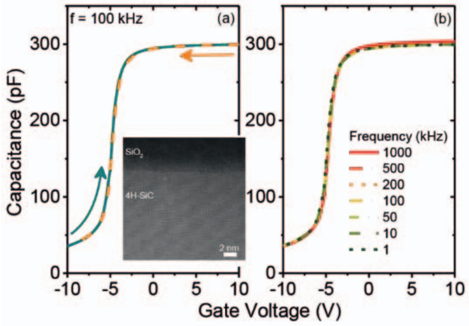

Fig. 3 Room-temperature C-V characteristics, The hysteresis and frequency dependent V_{FB}-shift are both negligible.

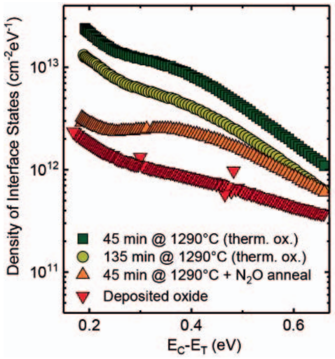

Fig. 4 D_{IT} distribution on MOS capacitors fabricated using different oxidation techniques.

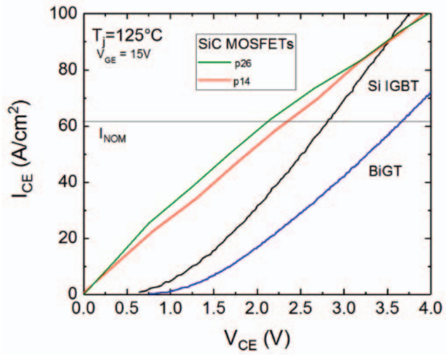

Fig. 5 Output IV of a 3.3kV MOSFET at 125C; reference Si IGBT and BIGT are also shown.

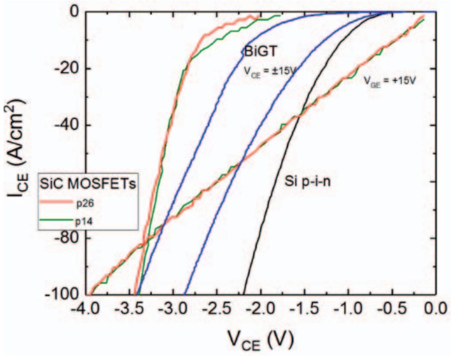

Fig. 6 Body diode characteritics of a 3.3kV MOSFET at 125C; reference Si PiN diode and BIGT diodes are also shown.

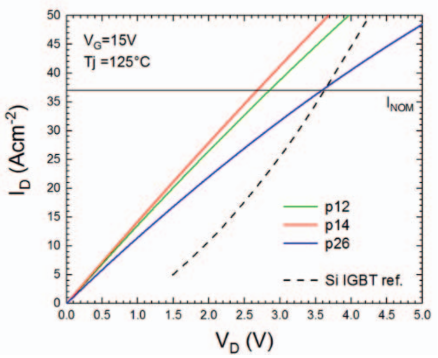

Fig. 7 Output IV of a 6.5kV MOSFET at 125C; a reference Si IGBT is also shown.

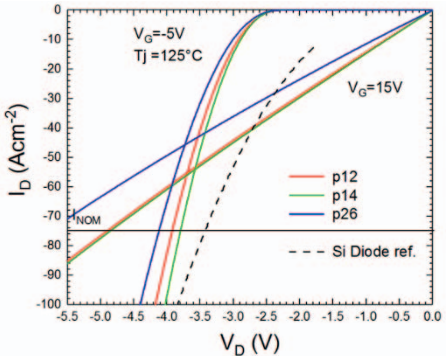

Fig. 8 Body diode characteristics of a 6.5kV MOSFET at 125C; a reference Si PiN diode is also shown.

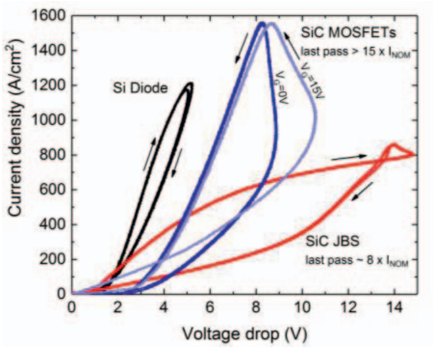

Fig. 9 Surge current density versus source - drain voltage drop of the body diode of 3.3kV SiC MOSFETs (4x in parallel), SiC JBS diodes (4x in parallel) and a Si diode.

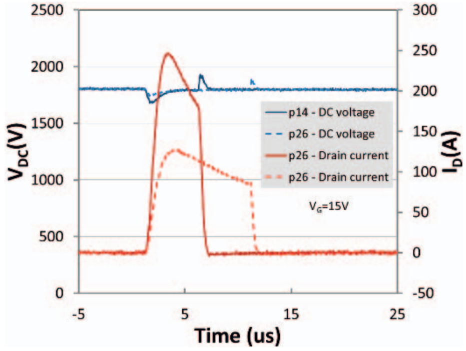

Fig. 10 Short circuit waveforms of p14 and p26 MOSFETs demonstrating 5µs and 10µs capability at 125°C, V_D=1800V and V_G=15V.

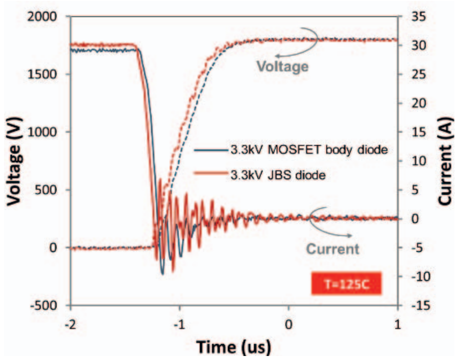

Fig. 11 Comparison between the turn-off curves of a 3.3kV MOSFET body diode and a JBS diode at 125°C; R_G= 33Ω; V_{DC}=1800V, I_D=30A.

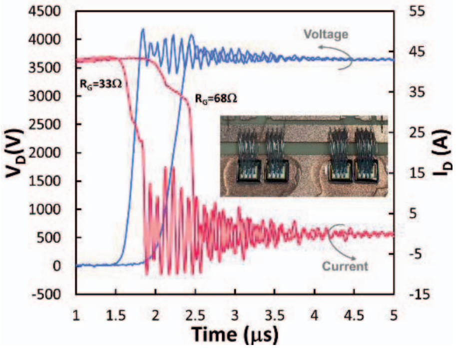

Fig. 12 Turn-off of 4x 6.5kV MOSFETs in parallel at 125°C, V_D =3600V, I_{NOM}=10A(per chip), R_G has been varied from 33Ω up to 68Ω.

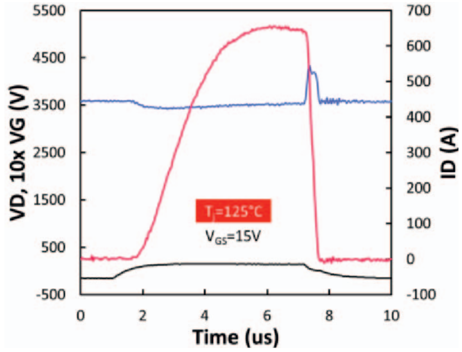

Fig. 13 Short circuit waveforms of 4x p12 MOSFETs in parallel at 125°C, V_D=3600V, V_{GS}=15V.

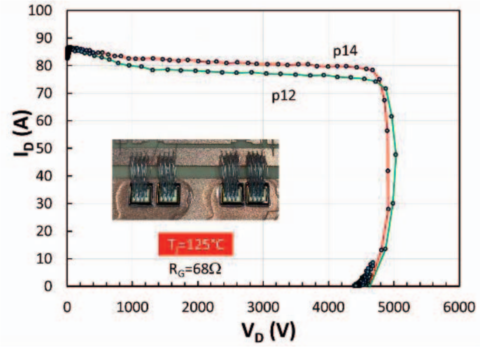

Fig. 14 Turn-off RBSOA for 4x 6.5kV MOSFETs in parallel with R_G=68Ω at 125°C; I_D=80A, V_D=4400V.

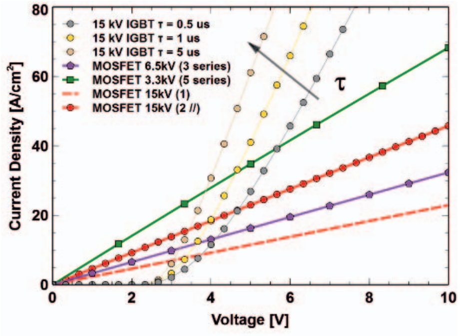

Fig. 15 Simulated output IV of 15kV-rated MOSFETs and IGBTs at 150°C; for comparison, series connections of 5x 3.3kV and 3x 6.5kV MOSFET are shown; the IV of 2x 15kV MOSFETs in parallel are also displayed.

Device type	**Current costs**	**Material issues**	**Main challenges**	**Expected benefits**
15kV SiC MOSFET	High	Quality of thick epi layer (≥100µm)	Static losses Large area devices-> yield issues Reliable body diode operation Packaging High dV/dt	Low switching losses (higher frequency operation) Body diode integrated Opportunity for simpler topologies
15kV SiC IGBT	Very high	Quality of thick epi layer (≥100µm) Lack of p+ substrates Low lifetime	Fabrication processes No body diode Negative T coefficient Packaging High dV/dt	High current ratings Enabler for ≥20kV applications Opportunity for simpler topologies
Series connection of lower voltage MOSFETs (e.g. 3.3-6.5kV)	Moderate	Quality of moderately thick epi layer (30 -60µm)	Voltage sharing Control Added complexity Moderate dV/dt	Lower cost Competitive static losses Improved redundancy Body diode integrated
Parallel connection of 15kV MOSFETs	High	Quality of thick epi layer (≥100µm)	Current sharing Reliable body diode operation Packaging High dV/dt	Lower static losses Low switching losses Body diode integrated Opportunity for simples topologies

Table 1. Summary of expected challenges and projected benefits of high voltage (15kV-rated) SiC devices