On-chip digital power supply control for system-on-chip applications

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Abstract
We present an on-chip, fully-digital, power-supply control system. The scheme consists of two independent control loops that regulate power supply variations due to semiconductor process spread, temperature, and chip's workload. Smart power-switches working as linear voltage regulators are used to adjust the local power supply. The smart power-switch allows us to keep the global power network unchanged. It offers an integrated standby mode and has a fast dynamic response, i.e. low transition times between voltage steps at the cost of the reduced power conversion efficiency when compared to complex DC-DC converters.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles – *advanced technologies, algorithms implemented in hardware, VLSI (very large scale integration).*

General Terms
Performance, Design.

Keywords
Adaptive voltage scaling, performance optimization, low power.

1. Introduction
Power efficient design technologies have become key drivers in modern integrated circuits targeting portable to high-performance application ranges. Besides technology scaling, one of the most effective ways to reduce power of active circuits is by operating at a lower power supply voltage (V_{DD}) [1]. Power supply voltage scaling can either be static or dynamic. Static supply scaling refers to the technique that assigns a minimum supply voltage to a circuit design such that it just meets its performance requirements [2]. Dynamic voltage scaling varies both operating frequency and supply voltage in response to workload demands. In this way, a processing unit always operates at the desired performance level while consuming the minimal amount of power. Despite the advancement in power supply control [3]-[6], solutions using off-chip DC-DC converters are not always suitable for island-based SoCs. The overhead of using off-chip converters can be significant when the power supplies for a large number of islands need to be individually controlled. Essentially, we see the following issues: i) each island may require its own DC-DC converter, ii) there is an overhead in the number of supply pins for the SoC, iii) DC-DC converters require additional external components, and iv) the global power grid distribution for many islands can be quite cumbersome. On the other hand, present on-chip solutions are based on analog implementations of linear power supply regulators [7], which are not easily portable to new CMOS technologies. In addition, they are more sensitive to digital supply noise and contain static biasing currents as compared to the case when the implementation is done in a digital fashion.

This paper describes a modular, adaptive V_{DD} control scheme enabling local power optimization in the voltage island SoC type of applications. In contrast to prior art, the scheme uses a fully digital control and makes use of on-chip components only. Our scheme offers the following advantages: 1) local adaptive control of power and energy per voltage island, 2) integrated power-switch gating in sleep mode, 3) simple digital control, and 4) low overhead in silicon area as compared to off-chip DC-DC converters.

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2. Proposed System Architecture
In our approach, voltage islands are performance rather than power managed, e.g. islands are expected to operate at a desired clock frequency with a minimum possible power supply voltage. In contrast to [7], the control of the power supply voltage is done in a fully digital fashion. As there are no DC-DC converters in this implementation, the proposed scheme consists of two negative feedback loops to regulate the power supply voltage. Our so-called μ-supply control loop takes care of the average supply voltage value, while the σ-supply loop regulates against circuit activity variations on a clock cycle basis. Figure 1 shows the proposed system architecture.

The μ-supply control loop consists of the μ-supply sensor, the μ-supply controller, and the power supply actuator (smart power-switch). The power supply voltage control is applied periodically to compensate global process variations and temperature drifts. The counter in the μ-supply sensor translates clock pulses to a count number N_{count} by counting the number of pulses for a predefined time ($\sim 1/f_{count}$). The μ-supply sensor monitors the actual silicon speed for a fixed period of time and compares it against the required speed characterized by the value of N_{ref}. Reference values are stored in a local look-up table such that the comparison is always done against design time values.

The μ-supply controller applies the appropriate control signals to the smart power-switch when there is a difference N_ε between the silicon and design performance values. The μ-reg and O-reg registers represent storage elements to control the power-

switch. The μ-supply control is applied to both the clock generating unit and the IP core.

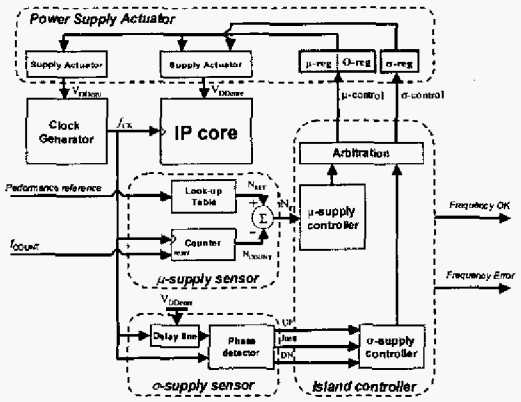

Figure 1. Proposed system architecture per island

The σ-supply control loop consists of the σ-supply sensor, the σ-supply controller, and the power supply actuator. Its purpose is to counterbalance changes in the average circuit activity of the IP. The σ-supply sensor detects a potential phase difference between the clock edge and its delayed version. The delay matches the critical path delay of the IP core. In this case, the *just* signal is triggered. Phase differences arise as the result of supply voltage fluctuations. The *up* signal is triggered when the delay is larger than one clock cycle indicating that the supply voltage has to be raised. In contrast, the *dn* signal is triggered when the delay is less than one clock cycle indicating that the supply voltage has to be lowered. The σ-supply controller sets the signals for the smart power-switch so that the power supply voltage is adjusted to compensate any phase differences. The σ-reg register represents a storage element as provided by the σ-supply controller. The σ-control is done on a few cycle-to-cycle basis of the clock frequency as provided by the clock generation unit (CGU). An arbitration unit is included to make sure that both the μ and σ loops are mutually exclusive to avoid racing between both loops.

2.1 Local Power Supply Conversion

We exploit the fact that modern SoCs use power switches for power gating purposes. Note that a power switch can be modeled simply as a resistor with zero or infinite resistance. Our actuator is a smart power switch with multiple discrete resistance values. This variable resistor is implemented as a parallel-connected segmented transistor in series with the circuit under control, see Figure 2. When the global power nets are shared among multiple islands, both header and footer transistors are required for signal integrity purposes. Capacitor C in Figure 2 represents the non-switching circuit and decoupling capacitance. The switch resistance value needs to be properly sized to cope with voltage fluctuations ΔV. The number of transistor segments and their geometry determine the resolution (step size) and the V_{DD} control range. Transistor segments always operate in cut-off and in linear region, thus the actuator acts as a linear resistor. Observe that the sleep mode is enabled when all segments are set to be non-conducting; in this case the resistor works as a power switch. The power switch can be (re)programmed at runtime to obtain a different degree of conduction.

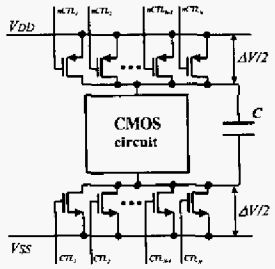

Figure 2. Proposed power supply actuator.

2.2 Smart Power-Switch Model

A first-order model of the power consumption of synchronous digital CMOS circuits can be expressed as

$$P_{circuit} = aC \cdot V_{DDC}{}^2 \cdot f_{CK} + V_{DDC} \cdot I_{leak} \quad (1)$$

where aC is the average switching circuit capacitance, V_{DDC} is the circuit's power supply voltage, f_{CK} is the operating frequency, and I_{leak} is the circuit's total off-state current. From (1) it is possible to derive an equivalent circuit resistance:

$$R_{circuit} = \frac{1}{aCf_{CK} + \frac{I_{leak}}{V_{DDC}}} \quad (2)$$

Since both header and footer transistors operate in the linear region, their resistance can be expressed as

$$R_{series} = \frac{K_p}{W_p} + \frac{K_n}{W_n} \quad (3)$$

where K_p and K_n are process-dependent constants, and W_p and W_n are the corresponding transistor channel widths. Using (2) and (3), the expressions for circuit, actuator and total power are:

$$P_{circuit} = \frac{(aCf_{CK} \cdot V_{DD} + I_{leak})(V_{DD} - I_{leak} R_{series})}{(1 + R_{series} \cdot aCf_{CK})^2} \quad (4)$$

$$P_{series} = \frac{R_{series}(aCf_{CK} \cdot V_{DD} + I_{leak})^2}{(1 + R_{series} \cdot aCf_{CK})^2} \quad (5)$$

$$P_{total} = \frac{(aCf_{CK} \cdot V_{DD} + I_{leak}) \cdot V_{DD}}{1 + R_{series} \cdot aCf_{CK}} \quad (6)$$

where V_{DD} is the constant global power supply voltage (V_{DD}=V_{DDC}+ΔV). By comparing (1) and (6) it can be observed that a scaling term is added to the denominator of (6), which represents to the impact of the resistor. The power conversion efficiency (PCE) of the proposed V_{DD} actuator can be determined by calculating the ratio of (4) and (6). PCE is linearly related with the circuit's power supply V_{DDC}.

The dynamic response of the proposed V_{DD} actuator can be determined by evaluating the voltage drop $\Delta V(t)$ across the actuator. The expression of $\Delta V(t)$ is

$$\Delta V(t) = \frac{R_{k+1} \cdot V_{DD}}{R_{k+1} + R_{circuit}} + \frac{(R_k - R_{k+1})R_{circuit} \cdot V_{DD}}{(R_k + R_{circuit})(R_{k+1} + R_{circuit})} e^{\frac{-t}{\tau}} \quad (7)$$

with $$\tau = \frac{R_{k+1} R_{circuit}}{R_{k+1} + R_{circuit}} C_{nsw}$$

where R_k and R_{k+1} are two consecutive resistance values of the V_{DD} actuator, $R_{circuit}$ is the equivalent circuit resistance, V_{DD} is the

constant global power supply voltage, τ is the transition time constant, and C_{nsw} is the non-switching circuit capacitance. Here, an instantaneous change from R_k to R_{k+1} and a constant operating frequency are assumed. From (7) one can determine voltage transition times, e.g. the time to change from one voltage level to another one.

These models have been applied to a standard-cell based CMOS circuit in a 0.13µm technology with an area of 1mm^2. Typical circuit parameters are: an average circuit activity of 0.3, a total circuit capacitance of 2nF, an operating frequency of 200MHz, a nominal power supply voltage of 1.2 volts, a threshold voltage of 0.35V, and an off-state leakage current of 27.3µA. Figure 3 shows the power consumption versus the power supply voltage of the circuit. The trend lines for circuit power, actuator power and total power are shown as calculated by expressions (4)-(6). At a nominal supply voltage, the circuit runs at a maximum operating frequency of 200MHz. The turn-over point at which the actuator power is larger than the circuit power is reached at about half the nominal supply voltage.

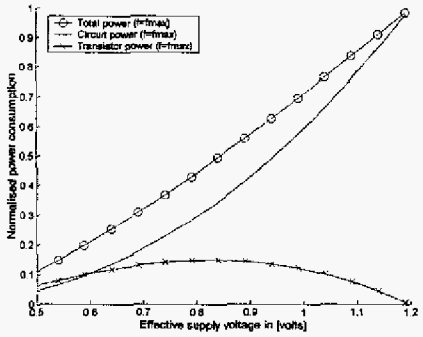

Figure 3. Normalized power versus effective supply voltage while operating at the maximum frequency

Expression (7) shows that the dominating voltage transition times are found when sweeping from a low to high resistance value of the V_{DD} actuator. This is the case when the power supply voltage changes from a higher to a lower value (e.g. from 1.2V to 0.6V). For the given circuit parameters, a steady-state voltage level (~0.6V) is reached after ~200ns. This shows that the proposed V_{DD} actuator enables voltage transitions in a time window of hundreds of nanoseconds as opposed to off-chip DC-DC converters that have transition times in the order of tens of microseconds.

3. Digital Power Supply Control

In our approach, islands operate at their peak performance when biased at their nominal power supply voltage. When the peak performance is not required, the clock frequency and the supply voltage are lowered to save power. The µ-supply control supports the selection of different operating frequencies by the performance scheduler, e.g. a power management unit (PMU). The supported frequencies are referred to as *major frequencies*, which are used for coarse-grained control of the operating frequency. Fine-grained frequency control is enabled through the so-called *minor frequencies*. These frequencies determine the frequency resolution and are used for tracking variations in global process parameters and operating conditions. The minor frequencies cannot be selected by the PMU; they can only be accessed by the µ-supply control loop. Every discrete operating frequency $f_{(i,j)}$ is mapped onto a corresponding resistance $R_{(i,j)}$ where i represents the K major frequencies and j represents the N minor frequencies per major frequency step. Figure 4 shows the relationship between operating frequency and power-switch resistance. The black and gray circles indicate the major and minor frequency-resistance pairs, respectively. These pairs are categorized in segment ranges. Each segment range contains a single major frequency and multiple minor frequencies.

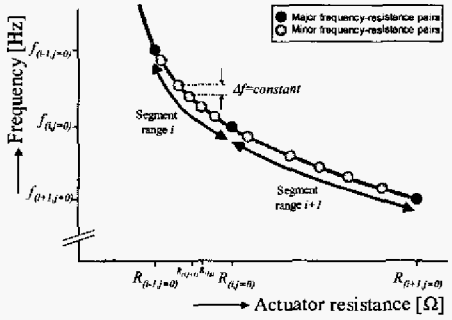

Figure 4. Operating frequency vs. actuator resistance.

3.1 µ-supply Control

A simple integral control is sufficient for the proposed V_{DD} control. Figure 5 shows the simplified block diagram of the µ-supply controller. The controller contains two counting units, namely the µ-counter and the O-counter, which provide the control signals to the transistor segments of the power-switch. Each combination of counter values results in a required discrete operating frequency $f_{(i,j)}$. As an example, $f_{(1,20)}$ is the 20th minor frequency in the 1st segment range that corresponds to µ-counter=1 and O-counter=20. At the edge of each segment range, the O-counter gives an overflow/underflow signal and the µ-counter is updated accordingly. The O-counter operates in a closed-loop and plays the role of an integrator. When the PMU requests a new major frequency, the µ-counter is updated with the new performance reference in an open-loop fashion.

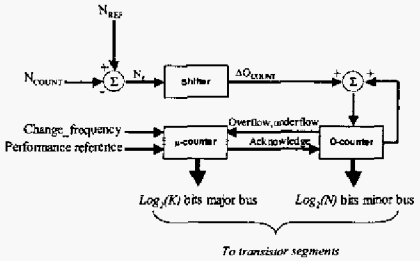

Figure 5. Block diagram of the µ-supply controller.

The controller's inputs in closed-loop operation are the reference performance (N_{ref}) and the measured performance (N_{count}). The error count N_e is converted to a value (ΔO_{count}) to update the O-counter. The frequency resolution Δf_{minor} is constrained to 2^X MHz, where X is an integer value. This constraint yields an implementation in which a simple shifter can be used to perform the division instead of a more complex multiplication unit. The outputs of the controller are binary-coded to reduce control complexity of the transistor segments. As a consequence, each segment range contains a segment decoder that ensures the desired resistance $R_{(i,j)}$ based on the outputs of the µ and O-counter. Each decoder contains two additional control bits, namely *standby* and *bypass*. The *standby* signal is used for power

gating control, and the *bypass* signal overrides the power supply control loops.

3.2 σ-supply Control

Given the properties of our power supply actuator, an increasing circuit activity will decrease the equivalent circuit resistance $R_{circuit}$ as can be observed in expression (2). Since the actuator acts as a voltage divider, ΔV will increase proportionally with the circuit activity, and thus, it will decrease the effective supply voltage of the IP core. The opposite happens for a decreasing circuit activity.

The σ-supply control adjusts the series resistance of the actuator to compensate for the supply voltage variation as a result of a change in circuit activity. A delay-locked-loop (DLL) has been used for this purpose as shown in section 2.1. The power-switch contains a number of transistor segments dedicated for the σ-supply control only. The number of segments depends on the circuit activity range and resolution one wants to cover. Their control signals are binary-coded and are controlled through a segment decoder as in case of μ-supply control.

4. Simulation Results

The adaptive V_{DD} control scheme has been implemented in a test-chip currently under fabrication. The design has been done according to the following specifications: Three performance references ranging from 100MHz up to 300MHz, a frequency resolution of 4MHz, a count frequency f_{COUNT} of 1MHz, 25 steps in circuit activity ranging from 0 up to 50%. Logic synthesis results show that up to ~950 logic gates and ~150 sequential cells are required consuming a silicon area of ~0.03mm^2 in total for 0.13μm CMOS. The area of the V_{DD} actuator has been estimated to be ~0.18mm^2 for a circuit of size ~0.86mm^2 containing 2K flip-flops and 48K logic gates.

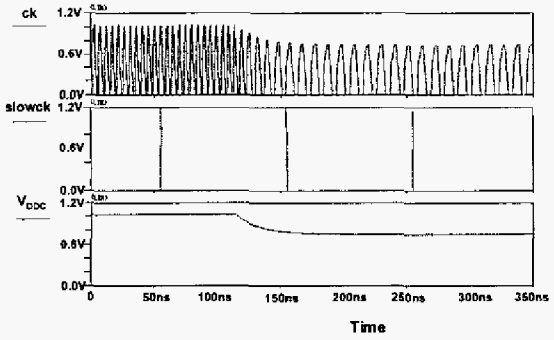

Figure 6. Circuit simulation of μ-supply control.

The μ-supply control loop has been verified using a transistor-level circuit simulator. A stripped version of the loop was used to reduce simulation time. This simplified version contains the μ-supply sensor, controller and one segment decoder. The circuit-under-control is a CGU and an IP core. The CGU generates an operating frequency of about 220MHz at nominal supply. The IP core has a total circuit capacitance of 2nF, a circuit activity of 0.3, and an additional decoupling capacitance of 6nF.

Figure 6 shows the results obtained from the circuit simulation of the μ-supply control for a particular 0.13μm CMOS circuit. In this case, the reference performance is changed from 200MHz to 100MHz. As a result, V_{DD} as well as frequency are reduced till the frequency meets a value of 100MHz.Figure 7 shows circuit simulation results of the σ-supply control demonstrating the tracking of the operating clock through V_{DD} control. When the *Just* signal becomes active, the desired V_{DD} has been reached such that reference and delayed clock are synchronized.

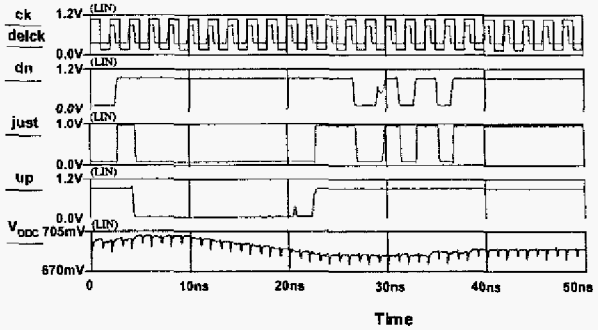

Figure 7. Circuit simulation of σ-supply control.

5. Conclusions

An on-chip fully-digital power supply control that enables adaptive performance regulation of individual voltage islands in an SoC has been presented in this paper. The proposed system solution consists of two independent negative feedback control loops that deal with operational drifts and workload changes of the island. In this implementation we have re-used standard power-switches to carry out the island's linear voltage regulation. The proposed solution enables local performance optimization of the IC and offers an integrated standby (or inactive) mode for each region. Another advantage over prior art is the fact that the IC's global power distribution network is not affected, which simplifies chip implementation significantly. The proposed solution offers fast dynamic response, i.e. low transition times, at the cost of reduced power conversion efficiency as compared to off-chip DC-DC conversion. Finally, the system is written in VHDL code and is fully synthesizable using a standard cell library and commercial tools.

6. Acknowledgements

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