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Integrated Transceivers for Emerging Medical Ultrasound Imaging Devices: A Review

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(Invited Paper)

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ABSTRACT As medical ultrasound imaging moves from conventional cart-based scanners to new form factors such as imaging catheters, hand-held point-of-care scanners and ultrasound patches, there is an increasing need for integrated transceivers that can be closely integrated with the transducer to provide channel-count reduction, improved signal quality and even full digitization. This paper reviews compact and power-efficient circuit solutions for such transceivers. It starts with a brief overview of ultrasound transducer technologies and the operating principles of the ultrasound transmit-receive signal path. For transmission, high-voltage pulsers are reviewed, from compact unipolar pulsers to multi-level pulsers that provide amplitude control and improved power efficiency. The review of receive circuits starts with low-noise amplifiers as the power- and performance-limiting building block. Solutions for time-gain compensation are discussed, which are essential to reduce signal dynamic range by compensating for the decaying echo-signal amplitude associated with propagation attenuation. Finally, the option of direct digitization of the echo signal at the transducer is discussed. The paper ends with a reflection on future opportunities and challenges in the area of integrated circuits for ultrasound applications.

INDEX TERMS Ultrasound imaging, high-voltage pulsers, analog front-ends, low-noise amplifiers, time-gain compensation, in-probe digitization.

I. INTRODUCTION

ULTRASOUND imaging is widely used to assist diagnosis and guide treatments in a broad range of medical applications, such as obstetrics and cardiology. Although ultrasound imaging has been around for decades, new developments are poised to radically change the way ultrasound is used. First, the form factor is changing. While ultrasound imaging is still mostly based on hand-held probes connected to a bulky imaging system, it is now becoming available in the form of pocket-size handheld scanners [1], endoscopes [2], catheters [3], pills [4] and patches [5] (Fig. 1). Second, ultrasound imaging is moving from 2D to 3D. While conventionally a 1D transducer array is used to produce 2D cross-sectional images, 2D arrays that can generate 3D images become increasingly common, not only in hand-held probes, but also in miniature probes like endoscopes and imaging catheters [2], [3]. Third, ultrasound is moving out of the hands of an expert sonographer into more widespread use by clinicians in general and, eventually, by the general public, calling for cost reduction and increased user-friendliness [1].

Integrated circuits play a key role in these developments. The electronics architecture of conventional imaging systems, based on commercial off-the-shelf components, is not scalable to the mentioned new form factors in terms of size and power consumption. Moreover, in terms of channel count, these architectures are not scalable to 3D imaging. Integrated transceiver circuits, closely integrated with the ultrasound transducer array, can solve these problems, *e.g.*, [2], [7], [8]. Combined with the move from conventional labour-intensive and expensive bulk-piezoelectric transducer technology to micro-machined transducers, integrated circuits also pave the way to the cost reduction needed for more widespread use [1].

This paper reviews recent advances in the design of integrated ultrasound transceivers. Section II starts with a review of transducer technologies and ultrasound system architectures, highlights the enabling role of integrated transceivers for new applications, and links system requirements to

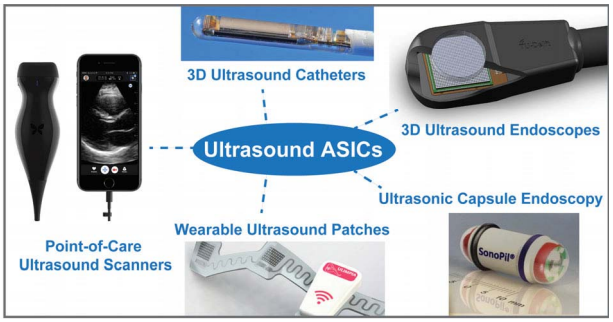

FIGURE 1. Examples of emerging medical ultrasound imaging devices (clockwise from the left): a hand-held point-of-care ultrasound scanner (image courtesy of Butterfly Network) [1]; a 3D intra-cardiac imaging catheter [3]; an artists impression of a 3D transesophageal ultrasound probe [2]; a pill-shaped ultrasonic endoscopy device (image courtesy of Univ. of Glasgow) [4]; an artist's impression of a wearable ultrasound patch (image courtesy of ULIMPIA project) [6].

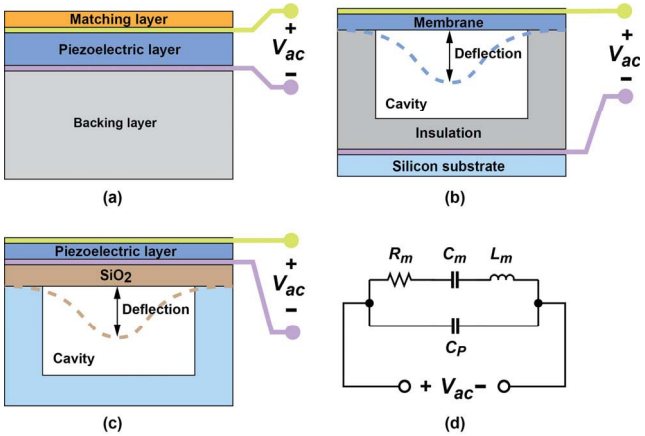

FIGURE 2. Schematic representation of (a) a bulk piezoelectric transducer, (b) a capacitive micromachine ultrasound transducer (CMUT), (c) a piezoelectric micromachined ultrasound transducer (PMUT), and (d) the Butterworth-Van Dyke equivalent circuit model.

front-end building-block specifications. Section III discusses recent advances in integrated transmitter circuits, while Section IV focuses on receiver circuits. Finally, Section V draws conclusions and provides an outlook.

II. ULTRASOUND SYSTEM ARCHITECTURE

A. ULTRASOUND TRANSDUCERS

In an ultrasound imaging system, the transducer is responsible for emitting acoustic waves into the body and for recording the returning echo signals [9], [10]. While information about the depth from which an echo originates can be derived from its arrival time, the ability to resolve objects or scatterers laterally is obtained by means of beamforming. For this, ultrasound transducers tend to be divided into an array of elements. For 2D imaging, 1D arrays (linear arrays or phased arrays) are used, with up to 256 elements. For 3D imaging without resorting to mechanical translation or rotation of a 1D array, a 2D array is needed (also referred to as a matrix transducer), which can consist of thousands of elements. The overall size (aperture) of the array relates to the field of view and spatial resolution that are required, while the element pitch tends to be dictated by beamforming requirements (in particular the need to avoid grating lobes). For phased-array transducers, this implies that a pitch of about half the wavelength is needed [9].

The vast majority of ultrasound probes in use today is based on bulk piezoelectric transducers (Fig. 2a) [9]. A layer of piezoelectric material, typically a piezoceramic such as lead-zirconate-titanate (PZT) or a piezocomposite, is mechanically diced into elements and equipped with top and bottom electrodes. An AC voltage applied to these electrodes is converted into a pressure wave through the piezoelectric effect, while, conversely, an incoming pressure wave can be detected as a charge displacement or voltage change on the electrodes. Mechanically, such a transducer is a thickness-mode resonator tuned to the frequency range of interest, typically with a low quality factor to allow transmission of short pulses. To ensure effective coupling of the acoustic waves into the medium in spite of mismatches in acoustic impedance, backing and matching layers are used. Fabrication of bulk piezoelectric transducer arrays, in particular 2D arrays, is relatively complex, time-consuming, and hence expensive.

To overcome these fabrication challenges, wafer-scale batch-fabrication techniques have been explored extensively as an alternative [11], [12]. The resulting micro-machined ultrasound transducers (MUTs) are based on a thin flexible membrane fabricated using surface or bulk micro-machining techniques. In the case of piezoelectric MUTs (PMUTs), a thin piezoelectric film with electrodes is deposited on the membrane (Fig. 2b) [12].

In the case of capacitive MUTs (CMUTs), the membrane is electrostatically actuated by means of electrodes in the membrane and in the substrate underneath (Fig. 2c) [11]. Typically, a relatively large DC bias voltage is applied to statically deflect the membrane and linearize its behavior. A smaller superimposed AC voltage is used for transmission, while for reception, the charge displacement due to capacitance changes associated with membrane deflection is detected.

In spite of their very different operating principles, the electrical impedance of all three mentioned transducer types can be modeled, to first order, using a so-called Butterworth Van-Dyke model (Fig. 2d), which includes a resonant branch (R_m, L_m, C_m) that models the mechanical resonance of the transducer, and a capacitor (C_p) that represents its electrical capacitance [13]. This single-port model proves useful in modeling the load that the transducer represents at the output of a transmit circuit, and in modeling of the transducer as a small-signal source at the input of an LNA, where a source can be included in the resonant branch to represent the acoustic input, and the thermal noise associated with R_m represents the noise contribution of the transducer. For a more accurate representation of the acoustic domain, a two-port model can be adopted [14].

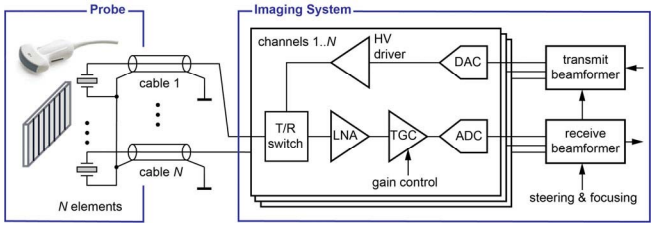

FIGURE 3. Block diagram of a conventional ultrasound imaging system.

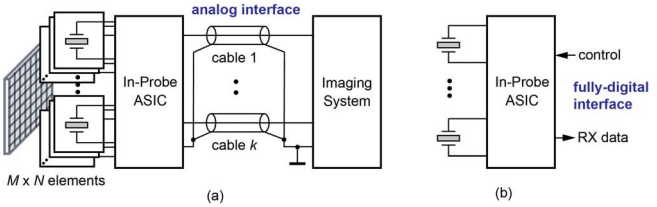

FIGURE 4. Smart ultrasound probe with in-probe ASIC.

B. CONVENTIONAL ULTRASOUND IMAGING SYSTEMS

Fig. 3 shows a block diagram of a conventional ultrasound imaging system interfacing with a probe containing an array of N transducer elements, each of which serves to transmit (TX) and receive (RX) acoustic waves [10]. These elements are connected using cables to transceiver channels in the imaging system. For transmission, the elements are driven by pulses timed by a TX beamformer to achieve a desired spatial distribution of the acoustic wave, typically focusing it at a point along the scan line to be imaged. To generate enough pressure to yield detectable echo signals even at the deepest point to be imaged, where propagation attenuation strongly reduces the signal amplitude, the transducer elements are typically driven with high-voltage (HV) pulses, with amplitudes ranging from tens of Volt to even more than 100 V. These pulses are fed to the elements through transmit/receive (T/R) switches that protect the receive circuits during pulse transmission.

After transmission, the echo signals received by each transducer element are amplified by a low-noise amplifier (LNA). In an attenuating medium such as the human body, the first echo signals that return to the probe, which come from scatters close to the probe, have higher amplitudes than echoes arriving later, which come from deeper scatters and hence are subject to more propagation attenuation [9]. This decreasing amplitude is compensated for by a time-gain compensation (TGC) amplifier, which provides a gain that increases linearly-in-dB with time [10]. Thus, the dynamic range is strongly reduced. The echo signals are then digitized by an analog-to-digital converter (ADC) (typically preceded by an anti-aliasing filter, not shown in Fig. 3).

An RX beamformer combines the digitized echo signals, in the simplest case by means of a delay-and-sum operation, so as to constructively add signals coming from a desired focal point while suppressing signals from other locations [9], [10]. The output of the RX beamformer is further processed to render an image. In the case of brightness-mode (B-mode) imaging, both the TX and the RX beamformer focus on a point along a scan line in the medium. Envelope detection of the output of the RX beamformer then yields the image brightness along the corresponding line in the image. Multiple scan lines are combined to form the image, each of which requires a cycle of pulse transmission and echo reception [9].

Due to the one-to-one correspondence between transducer elements, cables and transceiver channels in the architecture of Fig. 3, the number of elements is limited by practical constraints in cable count and system size to at most 256 for high-end imaging systems, *e.g.*, [15]. This limits the use of matrix transducers needed for 3D imaging, which readily consist of thousands of elements.

C. INTEGRATED CIRCUITS IN THE PROBE

A primary motivation to integrate ASICs into ultrasound probes is to bridge the gap between the high number of transducer elements needed for 3D imaging, and the limited number of system channels (Fig. 4a). Various approaches have been taken to do so, including multiplexing [16]–[18] and sub-array beamforming [2], [7], [19]. In these cases, the ASIC provides analog output signals to the imaging system. ASICs also help to improve signal-to-noise ratio (SNR), as they locally amplify the echo signals received by the transducer elements, thus avoiding the signal attenuation associated with connecting the small, high-impedance elements of a matrix transducer to long cables.

The functionality of in-probe ASICs can go well beyond channel-count reduction. For instance, the ASIC can provide full digitization (Fig. 4b) and further processing of the echo signals [8], [20]. In the case of portable ultrasound probes, this is an essential step, as the imaging system with analog front-ends and ADCs has been replaced by a smartphone or tablet [1]. Thus, the data acquisition functionality that was traditionally implemented in the imaging system moves into the ASIC, while the image processing is implemented in software.

D. TRADE-OFFS IN TRANSCEIVER DESIGN

Key building blocks of any in-probe ASIC are the element-level transceiver circuits. They determine to a large extent the performance in terms of SNR, and tend to dominate power consumption, and should therefore be carefully optimized.

Essential for this optimization is the analysis of the transmit-receive signal path, a typical example of which is illustrated in Fig. 5, in which each transducer element is driven by a pulser. The pressure generated at the surface of the elements depends on the amplitude of the applied pulse, and the transmit efficiency (expressed in Pa/V) of the transducer. In the case of focused transmission, the pulses

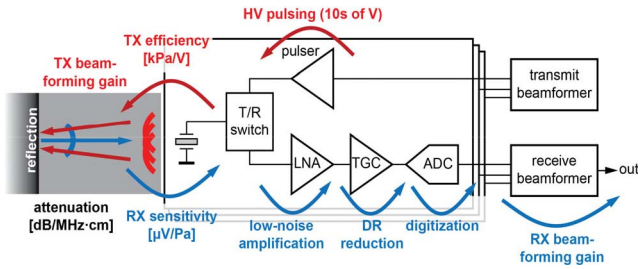

FIGURE 5. Transmit-receive signal path (with pulse transmission in red, and echo reception in blue).

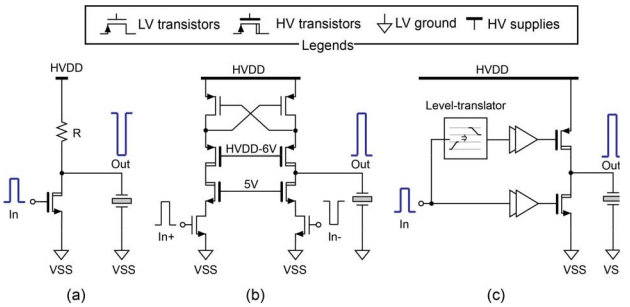

FIGURE 6. Variants of unipolar square-wave pulser front-ends: (a) a simple implementation using a single HV NMOS pull-up transistor [24]; (b) an HV cross-coupled level shifter [25]; (c) an HV inverter [26], [27].

are timed by the transmit beamformer such that the generated acoustic waves converge at the desired focal point. The pressure at this focal point can then be found by taking into account the TX beamforming gain and the propagation attenuation in the medium.

The acoustic wave will reflect from interfaces between regions with different acoustic impedance in the medium, leading to echoes that return to the transducer. The amplitude of an echo depends on the reflection coefficient associated with the interface, and the geometrical spreading and attenuation that the echo experiences as it travels back to the transducer. The resulting surface pressure at one of the elements then translates to a voltage through the transducer's receive sensitivity (expressed in V/Pa). This signal is amplified by the LNA and TGC and digitized, and finally combined with the signals from other elements by the receive beamformer. Here, the correlated signals from the different channels add up constructively, while uncorrelated noise does not, giving an RX beamforming gain. Note that other configurations are possible, *e.g.*, part of the beamforming may take place in the analog domain before digitization [19]. Still, a similar analysis will apply.

The system shown in Fig. 5 has many design parameters that need to be chosen to achieve a desired SNR at the RX beamformer output while minimizing power consumption. For a given array configuration, a given beamforming scheme and given transducer characteristics, the amplitude of the signal received by an individual transducer element is mainly dictated by the amplitude of the applied TX pulse, while the noise floor is limited by the noise of the element. The final SNR is degraded by the noise figure (NF) of the receive circuits, which can be improved at the expense of power consumption, and enhanced by the RX beamforming gain. Clearly, a minimum TX amplitude can be found for which the desired SNR is achieved in the ideal case of a noise-free receive circuits, *i.e.*, a NF of 0 dB. In many cases, this amplitude already exceeds tens of Volts, calling for HV pulsers implemented in special HV CMOS technology. The practical TX amplitude will need to be chosen higher, so as to leave room for a realistic NF, leading to a trade-off between TX power consumption and RX power consumption. Often, even at the highest TX amplitude supported by the CMOS technology, (average) TX power consumption is still far from dominant, due to the very short duration of pulse transmission compared to echo reception.

III. INTEGRATED TRANSMITTER CIRCUITS

While in conventional ultrasound systems, HV signals to drive the transducer elements are generated in the imaging system, the emerging devices addressed in this paper call for integration of TX functionality closer to the transducer. This can take the form of HV switching or multiplexing, which allows multiple transducer elements to be connected to a single TX channel in the imaging system [16]–[18]. However, to avoid the reduction in frame rate associated with multiplexing, it is desirable to generate the HV signals at the element level. Depending on the type of voltage waveform required, ultrasound transmitter circuits can be classified into two categories: pulsers and linear amplifiers. While both categories have been extensively adopted in discrete-circuit ultrasound systems [21]–[23], pulsers have been more widely adopted in integrated systems for their simplicity and superior power efficiency. Recent advances in solid-state circuit technologies, especially the rapidly expanding HV process options, have enabled several new on-chip transmitter solutions that address the diverse demands of emerging integrated ultrasound systems. This section reviews the latest advances of integrated transmitter circuits, with a special focus on emerging techniques for pulser design. A performance summary for state-of-the-art integrated pulsers is presented in TABLE 1.

A. SQUARE-WAVE PULSERS

As the simplest transmitter architecture, a square-wave pulser generates a wide-band excitation voltage that alternates between two voltage levels at a fixed or varying frequency. Unipolar square-wave pulsers were first adopted in integrated ultrasound transceivers for their simplicity. During transmission, their output swings between the ground potential and a single HV supply, either positive or negative. This typically can be realized using a small number of HV transistors. For example, in [24] Gurun *et al.* used a single HV NMOS transistor and a pull-up resistor to establish a compact pulser (Fig. 6a) for a high-frequency IVUS catheter where the space

TABLE 1. Performance comparison for state-of-the-art integrated pulsers.

	[25]	[26]	[7]	[38]	[39]	[30]	[37]	[8]	[40]	[41]
Target transducer	CMUT	CMUT	PZT	CMUT	CMUT	PMUT	PZT	CMUT	PMUT	N/A
Transducer capacitance [pF]	2.5	23	N/A	40	8	15.4	18	< 8	37.7	820
Process	1.5 µm HV CMOS	0.18 µm BCD-SOI	0.18 µm HV SOI CMOS	0.18 µm HV CMOS	0.18 µm 60V HV CMOS	0.18 µm LV CMOS	0.18 µm BCD	0.13 µm BCD	0.18 µm BCD	0.18 µm BCD
Max pulse voltage [V]	25V	100V	138V	30V	85 V	13.2V	60V	50V	28.7V	30V
Polarity	Unipolar	Unipolar	Bipolar	Unipolar	Unipolar	Unipolar	Bipolar	Bipolar	Unipolar	Unipolar
Pulse shaping	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Voltage levels	2	2	3	3	3	3	3	7	7	2
TX freq. [MHz]	N/A	10	1.5-2	3.3	8.33	5	7.5	1-10	1	N/A
Dynamic power saving	0%	0%	0%	38% (@3.3 MHz)	0%	32.8% * (@5 MHz)	N/A	0%	57.9% (@1MHz)	73.1%
On-chip area	0.02 mm^2	0.12 mm^2	0.04 mm^2	<0.3 mm^2	0.2 mm^2	0.02 mm^2	0.167 mm^2	<0.015 mm^2	10.8 mm^2	5.4 mm^2
Off-chip component	N/A	N/A	N/A	DC/DC converters	Capacitor (100 pF)	N/A	N/A	N/A	Capacitors (> 3 nF)	Inductor

* Only for dynamic power spent on charging and discharging parasitic capacitance to ground.

is limited. However, the current drawn when the pulser output is low results in power waste, and the pull-up resistor usually limits the pulse rising time when interfacing with a capacitive load, *e.g.*, a CMUT [11]. Alternatively, Wygant *et al*. employed a cross-coupled level-shifter with HV cascodes to eliminate static current while supporting up to 25-V unipolar pulses [25]. As shown in Fig. 6b, the cross-coupled pair at the high-side provides positive-feedback to ensure fast switching when driving highly capacitive MUTs. However, excess silicon area is required for the HV cascode pair. An inverter-type pulser [26], [27] as shown in Fig. 6c provides a better balance between power and area-efficiency. This requires an extra level-translator to drive the high-side PMOS relative to the HV supply (HVDD). It can be implemented using either a low-power capacitively-coupled latch, similar to [28], or a pull-up resistor in parallel with voltage-clamping diodes [8], [26]. Adding extra digital buffers between the level-translators and the gates of HV transistors helps to speed up switching [26], but requires a floating ground at the voltage of HVDD–V_{GS}, where V_{GS} is the gate-source voltage of the HV transistor. Alternatively, some designs [29], [30] proposed to generate HV pulses using stacked LV transistors, but this is associated with increased circuit complexity and potential reliability concerns.

A drawback of unipolar pulsers is that their output waveforms comprise a DC component (Fig. 7a), leading to a significant amount of the transmitted energy distributed around even-order harmonics [21]. This results in a loss of the round-trip SNR compared to a bipolar pulse with the same transmit pulse voltage. Moreover, it is not compatible with techniques like tissue harmonic imaging [31], which

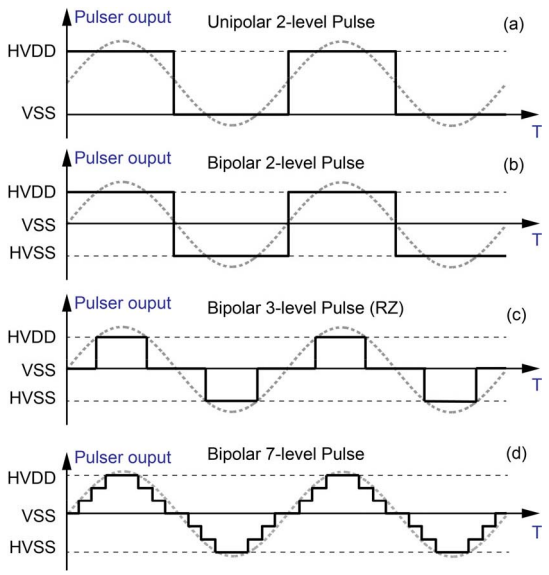

FIGURE 7. Typical pulse waveforms: (a) unipolar 2-level; (b) bipolar 2-level; (c) bipolar 3-level with return-to-zero; (d) bipolar 7-level.

improves the imaging quality by using second-order harmonics of tissue echoes. Furthermore, the utility of other non-linear imaging techniques, such as pulse inversion [32] and chirp coding [33], are also rather limited in unipolar pulsers. Integrated bipolar pulsers overcome these limitations by generating excitation signals that symmetrically transits between positive and negative HV voltage levels, as shown in Fig. 7b. The typical implementation of a bipolar pulser uses either an HV inverter [8] or a source-follower-based

push-pull stage [7] with positive and negative HV supplies as the front-end stage.

B. MULTI-LEVEL PULSERS

Multi-level pulsing (Fig. 7c, 7d) is becoming increasingly important for integrated ultrasound imagers because it 1) improves the transmission linearity and 2) allows temporal and spatial apodization by applying pulse-shaping to individual elements in a transducer array. Both contribute to sidelobe reduction and contrast enhancement in the reconstructed image. Moreover, some multi-level pulsing techniques help in saving the dynamic power dissipation associated with charging or discharging the capacitive load, provided that part of the charge can be recycled, *e.g.*, to regulated supplies during intermediate voltage transitions [34]. Finally yet importantly, for CMUTs that operate in the collapse mode [35], a multi-level pulsing profile reduces the membrane velocity at contact, which helps in improving the device reliability [1], [36].

As the simplest form of multi-level pulser, a 3-level pulser can be obtained by adding return-to-zero (RZ) switching to a bipolar square-wave pulser. In [37], this was realized by adding a direct discharging path from the transducer to ground via a HV floating-gate driver and a grounding switch. Alternatively, in [7] this grounding switch is added to the output of a pre-driver stage rather than the source-follower push-pull stage that drives the transducer directly. This helps in reducing the size of the switch transistor, but also eliminates potential savings of the switching power required for driving the transducer capacitance. In contrast, the design in [37] achieves ~50% dynamic power reduction as it resembles a 3-level charge-recycling pulser, which will be discussed below.

The general concept of N-level charge-recycling pulsers and its use in integrated ultrasound front-ends was first proposed in [38]. As shown in Fig. 8a, it employs (N-1) HV switches, each connected to a regulated voltage source, to charge and discharge the transducer in a stepwise manner. Rather than directly discharging the transducer capacitance to ground as in the case of square-wave pulsers, a 1/(N-1) portion of the charge stored on the transducer capacitance is recycled back to the regulated supply when the pulser transits between different voltage levels. As such, the dynamic power consumption (CVf^2) is reduced by a factor of N-1. A shortfall of this architecture is that it requires excessive HV switches when $N > 3$, which call for significant silicon area and dynamic driving power for driving internal gates rather than the transducer. Moreover, the need for multiple off-chip HV voltage sources complicates the system hardware. These problems prevent the application of charge-recycling multi-level pulsers in a large transducer array that calls for high integration density.

An alternative charge-recycling mechanism was proposed in [30], in which the two electrodes of a differential PMUT element are shorted to discharge the element, rather than switching both electrodes to ground. This helps to reduce the energy spent on charging and discharging parasitic capacitance to ground. In [39] and [40], a capacitive supply-multiplication scheme was proposed that substantially reduces power consumption, albeit at the cost of very large capacitors. Finally, the energy stored on the transducer capacitance can also be recycled using an inductor, for which power savings up to 75% have been reported [41]. However, the need for an off-chip inductor for each pulser makes this approach unsuitable for use with transducer arrays.

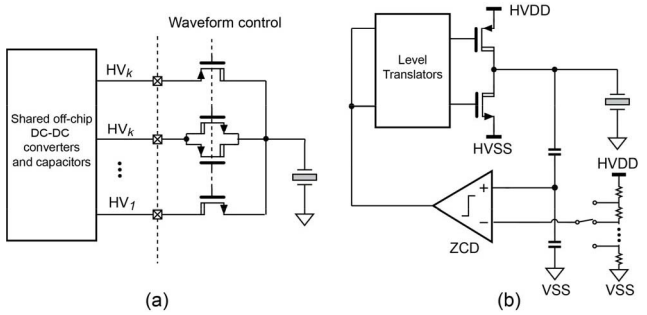

FIGURE 8. Pulser architectures that enable multi-level pulse shaping: (a) a charge-recycling pulser leveraging off-chip HV supplies [37]; (b) a feedback-based pulser [7].

As discussed in Section II-D, in an integrated ultrasound imaging system with a low TX/RX duty cycle, the transmission usually does not dominate the power consumption. This creates room for designers to trade the capability of dynamic energy saving for a more compact multi-level pulser. Sanchez *et al.* proposed a feedback-based 7-level pulser small enough to be closely integrated with a 208μm-pitch CMUT array [8]. Fig. 8b shows its conceptual schematic. It employs a capacitive voltage divider to scale down the HV pulser output voltage to a low-voltage (5V) domain, where a zero-crossing-detector (ZCD) and a digital feedback controller operate. There, the divided voltage is first compared with a scaled-down level-reference that is dynamically selected from a local voltage ladder. The decision is then sent to the digital controller to control the HV front-end to charge or discharge the transducer towards a target voltage. As neither HV transistors nor off-chip HV supplies are required in constructing the intermediate voltage levels, this solution permits the implementation of a highly compact multi-level pulser. It is worth noting that the accuracy of these voltage levels is directly affected by the ZCD overshoot [42], which can be optimized by implementing a dedicated ZCD bias control.

IV. INTEGRATED RECEIVERS

A. LOW-NOISE AMPLIFIERS

In most integrated ultrasound systems, an LNA is the first building block in the receive chain that interfaces with the transducer directly. It provides linear amplification of the echo signals to suppress the noise contribution from succeeding circuits. Depending on the impedance characteristic of the target transducer and the desired output format for further signal processing, such amplification can be

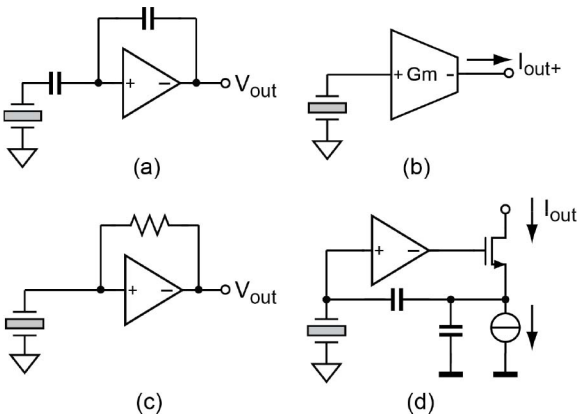

FIGURE 9. Ultrasound LNA topologies: (a) a capacitive-feedback voltage amplifier (VA); (b) a transconductance amplifier (TCA); (c) a resistive-feedback transimpedance amplifier (TIA); (d) a capacitive-feedback current amplifier (CA).

embodied as a voltage gain [43], a current gain [44], a transimpedance gain [45] or a transconductance gain [46]. As the LNA usually dominates the noise performance of an integrated receiver, it requires a considerable amount of power and area to guarantee an adequate NF for the entire system. In most cases, the majority of the receiver power is consumed by the LNA. A smart choice of the LNA topology requires an optimal trade-off between noise, power and area based on in-depth knowledge of transducer characteristics.

Among different LNA architectures, voltage amplifiers (VA) (Fig. 9a) [47], [48] and transconductance amplifiers (TCA) (Fig. 9b) [46] sense the transducer's voltage by creating a relatively high input impedance, while transimpedance amplifiers (TIA) (Fig. 9c) [26], [45], [49], [50] and current amplifiers (CA) (Fig. 9d) [51] sense the current by establishing a low input impedance virtual ground. Therefore, in integrated systems, VA and TCA are usually used to interface with transducers with lower impedance ($< 2\ k\Omega$), such as PZTs [52], [53] and PMUTs [30], [46], while TIA and CA are commonly adopted for CMUTs and polyvinylidene fluorides (PVDF) transducers [54], [55] which often exhibit relatively higher impedance ($> 10\ k\Omega$) [56]. Note that the transducer impedance is a complex function of its physical dimension, material, fabrication process and acoustic load. Therefore, for custom integrated systems a tailored analysis based on the specific transducer impedance profile is required to determine the optimal topology [57]. For example, the fine-pitch ($< 100\mu$m) PZTs for high-frequency IVUS applications as presented in [18] show a relatively high impedance (5 kΩ), making current sensing with a TIA the more energy-efficient choice.

On the basis of an efficient LNA architecture, various circuit techniques have been developed to further optimize the noise-power trade-off and area-efficiency. For instance, capacitive feedback has been exploited in both VAs [17], [47], [58] and TIAs [24], [26], [54], [59] to eliminate the noise contribution from the feedback path, at the cost of a slightly reduced bandwidth [60]. On the other hand, current-reuse amplifiers, either single-ended [2] or differential [8], [18], have been widely adopted in the implementation of the core amplifier to boost the current-efficiency and save area.

Besides noise, power and area, there are several specification parameters that should be considered when designing an ultrasound LNA for use in massively parallel arrays. For example, any subtle correlated signal that applies to an array of LNA channels, such as digital interference coupled to the analog supply, will get magnified with an extra gain of $\sqrt{N}$ (N being the array size) relative to its uncorrelated counterpart after array-level summing, averaging [8] or beamforming [2], [19]. This may result in distinct artifacts in the reconstructed ultrasound image [7], even if the original correlated noise is lower than the noise floor of individual LNA channels. Consequently, a power-supply rejection capability that is proportional to the size of the array is critical for LNA array design. Adding distributed supply regulators to each LNA subgroup is an effective way to address this challenge [47]. Similarly, any electrical crosstalk between neighboring LNA channels might cause elevation of side lobes, leading to artifactual echoes beside the main beam. Therefore, careful layout efforts are typically required to shield sensitive signals from each other despite their physical proximity.

As a summary, TABLE 2 lists a performance summary and comparison for state-of-the-art ultrasound LNAs targeting different types of transducers. We adopt the acoustic-domain noise-efficiency-factor (ANEF) [37] as a figure-of-merit (FoM) for this comparison:

$$ANEF = p_{n,in} \cdot \sqrt{P_{LNA}} \tag{1}$$

where $p_{n,in}$ is the input-referred acoustic pressure noise spectral density averaged across the passband, and P_{LNA} is the power consumption of the LNA. It measures the efficiency in trading the LNA power consumption for the minimum input-referred acoustic pressure noise. As noise is measured in the acoustic rather than the electrical domain, the transducer and the LNA are considered as a whole in the evaluation of the noise efficiency, which reflects the importance of selecting the optimal LNA architecture for maximizing the transducer receive sensitivity.

B. TIME-GAIN COMPENSATION AMPLIFIERS

There are various approaches to establish a TGC amplifier. Depending on how the gain control is implemented, these architectures fall into two main categories: programmable gain amplifiers (PGAs) with discrete gain steps, and variable gain amplifiers (VGAs) with continuous gain control. In both cases, the gain varies (approximately) exponentially with either the digital gain code or the analog control voltage, delivering a linear-in-dB time-gain profile.

A compelling advantage of PGAs for an integrated ultrasound system is that their gain steps can be precisely and robustly set, which is essential in ensuring the

TABLE 2. Performance comparison for state-of-the-art integrated ultrasound front-end amplifiers.

	[49]	[45]	[38]	[50]	[26]	[47]	[48]	[43]	[51]
Target transducer	CMUT	CMUT	CMUT	CMUT	CMUT	PZT	PZT	PMUT	PZT
Process	0.8 µm CMOS	1.5 µm HV CMOS	0.18 µm HV CMOS	0.18 µm HV CMOS	0.18 µm BCD-SOI	0.18 µm CMOS	0.35 µm CMOS	0.13 µm HV CMOS	0.18 µm BCD
Topology	TIA	Resistive-feedback TIA	Resistive-feedback TIA	Resistive-feedback TIA	Capacitive-feedback TIA	Capacitive-feedback VA	Open-loop VA	Open-loop VA	Capacitive - feedback TIA
Voltage gain [dB]	16	N/A	N/A	N/A	14.2	-12/6/24	16.5-31	21.8	N/A
Transimpedance gain [dBΩ]	N/A	112	96.6	104-116	N/A	N/A	N/A	N/A	70-107
Bandwidth [MHz]	11	25	5.2	10.2	10	9.8	6.6	22	7
Power/ch. [mW]	2	9	14.3	1.4	1	0.135	7.8	0.3	5.2
Input-referred Noise	6.5 nV/√Hz @ 1 MHz	0.9 mPa/√Hz @4.4MHz	0.55 mPa/√Hz @3MHz	0.41 pA/√Hz @8 MHz	0.55 mPa/√Hz *	5.5 nV/√Hz @ 2.5 MHz	5.4 nV/√Hz @ 2.5 MHz	7.1 nV/√Hz @ 3 MHz	1.7 pA/√Hz @ 5 MHz
Area/ch. [mm^2]	0.012	N/A	N/A	0.032	N/A	0.01	0.034	0.0006	0.12
ANEF $[mPa \cdot \sqrt{mW/Hz}]$	17	1.4	2.1	2.7	1	0.22	0.51	N/A	0.78

* Averaged across the bandwidth from 4.4 to 15.4 MHz.

gain uniformity across a large array. These discrete gains steps can be defined by digitally-programmable ratiometric passive component networks, such as resistor attenuators [8], resistive feedback [52], [53], [61], capacitive feedback [18], [20], [62] and current-steering feedback [63]. In addition, the PGA gain steps can be distributed across multiple amplifier stages, with coarse gain steps realized in the LNA and fine gain steps implemented in the succeeding PGA stages [20]. This helps in extending the gain range while keeping an acceptable area efficiency. The downside of a discrete-gain TGC scheme is that the switching transients between gain steps introduce both time-domain discontinuity and digital interference to the received signal, which can lead to noticeable image artifacts [1]. This problem can be mitigated by making the gain steps sufficiently small, typically below 0.5dB/step [8], [62], but at the cost of excessive silicon area due to the increased number of steps to cover the desired gain range.

In contrast, a VGA implements the TGC function by controlling the gain with a continuous-time signal, typically a ramping analog voltage. This avoids the switching transient issue associated with discrete gain steps. On the other hand, the translation from the linear control voltage to a decibel-scale gain profile inevitably increases the circuit complexity, especially in the analog domain. One approach is to control the bias point of bipolar or MOS transistors operating in their non-linear region [64]–[66] to realize an (approximately) exponential transducer function. This is, however, only effective within a limited gain range and vulnerable to process, voltage and temperature (PVT) variations, which complicates its adoption in large ultrasound arrays. An alternative approach is to implement continuous interpolation between discreate gain steps. A classic example is the design proposed by Gilbert in 1991 [67], which employs a resistive ladder attenuator and an N-path current-controlled transconductance stage to smoothly interpolate between the attenuator's outputs. Its demand for multiple transconductance stages makes its power and area efficiency less appealing for modern compact ultrasound devices. A more efficient solution that shares a similar concept is to use a differential pair to smoothly steer the output current of an amplifier between different taps of a discrete-type feedback network. By controlling the voltage applied to the differential pair, a continuous interpolation to the current gain of the amplifier can be realized. This approach was first proposed in [68] and recently got demonstrated in a compact variable-gain ultrasound TIA with compelling gain linearity and noise-power efficiency [51].

C. ELEMENT-LEVEL DIGITIZATION

While most state-of-the-art integrated systems perform signal conditioning, pre-beamforming or sub-aperture averaging in the analog domain before digitization, there has been a growing trend to move the analog-to-digital interface further towards the transducer element. From the system perspective, element-level digitization has several important advantages: it grants direct access to the RF data from individual elements, eliminates the constraint of fixed-aperture analog beamforming on the flexibility of imaging algorithms, and enables the integration of more powerful digital processing functions and artificial intelligence within a single ultrasound imaging device [1], [69].

The main obstacle on the road to element-level digitization is the mismatch between the large number of transducer elements and the limited power and area budget for per-element ADCs. Various attempts have been made to tackle this challenge. Kim *et al.* demonstrated a digital beamformer using element-level SAR ADCs

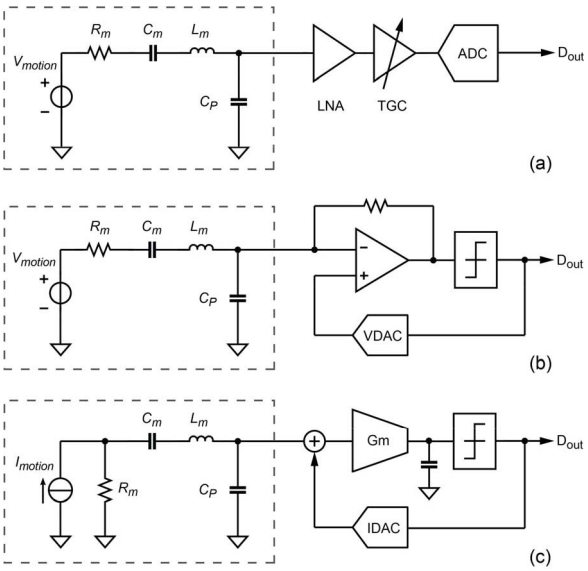

FIGURE 10. Element-level digitization topologies: (a) Stand-alone ADCs following an analog front-end [30], [62], [70], [71]; (b) an element-level ADC exploiting the transducer as a resonator of a bandpass $\Delta\Sigma$ modulator [72]; (c) an element-level ADC exploiting the transducer as a passive integrator of a lowpass $\Delta\Sigma$ modulator [73].

following conventional analog front-ends [70]. The ADC employs a conventional charge-redistribution capacitive DAC, hence requiring substantial silicon area, preventing it from being pitch-matched integrated with the transducer array. Chen *et al.* addressed this issue by leveraging a nanoscale CMOS process, and managed to integrate a $\Delta\Sigma$ ADC along with an analog front-end within the area of a single CMUT element [62], albeit at an energy efficiency that is not yet competitive with the analog approach.

It has become increasingly clear that ADC techniques customized for ultrasound signal processing would be the key to enabling element-level digitization. Lee *et al.* proposed a dynamic-bit-sharing technique based on the similarity of beamformed ultrasound signals, which allows adjacent element-level SAR ADCs in a 2×2 subarray to share the most-significant-bits, thus saving power [30]. Another hardware-sharing idea was proposed in [71], where a hybrid SAR/single-slope ADC shares its ramp generator with adjacent channels in a 2×2 subarray for area reduction. Both designs demonstrate promising area and power efficiency.

While all above approaches keep the analog front-end prior to the element-level ADC (Fig. 10a), a more radical solution is to establish the analog-to-digital interface right around the transducer element, turning it into an electromechanical filter of a closed-loop signal modulator. The feasibility of such direct digitization was first demonstrated in [72], where a piezoelectric transducer element is exploited as a resonator in a second-order bandpass $\Delta\Sigma$ ADC (Fig. 10b). Alternatively, a CMUT element which exhibits a more capacitive impedance can serve as a passive integrator in a continuous-time low-pass $\Delta\Sigma$ modulator (Fig. 10c), as described in [73]. The omission of front-end amplifiers grants these direct-digitization solutions an advantage in both power and area-efficiency. Future work will focus on integrating analog or semi-digital TGC functions into the loop, so as to extend the dynamic range of the ADC without compromising its efficiency.

V. CONCLUSION

This paper has reviewed circuit solutions for emerging ultrasound imaging devices, such as 3D imaging catheters, portable ultrasound scanners and wearable ultrasound patches. Despite the quite different operating principles of the transducer technologies currently available (bulk piezoelectric transducers, CMUTs and PMUTs), their electrical characteristics are quite similar, and hence similar circuit architectures can be applied. The paper has focused on the front-end building blocks that interface with the transducer elements and tend to limit power consumption and performance: high-voltage pulsers for transmission and low-noise amplifiers and time-gain compensation for reception. The paper has also reviewed advanced techniques, such a multi-level pulsing and element-level digitization.

Currently, most in-probe ASICs act as an interface between the transducer and a conventional imaging system, providing amplification for improved SNR, and channel-count reduction for 3D imaging, by multiplexing or sub-array beamforming. An emerging trend [7], [19], [29], [70] is moving from analog outputs to full in-probe digitization, to provide a robust digital interface to the system. This will enable further data reduction by means of in-probe digital signal processing. Moreover, standardized digital interfaces could ease the integration with other tools supporting the physician. Eventually, this can lead to the disappearance of imaging systems, with all front-end electronics integrated on-chip in the probe, and image processing moved to software [1]. Compared to PCB-based solutions [74], this is an essential step to reduce the size and cost of handheld ultrasound scanners. It is even more crucial for future wearable ultrasound devices [5], which can take ultrasound to home use, for instance for long-term monitoring applications. Such devices will have to operate from a small battery and communicate wirelessly, for instance with a smart phone. This will come with many new challenges, such as the need for drastic data reduction and improvements in power efficiency, that call for further advances in integrated circuit design for ultrasound applications.

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