Feedforward Phase Noise Cancellation Exploiting a Sub-Sampling Phase Detector

Bart J. Thijssen, *Student Member, IEEE,* Eric A. M. Klumperink, *Senior Member, IEEE,*
Philip Quinlan, *Member, IEEE,* and Bram Nauta, *Fellow, IEEE*

***Abstract*—This paper presents a feedforward phase noise cancellation technique to reduce phase noise of the output clock signal of a phase-locked loop (PLL). It uses a sub-sampling phase detector to measure the phase noise and a variable time delay for cancellation. Both phase noise and spurs are reduced. Analytical expressions have been derived that characterize the performance of this technique and show its fundamental limitations. A sub-sampling phase-locked loop with the cancellation technique as a built-in feature is described. The feedforward technique has no stability requirements in contrast to conventional PLL architectures. The phase noise reduction bandwidth is increased to almost a third of the reference frequency — 3x the maximal bandwidth for 3rd order type-II PLLs. The proposed analytical model shows a phase noise reduction of 9 dB at a frequency offset of $f_{ref}/10$. The total rms jitter is improved by 7.2 dB. The analytical results are verified by simulations.**

***Index Terms*—Clock generation, clocks, frequency synthesizer, jitter, phase detector, phase lock loop (PLL), phase noise, phase noise cancellation, sampling phase detector, sub-sampling phase detector, sub-sampling phase noise cancellation, timing jitter.**

I. Introduction

CLOCKS with low phase noise and jitter are required in many applications — e.g. analog-to-digital converters, optical data communication and RF front-ends. Sub-sampling phase-locked loops (SSPLLs) [1–4] have superior phase noise (PN) performance compared to conventional phase-frequency detector (PFD) PLLs. However, SSPLLs only reduce the close-in PN. The overall PN reduction is still limited to the maximal stable bandwidth of the PLL. For 3rd order type-II PLLs this is around the so-called Gardner's limit $f_{ref}/10$ [5].

A different method to reduce PN is by cancellation. This is a feedforward method and has therefore no stability limitations. Recently, several phase noise cancellation (PNC) approaches have been published [6–10]. In [7], the delay in a ring oscillator is exploited for a delay-discriminator PN detection. The cancellation is performed by a variable delay block. Although showing 12.5 dB PN improvement at $0.1f_{ref}$, the detection gain is constrained by limited inverter delay and the jitter performance is not state-of-the-art. [8] is also delay-line discriminator based and uses expensive off-chip components. The work in [9, 10] does not affect the clock PN, but the result of PN. In [9], the reciprocal mixing product as a result of PN is canceled and [10] cancels the PN in the digital domain — which does not improve the blocker noise figure.

B.J. Thijssen, E. A. M. Klumperink, and B. Nauta are with the Integrated Circuit Design Group, Centre for Telematics and Information Technology (CTIT), University of Twente (UT), 7500 AE Enschede, The Netherlands (e-mail: b.j.thijssen@utwente.nl)

P. Quinlan is with Analog Devices, Cork, Ireland

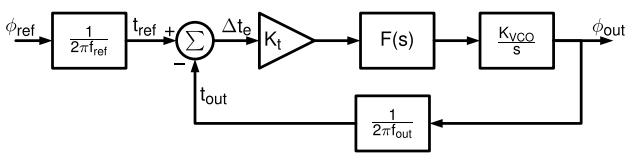

Fig. 1. Unified linear PLL model for timing error based phase detectors.

Injection-locked PLLs (ILPLLs) [11–13] and PLLs with cascaded sub-sampling delay-locked loops (SSDLLs) [14] are also promising techniques to improve clock PN. In ILPLLs the voltage-controlled oscillator (VCO) edge is aligned to the reference clock edge by injection. In the PLL with cascaded SSDLL, the phase error of a PLL is measured by a sub-sampling phase detector (SSPD) and corrected in a DLL; a feedback method. Recently, a feedforward PNC architecture was proposed that also exploits an SSPD [15]. All these techniques have ring oscillator implementations with state-of-the-art performance — a PLL FoM [1] around -235 dB.

In this brief, we analyze the fundamental limitations of a sub-sampling phase noise cancellation PLL (SSPNC-PLL) that we developed simultaneously but independently of [15]. Our analysis shows that the PN improvement is limited by aliasing and the SSPD hold operation. The SSPNC-PLL can achieve significantly lower rms jitter than an SSPLL alone.

The structure of this brief is as follows. First, in Section II, the PLL transfer characteristics are introduced. In Section III, the fundamental limitations of the feedforward PNC system exploiting an SSPD are analyzed. Section IV introduces the SSPNC-PLL. The theoretical results are verified by simulation in Section V and conclusions are presented in Section VI.

II. Phase-Locked Loops

PFDs and SSPDs both measure the timing difference of two incoming clock signals. The linear model of Fig. 1 allows for a *unified analysis* of PLLs with timing error detectors. It models the phase detector with jitter detection gain K_t, the loop filter with transfer function $F(s)$ and the VCO with transfer function K_{VCO}/s. The phase detector is often implemented including a charge-pump (CP) [1–5, 7]. The relation between output frequency f_{out} and reference frequency f_{ref} is

$$N \equiv \frac{f_{out}}{f_{ref}} \tag{1}$$

Note that we explicitly model the phase detector as a *timing error detector*, in contrast to the conventional approach of a phase detector [1, 5]. A divide-by-N — and multiply-by-N

in case of an SSPLL [1] — are not explicitly present in the model, because a frequency divider does not alter the timing instance of the clock signal zero crossings. Only the frequency of zero crossings is changed. In this brief, we use the following transfer functions of the PLL:

$$G(s) \equiv \frac{t_{out}(s)}{\Delta t_e(s)} = K_t F(s) \frac{K_{VCO}}{s} \cdot \frac{1}{2\pi f_{out}} \tag{2}$$

$$H(s) \equiv \frac{\phi_{out}(s)}{\phi_{ref}(s)} = \frac{1}{2\pi f_{ref}} \cdot \frac{K_t F(s) \frac{K_{VCO}}{s}}{1 + G(s)} \tag{3}$$

$$E(s) \equiv \frac{\Delta t_e(s)}{t_{ref}(s)} = \frac{1}{1 + G(s)} \tag{4}$$

A. PLL Phase Noise Spectrum

The output PN spectrum of the PLL can be derived given the additive noise at the different nodes in the model. Suppose, the CP noise $S_{i,CP}(f)$ and VCO PN $S_{\phi,VCO}(f)$ are the dominating components in the PLL output noise. The output PN spectrum can be determined as

$$S_{\phi,out}(f) = \left| \frac{2\pi f_{ref}}{K_t} \right|^2 |H(f)|^2 S_{i,CP}(f) + |E(f)|^2 S_{\phi,VCO}(f) \tag{5}$$

B. SSPD vs. PFD

The linear model of Fig. 1 can directly be applied to both SSPD and PFD based PLLs. Both phase detectors measure the timing difference of the two input clocks. The key distinction is in the timing detector gain [4]

$$K_{t,PFD} \propto f_{ref} \tag{6}$$

$$K_{t,SSPD} \propto \left. \frac{\mathrm{d}v(t)}{\mathrm{d}t} \right|_{t=t_{ref}} \approx 2\pi f_{out} \hat{v} \tag{7}$$

assuming a sinusoidal VCO output $v(t)$. In (7), $\hat{v}$ is the amplitude of $v(t)$ and t_{ref} the sampling instant. The slope of $v(t)$ is finite and known — e.g. provided by a constant slope generator [16]. The SSPD gain is approximately N times higher than of the PFD. Therefore, the CP PN contribution is reduced by N^2. The result is superior jitter performance of SSPLLs compared with PFD PLLs — e.g. [16] demonstrated 0.16 ps rms jitter while consuming only 8.2 mW.

C. SSPD Hold Delay

The SSPD introduces a delay of $0.5T_{ref}$ when it is implemented using an ideal sample-and-hold circuit. The result is 18° less phase margin for an SSPLL with bandwidth $f_{ref}/10$ — considerably reducing the loop stability. SSPLLs are often implemented with a pulser to reduce the SSPD gain and thereby reducing the required capacitor size for stable operation [1]. An added bonus is the reduced hold delay of the pulser implementation. This increases the phase margin and improves the SSPLL stability. The SSPD characteristics are further analyzed in Section III-A.

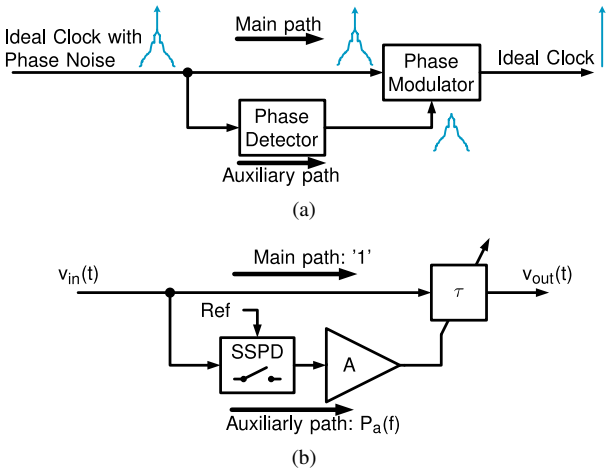

Fig. 2. Feedforward phase noise cancellation. (a) Basic principle [6–8]. (b) Block implementation [15].

III. Feedforward Phase Noise Cancellation

Feedforward PNC relies on the principle shown in Fig. 2a [6–8]. The PN of the input clock is detected in the auxiliary path and subtracted from the PN of the clock in the main path by a phase modulator. Ideally, the result is a clock without PN.

[15] proposed the implementation of Fig. 2b. It consists of an SSPD as phase detector, variable delay τ and an appropriate gain A. The SSPD bandwidth is constrained by the Nyquist limit $f_{ref}/2$. This potentially allows for PN reduction up to 5 times the maximal PLL bandwidth. In this brief, we refer to frequencies up to $f_{ref}/2$ as in-band and outside this range as out-of-band. Sub-sampling PNC can be cascaded to any generated clock signal as long as the reference and input clocks are aligned — e.g. realized by an SSPLL (Section IV).

In this section, we discuss the fundamental limitations of feedforward PN cancellation employing an SSPD. The variable delay and gain are assumed ideal. A possible implementation of the variable delay is e.g. with a current-starved inverter [15].

A. SSPD Analysis

An SSPD converts the timing error of input clock signal $v_{in}(t)$ into a sampled voltage, according to

$$v_{sam}(t_{ref}) = \Delta t_e \cdot \left. \frac{\mathrm{d}v_{in}(t)}{\mathrm{d}t} \right|_{t=t_{ref}} \tag{8}$$

where t_{ref} is the sampling instant. The timing error is

$$\Delta t_e = t_{ref} - t_{in} \tag{9}$$

where t_{in} and t_{ref} are the time instances corresponding to the zero crossings of the input clock and reference signal, respectively. The derivative of $v_{in}(t)$ is approximated as constant within time interval Δt_e.

Two mechanisms impair the PN detection performance: Aliasing during phase detection and the filtering of the hold function. During detection the clock PN aliases around every $f_{ref}/2$. The detected — sub-sampled — spectrum is

$$S_s(f) = f_{ref} \sum_{k=-\infty}^{\infty} S_{\phi,in}(f - k f_{ref}) \tag{10}$$

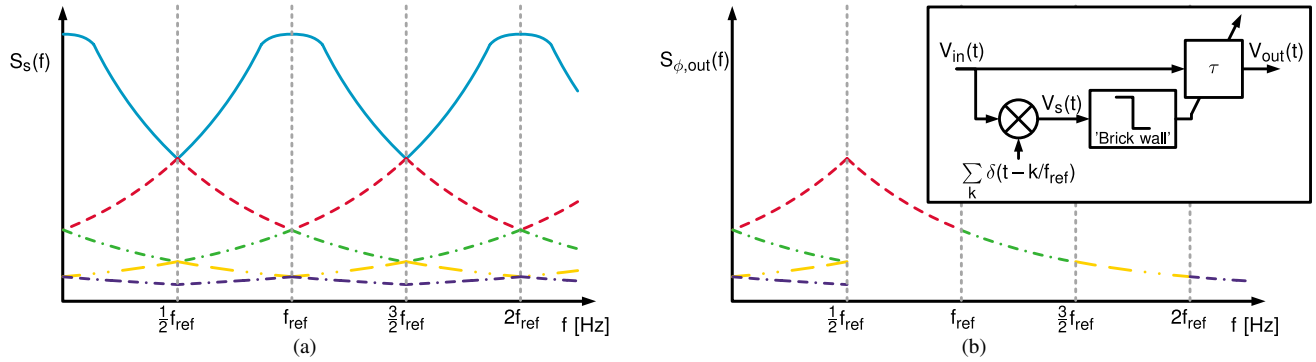

Fig. 3. Phase noise spectral components up to $k = \pm 2$. (a) After sub-sampling detection. (b) After cancellation with ideal reconstruction filtering.

This spectrum is illustrated in Fig. 3a. We assume a stationary input PN spectrum with bounded total rms jitter; e.g. the output of a PLL. The aliased spectral components are illustrated by color. The sum of these components is the actual detected spectrum. In addition to the wanted solid ($k = 0$) spectral component, several other spectral components alias towards the $[0, f_{ref}/2]$ band. Suppose an ideal brick-wall filter with cut-off at $f_{ref}/2$ is applied as reconstruction filter. As the filter comes after the sampler, the unwanted aliased components remain present in-band and are uncorrelated with the solid ($k = 0$) component that we wish to cancel. The resulting output PN spectrum $S_{\phi,out}(f)$ after cancellation is shown in Fig. 3b and can be approximated by

$$S_{\phi,out}(f) \approx \begin{cases} S_{\phi,in}(f_{ref} - f) & 0 \le f < f_{ref}/2 \\ S_{\phi,in}(f) & f \ge f_{ref}/2 \end{cases} \quad (11)$$

The aliased components up to $f_{ref}/2$ fundamentally limit the cancellation performance. Fortunately, the VCO PN shows a $1/f^2$ roll-off. This colored spectrum allows for PN detection even after aliasing, because in-band the non-aliased PN dominates the output of the SSPD.

In practical systems, a zero-order hold is applied to the sampled signal. The hold operation transfer function $H_h(f)$ is[†]

$$H_h(f) = T_h \,\mathrm{sinc}(fT_h) e^{-j\pi f T_h} \quad (12)$$

Several limitations arise due to the hold filter function:

- The hold attenuation limits the in-band cancellation.
- The delay of the zero-order hold impairs the cancellation performance, especially at high frequency offsets.
- The out-of-band aliases are only moderately filtered.

B. PNC Output Spectrum

Suppose, that the gain A and delay sensitivity K_τ are ideal, linear and with bandwidth $\gg f_{ref}/2$. The cancellation condition is

$$P_a(f) = f_{ref} T_h \,\mathrm{sinc}(fT_h) e^{-j\pi f T_h} A K_\tau = 1 \quad (13)$$

where $P_a(f)$ is the transfer function of the auxiliary path. $P_a(f)$ is frequency dependent, which means it is practically impossible to cancel at every frequency. The output spectrum of the PNC system $S_{\phi,out}(f)$ using (10) and (13) is

$$S_{\phi,out}(f) = \underbrace{|1 - P_a(f)|^2 \, S_{\phi,in}(f)}_{\text{correlated PN}} + \underbrace{|P_a(f)|^2 \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} S_{\phi,in}(f - k f_{ref})}_{\text{uncorrelated PN}} \quad (14)$$

In (14), we recognize two terms: The correlated PN ($k = 0$) and uncorrelated PN that is introduced by aliasing ($k \neq 0$). An equation with similar structure was also found for a feedback system analyzing sampling effects in PFD PLLs [17].

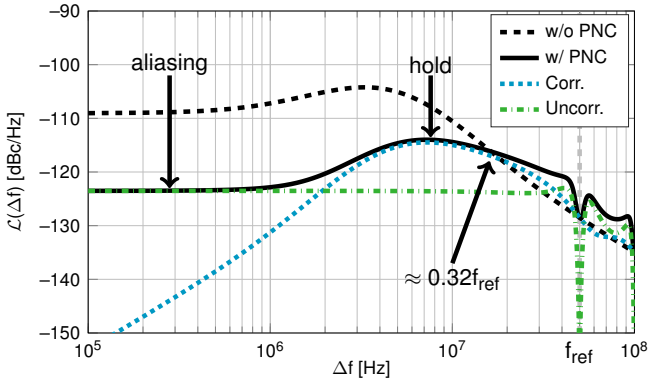

Fig. 4. Modeled phase noise cancellation output spectrum.

Fig. 4 illustrates the PNC performance for a clock with the PN spectrum of the Section V SSPLL; assuming $T_h = 1/f_{ref}$. The PN is canceled up to $0.32 f_{ref}$, more than 3x Gardner's limit. The reduction is limited by: aliasing at low frequency offsets, the hold operation at intermediate offsets and both correlated and uncorrelated PN contributions outside the cancellation bandwidth. (14) explains also the PN increase above roughly 10 MHz in [14]. Since, a wide bandwidth SSDLL does not provide filtering of aliased PN nor delayed PN that is introduced by the SSPD.

C. Practical Implementation Limitations

The total gain of the auxiliary path G_a should be 1. Mismatch between the main and auxiliary paths results in

[†]In this brief, we use the normalized sinc function: $\mathrm{sinc(x)} = \frac{\sin \pi \mathrm{x}}{\pi \mathrm{x}}$

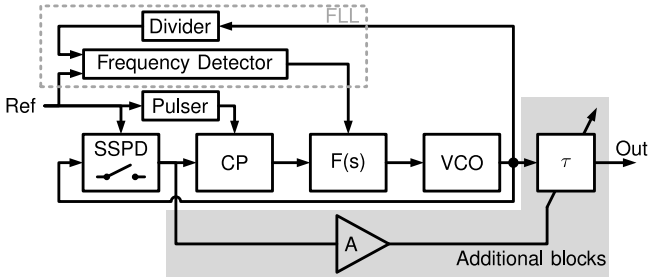

Fig. 5. Sub-sampling phase noise cancellation PLL [15].

imperfect cancellation, as expressed by

$$\text{Cancellation Limit} = 20\log|1 - G_a| \tag{15}$$

The required specification for maximal cancellation can be obtained from the fundamental limits. 90% accuracy limits the reduction to 20 dB, sufficient for the spectrum of Fig. 4. This also imposes the required linearity in the auxiliary path.

The PNC performance is in-band ultimately limited by the reference PN, which is directly present at the output. The noise contribution of A is small, because of the high SSPD detector gain; typically >1 GV/s. An SSPD phase offset introduces a delay offset in the variable delay. However, a fixed delay offset has no influence on the output PN — it just introduces clock skew. The input clock jitter should be constraint to avoid saturation of the variable delay. The variable delay τ can be part of an existing buffer [7], because the required delay is small; in the order of picoseconds, much smaller than the buffer rise/fall time. Therefore, the added jitter of the variable delay is marginal, since this is proportional to the delay [18].

D. Spur Cancellation

In addition to PN, other spurs introduced in the PLL loop are canceled as well. E.g. supply variations might introduce spurs at the VCO. In [15] it is shown that a spur at 100 KHz offset can be reduced by 19.5 dB.

IV. Sub-Sampling Phase Noise Cancellation PLL

The PNC system of Section III requires aligned zero-crossings of the reference and input clock. This is accomplished by cascading a PLL with PNC. In this way, the PLL aligns the clocks. The PLL is implemented by an SSPLL for minimal jitter. The SSPD error signal in the SSPLL can be reused for PNC, because both signals are the same — the SSPLL output phase error. The schematic of this sub-sampling PNC PLL (SSPNC-PLL) is shown in Fig. 5 [15]. It consists of a regular SSPLL with VCO, SSPD, CP, pulser and loop filter with transfer $F(s)$. The frequency-locked loop (FLL) is required to frequency lock the SSPLL [1]. Additionally, an appropriate gain and variable delay element for PNC are implemented. The SSPD is part of the SSPLL and reused for PNC.

The large detection gain of the SSPD results in only little required gain A in the auxiliary path, typically in the order of 1. Furthermore, the required bandwidth of A is small — approximately $5f_{ref}$ — and an existing buffer can be reused as variable delay. Therefore, we expect little additional power consumption compared with a conventional SSPLL.

To verify the derivations of Section III, the widely used 3rd order type-II PLL is applied, with loop filter [5]

$$F(s) = \frac{s\tau_2 + 1}{s\tau_1(s\tau_3 + 1)} \tag{16}$$

The bandwidth of the SSPLL can be estimated by [5]

$$K = K_t K_{VCO}\frac{\tau_2}{\tau_1}\cdot\frac{1}{2\pi f_{out}} \quad \text{[rad/s]} \tag{17}$$

From (5) and (14), the output PN spectrum of the SSPNC-PLL can be determined as

$$\begin{aligned} S_{\phi,out}(f) = {} & |1 - P_a(f)|^2 S_{\phi,SSPLL}(f) \\ & + |P_a(f)|^2 \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} S_{\phi,SSPLL}(f - kf_s) \end{aligned} \tag{18}$$

V. Simulation Results

The theory of Sections III and IV is verified in simulation. The assumptions of the simulations are listed below

1) The output frequency of the PLL is 2.5 GHz with a 50 MHz reference, ($N = 50$) and pulser on time of 1 ns.
2) The PLL is locked. The steady-state is achieved.
3) The CP noise and VCO PN are dominant. The VCO PN is purely $1/f^2$ and is modeled as additive white noise on the VCO input. The loop noise is modeled as additive white noise to the CP current. $1/f$ noise is neglected.
4) The reference is assumed clean; without PN.
5) The SSPLL is a 3rd order type-II PLL with loop parameters $K\tau_2 = 3$ and $\tau_2/\tau_3 = 9$. These normalization parameters fully characterize the PLL steady-state behavior and are identified as nearly optimum [5] when maximum bandwidth, good damping and as much filtering of the 3rd pole as possible is required.
6) The VCO PN is based on a 1 mW (ring) oscillator with $\text{FoM} = -163$ dBc/Hz — close to the theoretical limit of -165 dBc/Hz for ring oscillators [19].
7) The loop noise power is chosen such that the loop noise and VCO PN equally contribute to the total rms jitter; i.e. the bandwidth is chosen as the optimum bandwidth given the loop noise and VCO PN power [20].
8) Both the gain A and variable delay τ are ideal.
9) The noise spectra are obtained by averaging 200 (transient noise) simulations in Matlab Simulink.

Fig. 6 shows the output PN with and without PNC for both a PLL bandwidth of $f_{ref}/10$ and $f_{ref}/50$. We first discuss $f_{ref}/10$. The PN is reduced at low frequency offsets up to 15 dB. At 5 MHz offset ($f_{ref}/10$), the PN reduction is 8 dB. The PN reduction bandwidth is 14 MHz ($f_{ref}/3.6$). Outside the reduction bandwidth the PN is slightly increased as expected. The model of (14) is in accordance with the simulated PN spectrum. We define the cumulative rms jitter $\sigma_t(f_u)$ as

$$\sigma_t^2(f_u) = \frac{1}{(2\pi f_{out})^2}\int_0^{f_u} 2\mathcal{L}(\Delta f)\mathrm{d}\Delta f \tag{19}$$

The total rms jitter $\sigma_t(\infty)$ is improved by 3.2 dB.

The PNC system allows for novel loop filter designs to improve the jitter even further. Most of the jitter contribution

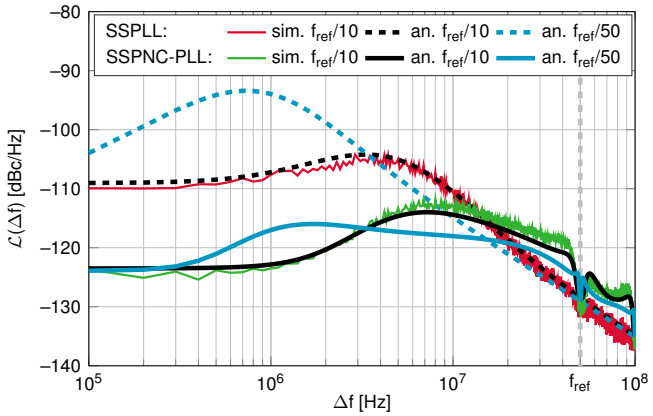

Fig. 6. Simulated (sim.) and analytical (an.) phase noise w/ and w/o PNC for different PLL bandwidths using (5) and (18).

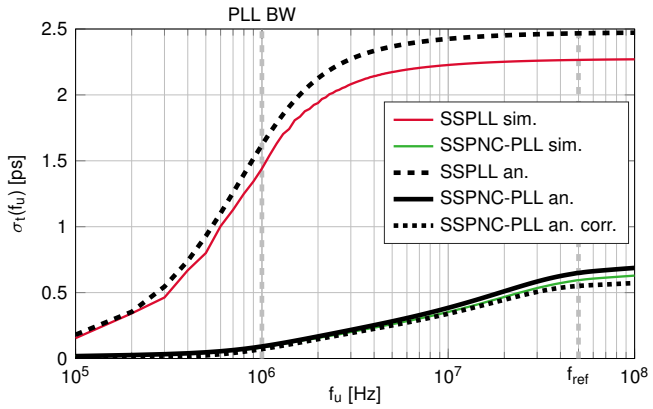

Fig. 7. Simulated (sim.) and analytical (an.) cumulative rms jitter w/ and w/o PNC, the SSPLL bandwidth is $f_{ref}/50$.

is around the PLL bandwidth. Reducing the PLL bandwidth repositions the PN bump to lower offset frequencies.

This is illustrated by the $f_{ref}/50$ plots in Fig. 6. At low offset frequencies the SSPLL PN slope is +20 dB/decade, so the VCO PN contribution is dominant. The PN reduction bandwidth is $0.3f_{ref}$. 9 dB PN reduction is achieved at a frequency offset of $f_{ref}/10$. The out-of-band PN is 4 dB lower than in the case of $f_{ref}/10$. The corresponding cumulative jitter is shown in Fig. 7. The jitter contribution is much more spread across frequencies than without PNC. The aliased components have only a minor effect on the total rms jitter as illustrated by the jitter of the correlated part. The total rms jitter is significantly reduced: 11 dB and 7.2 dB compared with the SSPLL with bandwidth $f_{ref}/50$ and $f_{ref}/10$, respectively.

Our analysis shows that the state-of-the-art performance of [15] can still be enhanced. The PN reduction bandwidth can be improved from roughly $f_{ref}/10$ [15] to $f_{ref}/3.6$ by increasing the auxiliary path bandwidth; significantly reducing the jitter.

VI. Conclusions

Feedforward phase noise cancellation can reduce the phase noise and jitter of clocks without stability limitation. A sub-sampling phase detector is attractive, because of its linearity and high detection gain. The performance of this detector is fundamentally limited by aliasing, hold delay, in-band hold attenuation and limited out-of-band attenuation of the aliases. A sub-sampling phase noise cancellation PLL architecture that reuses the error signal of a sub-sampling PLL is discussed for feedforward phase noise cancellation. Moreover, it cancels spurs that are introduced in the PLL loop. Analytical expressions are derived that predict the output phase noise given an input phase noise spectrum to the cancellation technique. These expressions are verified by simulations for a given wideband sub-sampling PLL design. The phase noise reduction bandwidth is increased to $f_{ref}/3.6$ by the phase noise cancellation technique. The phase noise is improved by more than 9 dB at a frequency offset of $f_{ref}/10$. The total rms jitter of the PLL is improved by 7.2 dB compared with a sub-sampling PLL with maximal bandwidth.

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