RF Self-Interference Reduction Techniques for Compact Full-Duplex Radios

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***Abstract*—This paper describes three RF self-interference reduction techniques for full-duplex wireless links, which specifically target integration in compact radios. Concretely, a self-interference cancelling front-end, a dual-polarized antenna, and an electrical balance duplexer are proposed. Each technique offers specific benefits in terms of implementation density, self-interference rejection, bandwidth and flexibility. Depending on their characteristics, they can be adopted in different next-generation full-duplex applications and standards. All concepts are prototyped, and achieve at least 45dB of self-interference reduction over more than 10MHz bandwidth.**

***Index Terms*—Full-duplex wireless, self-interference, polarized antenna, electrical balance duplexer, analog cancellation.**

I. INTRODUCTION

IN-BAND full-duplex is a promising scheme in wireless communications to increase the spectral efficiency and wireless throughput. As this scheme utilizes the same frequencies for simultaneous transmission and reception, novel communication techniques are being developed to improve e.g. the capacity and user access in cellular, access point and mesh networks [1]. The full-duplex (FD) scheme however sets challenging requirements for the radios, in particular their capability to prevent receiver sensitivity degradation due to self-interference (transmit signals leaking into its own receiver). The self-interference enters the receiver through various paths as illustrated in Figure 1: direct crosstalk (A), limited antenna isolation (B) and reflections through the environment (C). For FD operation, the self-interference (SI) should be *prevented* by minimizing leakage from the local transmitter (TX) onto its own receiver (RX), and should be *cancelled* at various points in the receiver chain by tapping signal copies from various points in the transmitter.

Recently, several radio designs were published dealing with the SI problem. Most of these techniques use bulky components and rely on the physical dimensions of the analog/RF circuits or antenna structure [1, 2, 3]. Therefore, these techniques can only be applied in devices with a larger form factor. Only few of the published techniques [4, 5, 6, 7, 8, 9] target integration in compact radio devices such as portable devices and small access points; e.g. [6] presents promising analog/RF and antenna design concepts for compact radio devices, and in [7, 8, 9] some of these concepts have been hardware prototyped and measured. As these techniques are implemented in RF, on a strong correlation between the cancellation signal and the source of SI is obtained [10, 11].

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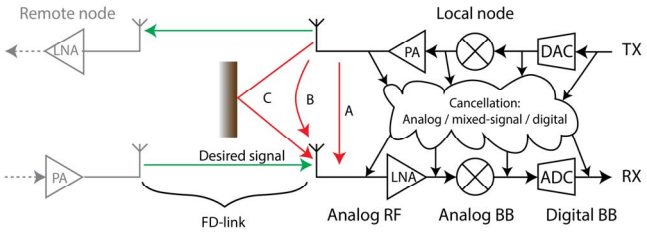

Figure 1: Full-duplex radio is subjected to different self-interference paths. Self-interference cancellation can be realized from various points in the transmitter chain to various points in the receiver chain.

This paper further elaborates these techniques, and describes the latest prototype designs of 1) the SI cancelling front-end, 2) the dual-polarized antenna and 3) the tunable electrical balance duplexer (see Figure 2). These designs aim at reducing types A and B self-interference (Figure 1), but cannot distinguish type C (reflected and delayed SI) from the desired signal. For typical link bandwidths in indoor environments, this limits the analog SI-isolation/cancellation to 40-60dB [2], relying on digital cancellation to suppress reflections and realize a complete FD system. Achieving this 40-60dB is also crucial to reduce the requirements on transmitter and receiver dynamic range as described in [6].

II. SI-CANCELLING FRONT-END

In compact FD radio devices, space may not permit sophisticated antenna solutions to provide high SI isolation. Also, a varying near-field environment (e.g. a person holding the device) constantly changes the magnitude and phase of type A and B self-interference (Figure 1), requiring an adaptive solution. Experiments using two crossed WLAN dipole antennas as a simple FD antenna showed that 20dB worst-case isolation is a reasonable assumption for a basic 2-port antenna solution in such situations. This leaves room for 20 to 40dB improvement in the analog domain before type C SI becomes the bottleneck [6].

For this application, an integrated front-end was implemented with a SI cancelling receiver (Figure 2) [9]. A

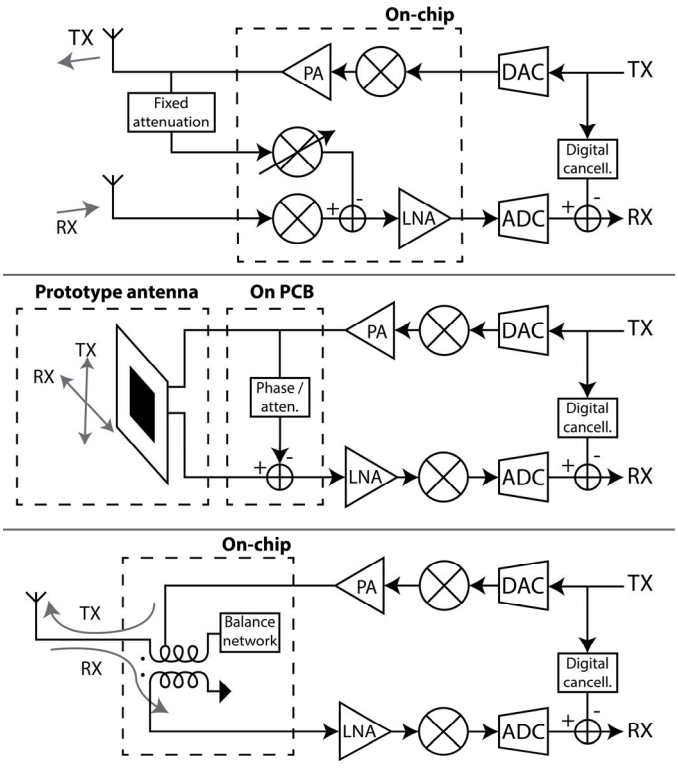

Figure 2: Three topologies to reduce self-interference, applied in a generic full-duplex transceiver structure with digital cancellation. The outlined parts are discussed in this paper. Top: front-end with SI-cancelling receiver, middle: dual-polarized antenna and active cancellation network, bottom: electrical balance duplexer.

second receiver path subtracts a phase shifted, amplitude scaled copy of the transmit signal in the analog baseband.

The prototype front-end in 65nm CMOS boosts the isolation of a moderately isolating antenna solution by 27dB for a wide range of SI amplitudes and phases. Despite the high power levels before cancellation, it maintains very low distortion at the receiver side. This is crucial to prevent masking the weak desired signal in distortion products, which would limit subsequent digital cancellation. The resulting design allows for sufficient digital cancellation to realize FD links at practical transmit powers (e.g. 0-10dBm) and ranges (e.g. 100 meters at 2.5GHz) [9]. The prototype is frequency-agile and can be operated between 0.15 and 3.5GHz.

A. Front-end design

As shown in Figure 2, the SI-cancelling path takes a copy of the transmitted signal at RF through a fixed attenuator. The attenuator value is chosen dependent on the worst-case isolation expected from the antenna solution. Subsequently, a variable phase shift and attenuation is applied, the signal is downmixed and the resulting signal is subtracted in the analog baseband. The advantage of this architecture is that phase shift, attenuation and downmixing can be efficiently combined in a *vector modulator (VM) downmixer*. Figure 3 shows a simplified implementation of the receiver with such a VM downmixer. Essentially, both the VM and the main RX mixer are 4-phase switched resistor mixers which maintain high linearity under large SI powers. The VM is a sliced version of the main RX mixer, incorporating multiplexers in each slice that steer the 4-phase output current to the appropriate baseband phases. For 31 slices, this results in a 32x32 constellation of discrete phase/amplitude values, theoretically allowing 28.5dB SI-cancellation.

As shown in Figure 3, the SI-currents are absorbed by the VM before any amplification of the received signal, resulting in high linearity and preventing clipping. Figure 4 shows a chip photo of the manufactured design.

B. Experimentation results

The linearity and raw cancellation performance of the receiver were evaluated in [9]. In current paper, the SI-cancellation performance is measured with the build-in transmitter and crossed WLAN dipole antennas as illustrated in Figure 5. A test signal of 20 tones with random phases over a 20MHz bandwidth are transmitted at 2.5GHz while the RX baseband bandwidth is set to 24MHz. The setup was located in an RF lab environment without taking any specific measures to induce or reduce reflections. The external attenuator is set to 20dB to mimic a worst-case antenna isolation of 23dB (including 3dB coupler loss).

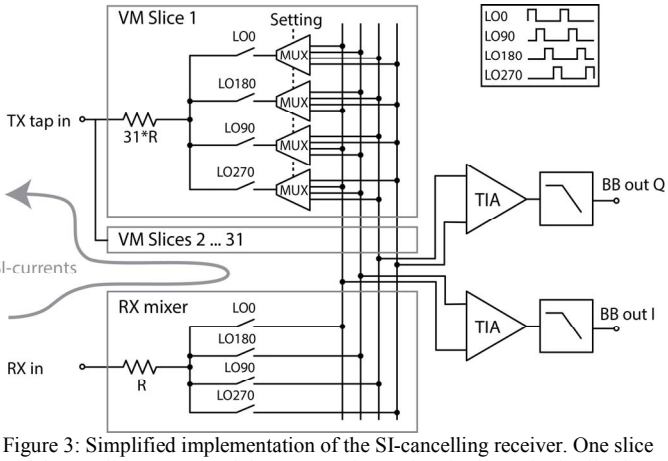

Figure 3: Simplified implementation of the SI-cancelling receiver. One slice of the 31-slice vector modulator (VM) downmixer is shown in detail. The depicted design is single-ended, the actual design is fully differential. For more implementation details, consult [9].

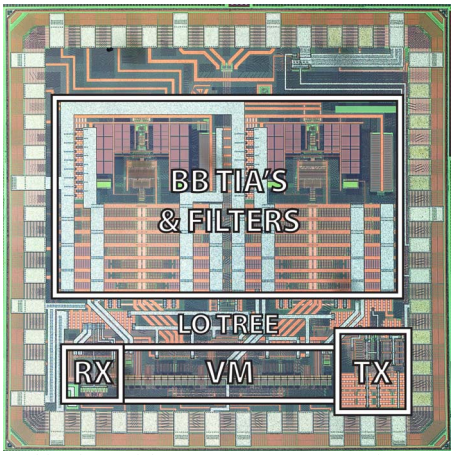

Figure 4: Chip photo of the 1.4 x 1.4mm prototype in 65nm CMOS.

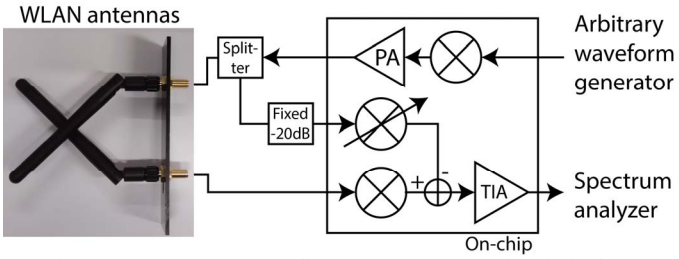

Figure 5: Test setup for cancellation measurements using the built-in transmitter and crossed WLAN dipoles as FD antenna.

Figure 6 shows measured spectra in the system: at the transmitter output, at the receiver input and after cancellation (referred to the receiver input). At a transmit power level of about 0dBm, the antenna isolation equals 28.9dB. Added with a VM cancellation of 16.8dB, the combined SI rejection equals 45.7dB. The residual SI becomes strongly frequency-selective, indicating the presence of reflected SI (type "C") in the residue, since this type of SI is delayed and therefore not well approximated by a phase shift & attenuation. For narrow bandwidths, the VM phase shifting and attenuation provides a better fit, resulting in increased SI cancellation. Delay can be implemented in an RF canceller with long delay lines [3], but is incompatible with CMOS integration. Therefore, in a compact radio, type C self-interference should be dealt with in the digital domain.

Finally, Table 1 lists the main specifications of the receiver side of the system. The transmitter characterization is ongoing.

III. DUAL-POLARIZED ANTENNA

The antenna is a critical block when building a FD radio. As both the TX and RX antenna are designed to operate on the same frequency, the RX antenna is likely to pick up part of the transmitted signal. Several antenna techniques were published [1, 2]] which suppress the TX-RX antenna coupling. As these techniques rely on physical spacing, they are inappropriate for integration in compact radio devices. An alternative antenna technique, implementing a small form-factor dual-port single antenna, is described in [6] and prototyped in [7]. This antenna is suitable for simultaneous transmission and reception due to the orthogonal polarization technique. Such an antenna, integrated in a complete radio system including additional RF cancellation, is illustrated in Figure 2.

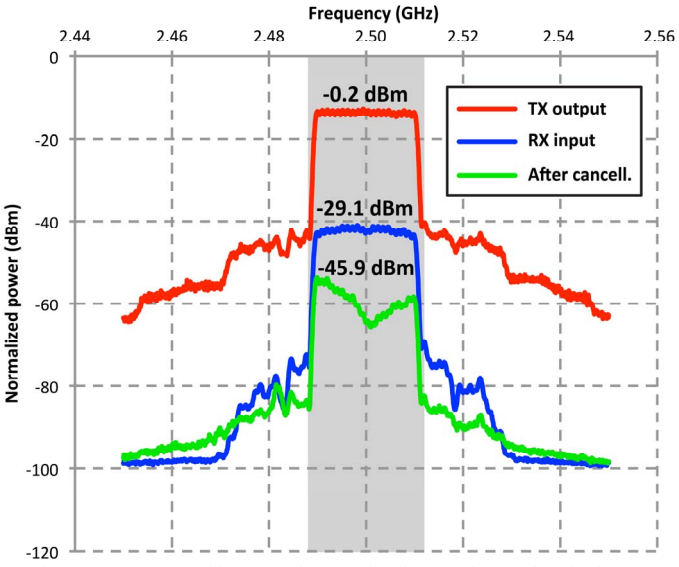

Figure 6: Spectra and integrated power levels at various points in the FD front-end, all referred back to the antenna ports for comparison. The shaded area indicates the 25 MHz integration bandwidth.

Table 1: Measured front-end receiver performances.

Mixer-first receiver + SI-cancelling VM-down-mixer	
Technology	65 nm CMOS
Supply	1.2V
Operating frequency	0.15 – 3.5 GHz
Maximum gain	24 dB
Noise figure	10.3 – 12.3 dB (6.3 in HD)
Power consumption	23 – 56 mW (RX incl. LO tree)
Baseband bandwidth	24 MHz (-12 MHz to +12 MHz)
In-band IIP3	+8 dBm
Effective in-band IIP3 for SI	+19 dBm
Out-of-band IIP3	+22 dBm
TX/RX isolation	27 dB
1/f Noise corner	2 MHz
Area	2 mm^2

A. *Dual-polarized antenna concept*

The antenna polarization determines the direction of the radiated electric field vector. The maximum energy transmission between two electromagnetic waves occurs when both waves have the same polarization, while the transferred energy is zero if both waves are polarized orthogonally. This behavior can be exploited in FD operation by polarizing the transmission and reception orthogonally such that a single radiating aperture antenna can be used with two independent excitation ports. The dual-polarized antenna prototype presented in [7] provides >50dB isolation over a bandwidth (BW) of 10MHz, and covers an area of 90x90mm. This BW is

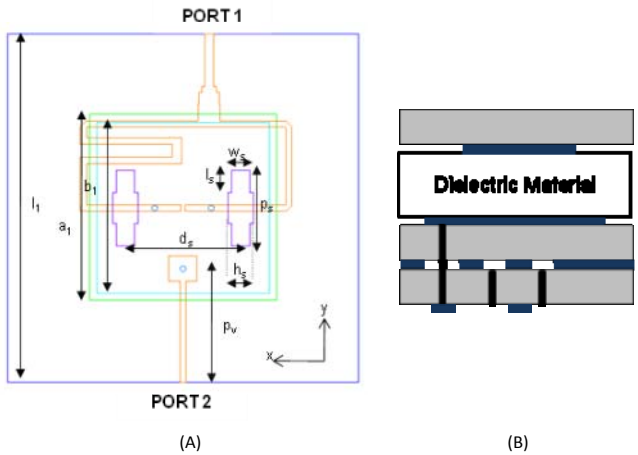

Figure 7: Geometry of the dual-polarized antenna. (A) Top view of the antenna, (B) multilayer antenna stack-up.

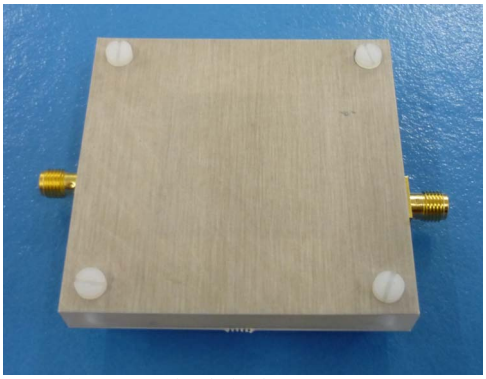

Figure 8: Dual-polarized antenna prototype.

Table 2: Dual-polarized antenna design parameters.

Parameter	d	I_1	a_1	b_1	d_s	p_s	I_s	h_s	w_s	p_x
Dimension [mm]	7.0	60	33	30	20	13.7	4.0	2.5	3.3	20.2

mainly limited by the impedance BW of the antenna. This prototype has been redesigned for increased BW and smaller form-factor as described in the following section.

A. Antenna prototype design and performance

Figure 7 illustrates the antenna geometry of the new dual-polarized antenna prototype. The antenna consists of two square patches and three substrate layers with the same thickness and dielectric constant. The horizontal polarization (PORT 1) is excited by a 1:2 divider, a 180º delay line and two coupled slots. The vertical polarization (PORT 2) is excited by a 50Ω microstrip line and an internal via. A rigid dielectric material with a dielectric constant of 2.5 separates the two square patches. The optimal design parameters given in

Table 2 were derived from geometrical parameter sensitivity analysis performed on the full 3D electromagnetic antenna model. These analysis were based on the 'Trust Region Framework' algorithm and considered a Rogers substrate with 3.55 dielectric constant and 0.508 thickness. The manufactured dual-polarized antenna prototype is shown in Figure 8 and measures 60x60x8mm.

The measured antenna matching, isolation and radiation performance over different operation bandwidths are reported in Table 3. These measurements were performed in a normal lab environment. This antenna prototype provides a 42dB SI-isolation over an 80MHz BW with an antenna efficiency of more than 70%.

B. Active RF cancellation

The changes in the environment close to the FD antenna may affect its performance in terms of passive suppression. To maintain a SI rejection of more than 50dB before the LNA, an active cancellation network operating in-between the antenna ports is used as indicated in Figure 2. This active RF cancellation network uses an attenuated and phase shifted copy of the transmitted RF signal to cancel the SI and implements a tunable attenuator and phase shifter. The remaining SI signal

Table 3: Measured specifications of the antenna prototype.

BW [MHz]	10 (channel)	80 (band)
Antenna Return loss	< -15dB	< -9dB
Antenna Isolation	< -49dB	< -42dB
Antenna Gain	> 6.5dB	> 5.5dB
Antenna XPD	> 24dB	> 20dB
3dB BeamWidth	> 70 deg	> 75 deg
Antenna efficiency	> 75%	> 70%

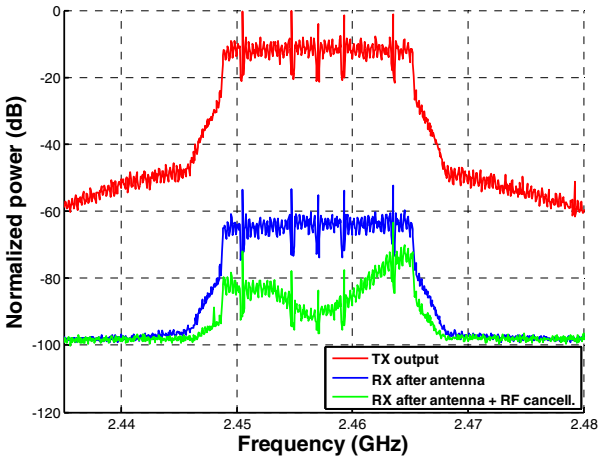

Figure 9: Lab-measured spectrum response of the dual-polarized antenna with and without active cancellation.

power automatically tunes these components based on a gradient descent algorithm [12]. Figure 9 shows the measured SI-isolation and cancellation performance of the dual-polarized antenna with and without the active cancellation network. The experiment uses a 16QAM modulated 15MHz bandwidth signal which is transmitted around 2.46GHz with an RF power of 15dBm. The residual SI is measured with a spectrum analyzer. The obtained dual-polarized antenna isolation equals 50dB, whereas active cancellation further improves the isolation to 62dB over the signal BW of 15MHz.

IV. Electrical Balance Duplexer

The antenna size is generally considered as one of the main bottlenecks for compact integration of FD radios. In the previous section, an antenna technique was described which combines transmission and reception in a compact form-factor antenna structure. When targeting even denser integration, it would be favorable to replace this special antenna structure with a conventional single port antenna, which are commercially available in extremely small size (e.g. SMD components). Such antennas require a duplexer in-between the antenna and the transceiver to prevent the TX signal from coupling into its own receiver. In frequency division duplex (FDD) systems, the signal suppression between TX and RX (simultaneously operating via the same antenna) is achieved by means of frequency selectivity, i.e. conventional filtering. Such filters cannot be applied to enable FD duplexing as there is no frequency spacing between the transmitted and received signals. Some FD designs propose a circulator to route the TX and RX signals over the common antenna [3, 13]. However, such circulators provide a moderate isolation (~20dB) and

would require additional cancellation loops at RF. Therefore, circulators are unattractive for implementation in compact radios such as smartphones. This section proposes an electrical balance duplexer (EBD) instead of a circulator. This hybrid junction circuit provides an attractive duplexing performance for FD (and potentially FDD operation [14]), can be densely implemented in CMOS technology and can be co-integrated with the transceiver circuitry.

A. Electrical balance duplexer concept

The EBD operation principle is illustrated in Figure 2; the RF circuit comprises a hybrid transformer and a balance network which is essentially a tunable dummy load impedance. In case the balance network impedance equals the antenna impedance, the isolation between the TX and RX is high [6]. The first prototype architecture was based on a differential receiver input [7], whereas Figure 2 depicts an alternative single-ended topology [8]. In this alternative topology, the balance network impedance must ensure that the different TX-RX transfer paths through the transformer destructively interfere at the single-ended RX port. Then, common-mode SI is avoided and high-power operation is enabled.

The first prototype [7] illustrated that an EBD can be densely integrated, i.e. 0.4mm^2 in 180nm CMOS, and offers acceptable FD performance. The measured average SI isolation of 50dB over 6MHz is limited by the ability to balance the antenna impedance over frequency. The second prototype [8, 7] has a redesigned balance network to overcome this BW limitation.

B. Multi-dimensional frequency tuning

In the first prototype [7], the balance network is implemented as a first-order RC network, resulting in a limited impedance variation with frequency and only two tuning dimensions, limiting the impedance control to real and imaginary at a single frequency. To increase the isolation BW, the balance network has been redesigned to enable (dependent) control of real and imaginary at two frequencies as depicted in Figure 10. The frequency tunability of these notches enables to track the antenna impedance across frequency, ideally allowing a trade-off between the BW and the average SI isolation performance.

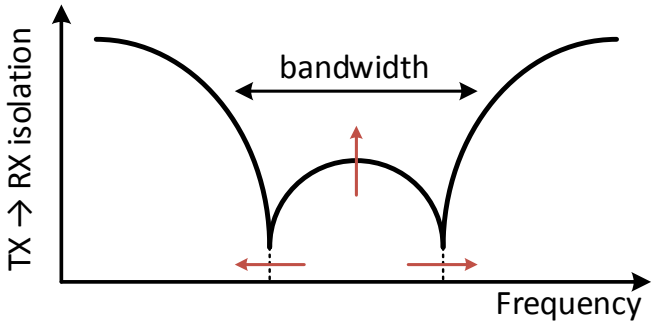

Figure 10: Multi-dimensional frequency tuning enables trading-off the bandwidth with the average SI isolation.

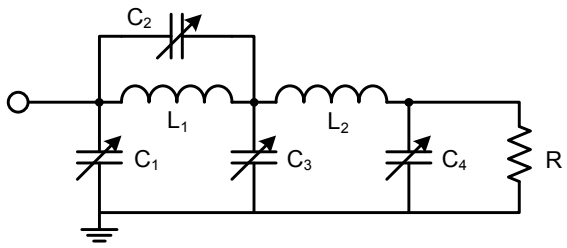

Figure 11: Balance network circuit topology enabling multi-dimensional frequency tuning and high-power operation.

The balance network should not only provide the multi-dimensional tuning, but also offer high power handling capability. To achieve this, the balance network topology depicted in Figure 11 was used for implementation in 180nm SOI CMOS. This technology, has a lower parasitic non-linear substrate capacitance compared to bulk CMOS and is favorable for stacking switches in tunable switched capacitors. Only the capacitors are tuned to achieve four tuning dimensions. To reduce the implementation area, only two inductors are used, and the resistor dissipates the power split between the antenna and the balance network. Up to 30dBm signal power can be applied to the TX port without breakdown issues.

C. Experimentation results

This balance network is implemented together with a transformer in 180nm SOI CMOS in a total area of 1.75mm^2. The average SI isolation versus BW trade-off is illustrated in Figure 12. The BW is drastically improved with respect to the first prototype [7], offering e.g. 55dB of SI isolation over 138MHz. Note however that these measurements were performed with a capacitive 50Ω reference impedance instead of a real antenna. The challenge of consistently balancing a real world antenna across frequency is left for future work.

V. CHARACTERISTICS

The previous sections describe three RF-SI rejection techniques. Although all techniques target integration in compact radios, they offer specific benefits and can thus be applied in different applications. Table 4 highlights specific characteristics of the different techniques.

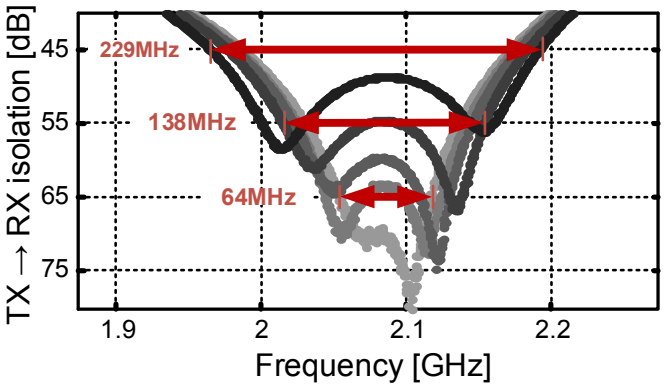

Figure 12: Measured electrical balance duplexer self-interference isolation performance with a capacitive 50Ω reference impedance.

Table 4: Specific benefits of the three proposed RF-SI rejection techniques

SI-cancelling front-end:
• *Integration:* dense on-chip implementation (2mm^2 in 65nm CMOS); suitable for mass-production and digital/analog/RF co-integration • *Antennas:* any two-port antenna solution with moderate initial isolation (e.g. two conventional WLAN antennas) • *Flexibility:* broad flexibility in operation frequency (0.15–3.5GHz), tunable SI cancellation • *Isolation & bandwidth:* Moderate isolation over a broad bandwidth (45.7 dB in 24 MHz with WLAN antennas)
Dual-polarized antenna:
• *Integration:* patch structure for system integration (60x60x8mm), larger than 2 other techniques • *Antennas:* one radiation aperture with 2 ports (TX/RX) • *Flexibility:* frequency fixed, tunable SI cancellation • *Isolation & bandwidth:* High SI isolation over a broad bandwidth (49dB/10MHz stand-alone and 62dB/15MHz with added active cancellation) • *Note:* Polarization dependent performance over wireless link
Electrical balance duplexer:
• *Integration:* dense on-chip implementation (1.75mm^2 in 180nm SOI CMOS); suitable for mass-production and digital/analog/RF co-integration • *Antennas:* one conventional single antenna (for simultaneous TX/RX operation) • *Flexibility:* frequency flexible, tunable SI cancellation • *Isolation & bandwidth:* Isolation vs. bandwidth trade-off, high peak SI isolation • *Note:* Moderate loss (<3.9dB), high TX-power capable

VI. Conclusion

This paper describes and prototypes three techniques to achieve more than 45dB of RF self-interference rejection over a bandwidth of more than 10MHz. The proposed techniques target integration in compact wireless radio devices for next-generation full-duplex applications and standards. Each technique offers specific benefits detailed below.

The integrated front-end includes SI cancellation path which is implemented via a 31-slice vector modulator downmixer for accurate, flexible and linear cancellation. The complete front-end, excluding the antennas, occupies 2mm^2 in 65nm CMOS technology and operates over a wide frequency range (0.15–3.5GHz). The SI isolation equals 45.7 dB in 24 MHz with WLAN antennas.

The dual-polarized antenna demonstrates a dual-port patch antenna of 60x60x8mm which offers, including an active RF cancellation network, 62dB isolation over 15MHz at 2.46GHz (including an active RF cancellation network).

The electrical balance duplexer demonstrates the usage of a conventional single-port antenna for full-duplex operation. The duplexer prototype offers frequency-flexible tuning to increase and trade-off the operation bandwidth with the SI isolation. The prototype, excluding the antenna, occupies 1.7mm^2 implemented in 180nm SOI CMOS technology.

This work brings full-duplex transceivers a step closer to realistic implementation and indicates the feasibility of full-duplex in compact radios.

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