Mixed-Signal Circuits and Boards for High Safety Applications*

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Abstract

A design methodology for analogue on-line test is presented by means of a real circuit implementation. The test strategy is based on monitoring via a very small analogue checker the inputs of all operational amplifiers of a fully differential circuit. The self-checking properties of the functional circuit are evaluated for a hard/soft fault model. Since the analogue checker outputs a double-rail error indication, the compatibility with digital checkers is ensured and the design of self-checking mixed-signal circuits becomes very simple. The mixed-signal approach is extended to boards through the IEEE Std. 1149.1 digital test bus and a layout rule to avoid interconnect differential shorts.

1 Introduction

Circuits for high safety systems require on-line monitoring of the function being performed. For many years on-line testing techniques have been developed for digital circuits using error-detecting codes. In the real world digital systems interact with analogue environments and thus the analogue part and the analogue/digital interface must also be monitored.

More recently, some techniques on concurrent error detection (CED) for analogue and mixed-signal single-ended circuits have been published [1,2,3]. The method we propose is aimed at mixed-signal circuits whose analogue parts are fully differential. The use of fully differential circuits has contributed to achieve the high linearity and/or the high signal-to-noise ratio required in high performance linear and non-linear applications [4]. In this work we concentrate on the on-line testing of the analogue parts of mixed-signal circuits.

The CED in fully differential circuits has been addressed before in [5] and [6]. In [5], a differential code is defined. In the use of this code, the problems of designing self-checking mixed-signal circuits for a single hard fault model are identified and a tentative way of facing them in the specific case of a sample-and-hold circuit is given.

In [6], the redesign of fully differential operational amplifiers (opamps) is proposed as the means of ensuring the detection of single transient faults by corruption of the differential code at the amplifier outputs.

In this paper, we propose an on-line testing approach based on monitoring some fully differential circuit nodes via an analogue checker. In order to comply with self-checking digital parts, this checker outputs a double-rail error indication. In comparison to previous works, ours has the following advantages: 1) only the inputs of opamps are monitored; 2) only one very small analogue checker is used for simultaneously monitoring all circuit stages; 3) hard and soft faults of components internal and external to opamps are simultaneously considered; and last, but not least, 4) the redesign of existing opamps is avoided.

Although our design methodology for analogue CED is based on a formal analysis of the self-checking properties in functional circuits and checkers, the theory is kept transparent to designers. The extension of our approach to mixed-signal boards implementing the IEEE Std. 1149.1 [7] is also proposed in this paper.

2 Preliminaries

2.1 Analogue fault modelling

At the circuit level, we assume a complete set of single hard (catastrophic) faults in internal elements [5] and a complete set of single hard and soft (parametric) faults in passive components external to opamps.

For the fault detection analysis, the external components that are implemented as switched-capacitor (SC) resistances are replaced by the corresponding continuous-time element. As shown in the example of figure 1, the switch stuck-on/stuck-open faults, the capacitor open/short faults and the capacitance deviations are fully mapped onto the fault modelling of the continuous-time resistor that we consider. The $R/R_{nominal}$ (R/R_n) ratios given in figure 1 were obtained by simulation for a classical switched-capacitor integrator.

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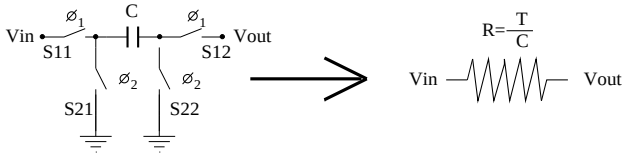


Fault location	Switch								Capacitor			
	Stuck-open				Stuck-on				open	C↓	C↑	short
	S_{11}	S_{12}	S_{21}	S_{22}	S_{11}	S_{12}	S_{21}	S_{22}				
R/R_n	∞	∞	6.4	6.4	4	6.6	∞	2.7	∞	↑	↓	0

Figure 1. Fault effects on a SC resistor.

The study of the influence of parameter deviations of passive components on the embedded testing mechanisms are usually based on sensitivity computation [8]. We address this problem by means of a new concept:

Definition D1: fault detection boundary [9]. Considering a circuit component P with a nominal value of P_n, the intention is to determine for each frequency the minimum deviations (both positive and negative with respect to the nominal value) of each component P which can be detected by an error function. For each component P, these values define the fault detection boundary of the component.

The region beyond the fault detection boundary of a component corresponds to deviations which will be detected. This region is called the fault detection region of the component. The capability to detect soft faults is then determined by computing the fault detection boundaries of the circuit components.

At the board level, interconnect faults considered are open and shorts. Since we deal here with fully differential circuits, special attention is paid to the case of shorts involving differential nodes.

2.2 A brief on the self-checking theory

In digital self-checking circuits, the CED capability is achieved by means of functional circuits which deliver encoded outputs and checkers which verify whether these outputs belong to the error-detecting code in use (figure 2(a)). In a more general way, we can say that, especially due to commonly used feedback circuitry, in the analogue case the nodes to be monitored by the checker will not necessarily be those associated with the functional circuit outputs (figure 2(b)).

Despite of this difference, analogue codes can be defined for performing on-line checking similarly to the digital case. For fully differential designs, we have:

Definition D2: differential code [5]. Let any two differential nodes + and − carry the components S_+ and S_- (with respect to analogue ground) of a signal S. The relation $S_+ \approx -S_-$ must be satisfied for S. Also let ϵ be the maximum commom mode signal admitted for S. Then the differential code space will be made up

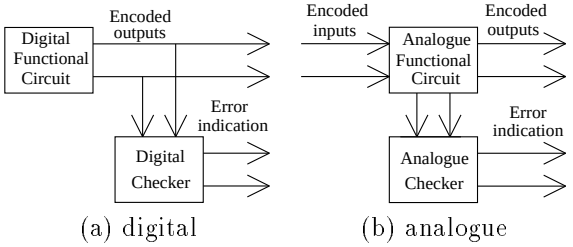


Figure 2. Self-checking circuit.

of all S for which $|\ S_+ + S_-\ | \leq \epsilon$ is met, and the noncode space by those signals for which $|\ S_+ + S_-\ | > \epsilon$ applies.

Definition D3: balance property. Let G be a differential circuit with inputs (U_+, U_-) and outputs (Y_+, Y_-) made up of switches and passive components and of a fully differential opamp whose inputs (X_+, X_-) are virtually shorted. Then the circuit G is balanced if: (a) its input and output signals are in the differential code space and, (b) the voltages at the opamp inputs (Vx_+, Vx_-) are virtually grounded.

The goal of (digital, analogue and mixed-signal) self-checking circuits – known as totally self-checking (TSC) goal – is to signal via the checker the first erroneous output of the functional circuit. In the case of analogue circuits, a tolerance is required for checking the validity of the functional circuit outputs. In general, it is assumed that faults occur one at a time, and, between any two faults, enough time elapses so that the functional circuit and the checker are sufficiently exercised. The properties required for mixed-signal and analogue circuits to achieve the TSC goal are:

Definition D4: finitely self-testing property [10]. G is finitely self-testing with respect to a fault set F if there is a subspace Af of the input code space A which has a finite number of elements and such that: for each fault in F there is at least one input value belonging to Af that produces a value on the nodes being monitored which does not belong to the checker input code space.

Definition D5: fault-secure property. G is fault-secure with respect to F if for all faults in F and all input values belonging to the input code space, the output value is either correct or it does not belong to the output code space.

Definition D6: finitely TSC property [10]. G is finitely TSC with respect to F if it is fault-secure and finitely self-testing with respect fo F.

If the checkers cannot achieve the self-checking properties when the application is executing, they can be accompanied by pattern generators for off-line testing. This technique is known as self-exercising and is extremely useful whenever noncode words are required to

fully test the checker capability of signalling functional error occurrences. The self-exercising technique is further discussed for the analogue case in [10] and [11].

3 Analogue CED design methodology

Our observability strategy consists of sensing the opamp inputs through a balance checking circuitry. We have observed in previous works that faults internal and external to the opamps corrupt the balance of the circuit [12]. It is thus expected that the TSC goal is achieved by checking the common-mode of these functional circuit sensing nodes.

Under the light of this observability strategy, our self-checking design methodology consists of 5 steps:
1) obtain a fully differential implementation of the transfer function;
2) define the differential code space by determining the tolerance admitted in the detection of a given fault set;
3) design a checker for this differential code space;
4) evaluate the fault coverage for the functional circuit and the checker;
5) evaluate the performance degradation of the transfer function resulting from the checker connection.

This methodology is hereafter exemplified by means of the SC biquadratic filter of figure 3. We next skip step 2 of our methodology and discuss in detail step 3. This is because the computation of the exact tolerance admitted in testing is extremely dependent on the technology in use and on the final application into which the circuit will be inserted.

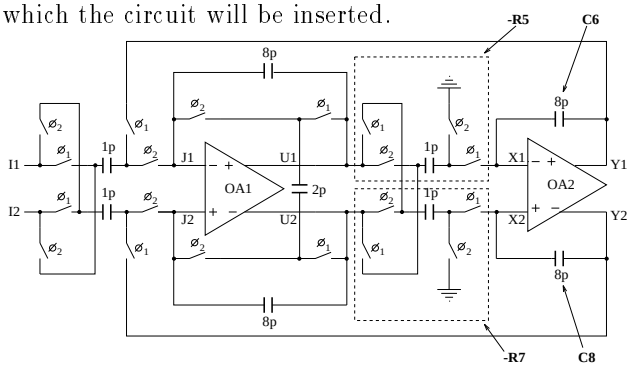


Figure 3. Fully differential SC filter.

4 Analogue checker design

The inputs of all differential amplifiers in the circuit (nodes J and X) are on-line observed by the analogue checker shown in figure 4. This checker is an extension of a common-mode feedback circuit as used to improve common-mode rejection in opamps [4].

During correct operation, all signals in nodes J and X are at analogue ground. Signals Vc and Vc' in the checker have the same constant voltage. As shown in [12], most single faults in an opamp and all single faults in passive components will corrupt the balance of the

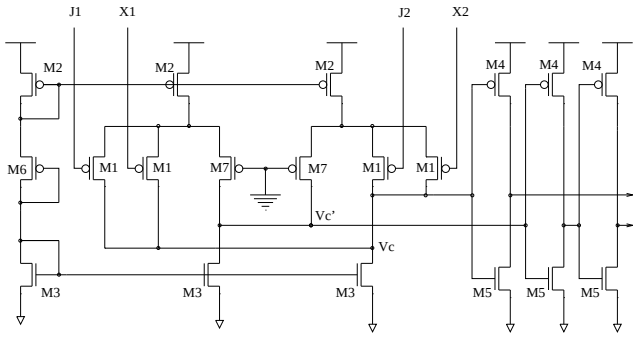


Figure 4. Analogue checker.

circuit resulting in a common-mode signal observed by the checker. The common-mode signal will change the current (and voltage) in node Vc and the opposite effect will result in node Vc' by virtue of the current sources.

Considering the valid approximation $gm1 \gg gl2$ (the transconductance of transistor M1 is much larger than the output resistance of transistor M2), the AC analysis of the circuit gives $Vc = -gm1 \cdot Vcom/gl3$ and $Vc' = gm1 \cdot Vcom/gl3$, where $Vcom = (V1+V2)/2$ represents the common-mode signal of the unbalanced node.

The sizes of the checker transistors are indicated in table 1. The silicon space required is very small. The transistor M7 is composed of two transistors M1 in parallel. The transistors are dimensioned such that an AC gain of 10 is achieved. Considering that the DC values of Vc and Vc' are set to approximately 1.5V, a common-mode signal of 100mV will trigger one of the two minimal size output inverters (which switch around 2.5 DC Volts). With this, a tolerance window [-100,100] mV is embedded in the circuit. For the two outputs of the checker, 11 or 00 indicate an error and 10 indicates correct performance.

	M1	M2	M3	M4	M5	M6	M7
W μm	2	26	2	5.9	2	2	4
L μm	3	2	2	2	2	6	3

Table 1. Checker transistor sizing.

It must be noted that fault masking can occur for multiple faults, although the likelihood of these faults is very low. For example, a multiple fault can result in several unbalanced signals but which cancel each other in the checker, thus leaving the currents in nodes Vc and Vc' unchanged. For this limit case of multiple fault, an off-line test procedure scanning each differential node individually would detect the fault.

Finally, in order to ensure the TSC goal, an off-line testing phase is required for testing the checker. For example, a fault at any of the two outputs of the checker that behaves like a stuck-at may not be detected if the circuit under test is not faulty. Therefore, similarly to [11], a test phase which periodically applies unbalanced signals to the checker is used to ensure the TSC goal.

5 Analogue fault coverage

This section is devoted to step 4 of the CED design methodology introduced in section 3. We show out how faults affect the circuit behaviour, how these faults are detected by the checking circuitry, and the hard and soft fault coverages achieved.

Generally speaking, each stage of a differential circuit consists of an active differential amplifier and some passive components. Without loss of generality, the second stage of the filter of figure 3 is considered here (a similar analysis can be applied to the other stage). The corresponding continous-time version of this stage is given in figure 5, where R5=R7=25MΩ and C6=C8=8pF. According to the discussion in section 2.1, when carrying out circuit hard/soft fault analysis, such modelling leads to a good coverage of faults occurring at the level of switches and capacitors.

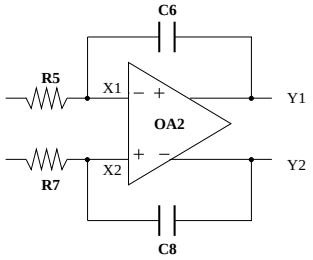


Figure 5. Modelling the second stage of the biquad for fault detection analysis.

In the case of single hard faults in the opamp, it has been shown [12] by fault simulation that 99% of faults can be detected by balance checking. Furthermore, for these faults, the functional circuit in which the opamp is inserted will achieve the TSC goal for the whole frequency spectrum. The remaining 1% of faults do not change at all the amplifier behaviour keeping the circuit in a fault-secure operation region.

For hard faults in passive components, since the opamp is fault-free due to the single fault assumption, the circuit DC operating point does not change and the circuit never saturates. These faults are then analysed in the AC domain. The effects of these faults on the overall circuit transfer function and on the sensing node X are shown in figures 6(a) and 6(b), respectively. It must be noted that faults in oppositely situated components (R5/R7 and C6/C8) are equivalent from the point of view of the effect on the transfer function and the magnitude of the common-mode signal [9].

For example, a short in R5 (which is equivalent to an open in C6) is undetected for frequencies lower than 100Hz. However, the functionality of the circuit is not affected in this frequency band (fault-secure). For frequencies larger than a few hundred Hertz, the functionality of the circuit is altered but the fault is detected

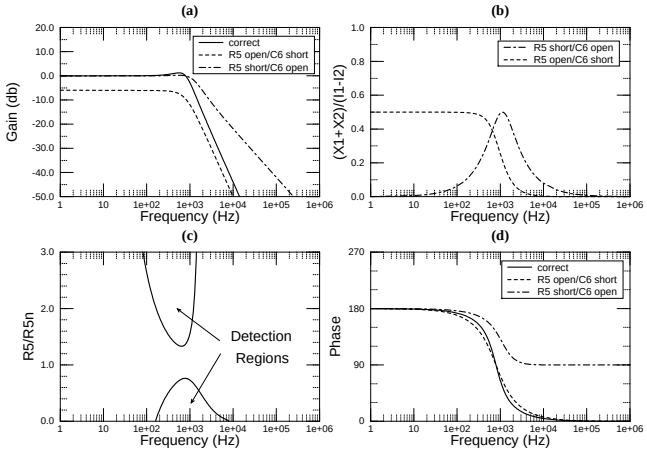


Figure 6. Effect of hard faults: (a) on circuit gain, (b) on balance node X, (c) fault detection boundary for R5, and (d) on circuit phase.

in the checker since a common-mode signal larger than 100mV is generated. Finally, for large frequencies, the fault is undetected but the gains are so small that the circuit output is practically the same for the fault-free and the faulty circuit. A similar analysis can be done for an open in R5 (which is equivalent to a short in C6).

In the case of soft faults, deviations of the same amount for each one of the four passive components (R5, C6, R7 and C8) have the same effect on the balance of node X and on the circuit transfer function. The same analysis shown for hard faults in figures 6(a) and 6(b) can be repeated for soft faults. The result is the same: once the soft fault significantly affects the transfer function (as determined below) the checker observes a common-mode signal which generates an error.

The soft fault coverage is determined by considering the definition of fault detection boundary in section 2.1. The soft fault detection boundary for a component is obtained by determining the minimum deviations which generate a common-mode signal of 100mV at each circuit frequency. The fault detection boundary for component R5 (which is the same for the other components) is shown in figure 6(c). The boundary extends along both sides of the nominal value (R5/R5n=1) which corresponds to positive and negative component deviations. The area between the boundaries corresponds to a region of non-detection. From figure 6(c), it can be seen that a fault for a passive component in the second stage with nominal value Pn is detected if $P/P_n > 1.34$ or $P/P_n < 0.76$, e.g. for those parameter deviations the finitely self-testing property is ensured. It must be noted that for higher input voltages (a differential input of 1V was considered in this example) the region of undetectability becomes narrower (considering that the amplifiers do not reach saturation) and

the soft fault coverage can become larger.

Note that the analysis done for the effect of hard faults on circuit gain can be repeated for the effect of hard faults on circuit phase (figure 6(d)) and it leads to the same conclusions above drawn.

Given this context, we can conclude that the TSC goal cannot be ensured for the whole frequency spectrum, but it is achieved for the range of frequencies of interest to the circuit operation. The other operation regions are not self-checking, because the fault-secure property is not ensured and the erroneous circuit behaviour is not accompanied by an error indication provided by the checker.

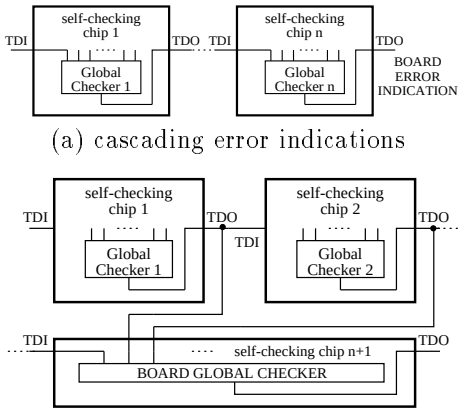
Nevertheless, due to the small gain for the non-fault-secure frequencies of the case-study circuit, the filter operation is likely to be considered safe for most applications. For example, assuming an input of 1V and a frequency of 8kHz, the fault-free circuit would give an output of 10mV, while an output of 100mV would be obtained for an R5 short (figure 6). Although this difference may seem large, one should note that the checker is designed to tolerate 100mV common-mode signals!. Since in general the finitely self-testing property is achieved, a periodical off-line testing phase will be capable of detecting those non-dangerous faults and will prevent that the accumulation of faults leads to the loss of the circuit safety.

6 CED in mixed-signal boards

The extension of the CED from circuits to the board level becomes a must when the goal is to design systems for high safety applications.

In [13] this kind of extension is proposed for digital boards by merging self-checking and BIST circuit level techniques with the boundary scan board level approach (IEEE Std. 1149.1, [7]). This proposal is based on the fact that the boundary scan path is not used during the normal operation of the board, thus being available for carrying the on-line error indications of the circuits. Three different approaches – fitting different application speed requirements – are used for compressing and propagating the circuit error indications across the board. Two of them are presented in figure 7: the cascading of error indications through the circuit global checkers and their parallel verification by means of a board global checker. The third approach, named mixed, simply merges the previous ones by verifying in parallel error indications of cascading branches. Finally, the board interconnects are encoded and on-line tested by built-in checkers placed at circuit input interfaces; these checkers are in charge of verifying the codes associated with the data flowing from one circuit to another in the board.

One of the basic guidelines of IEEE P1149.4 Mixed-Signal Test Bus Standard [14] is to maintain compatibility with IEEE Std. 1149.1. Taking this into account and the fact that our analogue checker provides a digital double-rail encoded error indication, an on-line testable mixed-signal circuit, like the one shown in figure 8, will comply with the scheme of figure 7 with respect to the compression/propagation of error indications.



(a) cascading error indications

(b) parallel verification of error indications

Figure 7. Self-checking board.

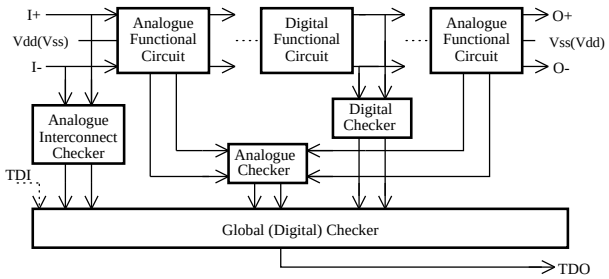


Figure 8. On-line testable mixed-signal circuit.

With respect to the concurrent error detection on the board interconnects, in order to have the diagnosis resolution required at the board level, the interconnects should not be monitored by the same checker associated with the analogue functional circuits.

It is easy to show that a short beween two symmetrical nodes n_{i+} and n_{i-} could never be detected by balance checking. The only behavioural change would be observed as a reduction in signal amplitude that would be, however, symmetrical. The occurrence of these faults can be prevented if an appropriate board layout rule is adopted:

"Two differential nodes n_{i+} and n_{i-} (which carry complementary information about a signal S) should never be laid down very close to each other. They must be separated, whenever possible, by an equidistant wire connected to a potential different from the analogue ground, e.g. one of the power supply rails."

A single short between one node (let us say n_{i-}) and this wire would thus cause an asymmetry of the differential node potentials $v(n_{i+})$ and $v(n_{i-})$. Since the geometrical symmetry is preserved, the noise injection from the wire parasitic elements into the signal wires will be identical and appear as a small common-mode signal rejected by the following circuit stages.

Therefore, we propose that the power supply pins and wires (V_{dd} and V_{ss}) are used to separate I_+ and I_-, O_+ and O_- (figure 8), everywhere in the board, in order to cope with the design for on-line testability rule presented above at the same time that the circuit pin counting is kept at a minimum.

7 Conclusion

This paper describes an attempt to formally analyse the faulty behaviour of analogue differential circuits along with a methodology for on-line testing which is kept simple enough and transparent to the final user with respect to the theory which supports it.

Besides the methodology itself, other novelties brought in by this work are:

- the use of a simple on-line analogue checker capable of monitoring several circuit stages at the same time and of providing a digital error indication;
- the simultaneous study of both the hard and soft faults of components external to operational amplifiers and the hard faults of operational amplifier transistors;
- the definition of the operation regions (in terms of signal amplitudes, frequencies, the acceptable deviation of the transfer function, the checker tolerance window and types of faults) in which the totally self-checking goal can be achieved by balance checking; and,
- the extension of the differential circuit test approach to on-line checking of mixed-signal boards.

The AMS 1.2μm double-metal double-poly process was chosen for the implementation of the analogue circuit studied in this paper. The chip that we have recently sent for fabrication is composed of 12 copies of the filter: some with and others without the checker, some fault-free and other faulty. The goal is to evaluate both the fault coverage and the circuit performance degradation (given that the operational amplifier input transistors are 333 times larger than those of the checker, a negligible performance degradation is expected). Figure 9 shows the layout of the on-line testable biquadratic filter. The analogue checker takes only 3% of the 0.5mm^2 total circuit surface.

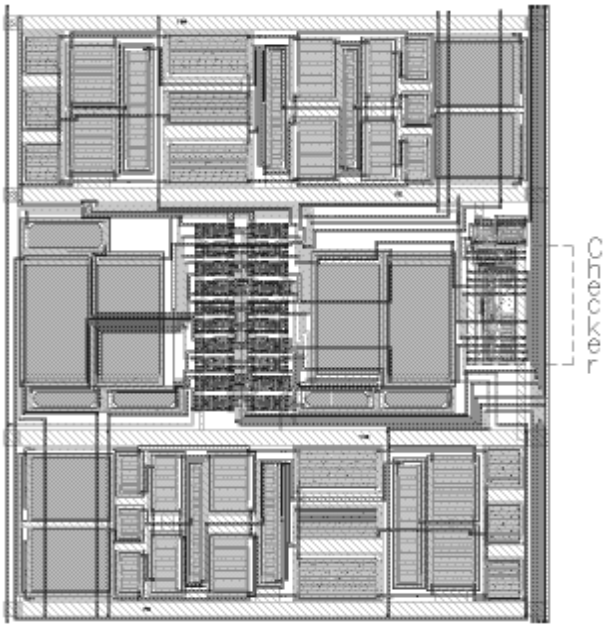


Figure 9. On-line testable biquad filter.

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