LDO-assisted Voltage Selector over 0.5-to-1V VDD range for fine Grained DVS in FDSOI 28nm with 200ns/V Controlled Transition

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***Abstract*—This paper presents a 95% power-efficient duty-cycled LDO-assisted voltage selector (LAVS) for fine grained spatial and temporal voltage scaling in FDSOI 28nm technology. LAVS enables 200ns/V controlled transitions between three power rails over a 0.5-to-1V range while maintaining the digital activity of the supplied load. During transitions, current and voltage detections are proposed to protect power rails from reverse current. LAVS has a 13% Si area overhead to drive a 0.2mm^2 digital load. Thanks to a 100MHz-bandwidth LDO, which is only enabled during transition to save power consumption, the voltage selector also maintains a smooth voltage transition even if a digital load suddenly changes its activity factor (4mV/mA load transient). LAVS achieves 30pJ energy dissipation per voltage transition which is negligible compared to the power consumed by the digital load (50mW@0.2mm^2). This therefore allows a MHz dynamic voltage scaling rate.**

Keywords— Voltage Selector, LDO, Dynamic Voltage Scaling, Voltage Regulator, FDSOI.

I. INTRODUCTION

Dynamic voltage scaling (DVS) is a conventional solution to reduce the energy dissipation of digital circuits by dynamically adjusting the digital power supply in order to find the best trade-off between energy dissipation and calculation speed for a given workload requirement. In addition, a high-performance computing processor is now divided into multiple cores which operate at different frequencies and where their individual workload changes dynamically. The power tree therefore has to be reviewed to address each core.

One off-chip power supply per island is a costly solution to set the best energy point of each core. Therefore, to reduce the PCB surface area, BoM (Bill of Materials) and allow rapid V_{DD} switching, fine grained DVS can be done using multiple on-die DC-DC converters (no external component needed) as suggested in [1-3] and shown in Figure 1. However, their low-power densities (10's of mW/mm^2 in deep CMOS technology) compared to the digital power density (10's of W/mm^2) has negated the benefits of a fully-integrated power tree due to its costly silicon overhead. The low density is mainly due to the low quality of on-chip inductor and capacitor compared to their off-chip counterparts [4]. Furthermore, an external DC-DC converter is still needed to step-down the available DC-bus voltage e.g. 12V to an admissible level i.e. 1.8V in order not to operate the switching transistors of on-chip converters at a higher rate than the voltage rating of the chosen CMOS technology [5].

Awaiting the ultimate power-tree CMOS integration, [6] proposes a reasonable trade-off between PCB and Si area saving where only power-rail selectors are integrated in the digital die to address individual power islands from a discrete set of shared external converters. Fig. 1 shows the typical power chain for M digital cores. M dedicated voltage selectors are fully integrated on chip which selects the optimal voltage V_{CORE} for a given core's workload requirement between N V_{DD} (N<M). The N V_{DD} power rails are generated from N off-chip shared DC-DC converters. [7] shows that just three different V_{DD} (N=3) are sufficient for near-ideal minimal energy point tracking over a large targeted operating frequency range. In this way, a power tree with only three external power supplies allows fine grained DVS for a multiple-core digital system. The benefit of this solution is the higher power density of on-chip voltage selectors compared to on-chip DC-DC converters as by nature, they do not need any flying passive components.

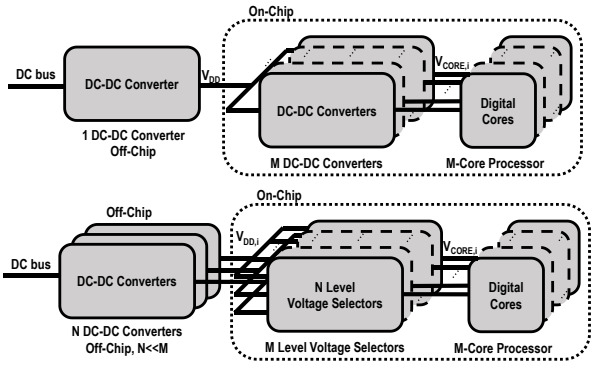

Fig. 1. Power-Tree Integration in a Multicore Processor using Independent Voltage Domains for Fine Grained DVS.

However, the *hot switching*, i.e. V_{CORE} switching when the digital core remains active, is challenging. If the power paths are not controlled, some cross-currents between $V_{DD,i}$ occur and the V_{CORE} slew rate depends on the digital activity and power network. To avoid turning off the digital core at each V_{CORE} transition, we propose a topology called LAVS by assisting the power-rail selector using a linear regulator (LDO). By using LAVS, the V_{CORE} transition is controlled while both

maintaining digital activity and preserving it from a cross-current between different voltage rails V_{DD},i. In the following sections, the LAVS topology and sequencing are described, and then the experimental results are discussed and compared to the state-of-the-art.

II. VOLTAGE SELECTOR TOPOLOGY

A. LAVS System Overview

The LAVS topology is shown in Figure 2. It is composed of a fully-integrated voltage selector which selects the core voltage V_{CORE} between three shared voltage rails $\{V_L,V_M,V_H\}$ generated from an external DC-DC converter (out of the scope of this paper) in the range of 0.5-1V. Digital word SEL [1-2] selects the input voltage and a TR edge starts the voltage transitions (synchronized with external clock). The aim is to maintain a constant voltage slew rate (200ns/V) under any condition (voltage, activity factor, etc.) and a less than 5% DC voltage drop at full load (50mA@1V) outside transitions. LAVS is composed of three LDO-assisted power-switches M_i, a voltage ramp generator, a 100ns delay block, shared current/voltage-mode comparator and a digital state machine. A single LAVS was conceived to drive a 0.2mm^2 digital core (400pF equivalent load on the V_{CORE} node) and fully integrated in 28nm FDSOI technology with no external component. Multiple LAVS can be distributed to drive individual 0.2mm^2 power islands.

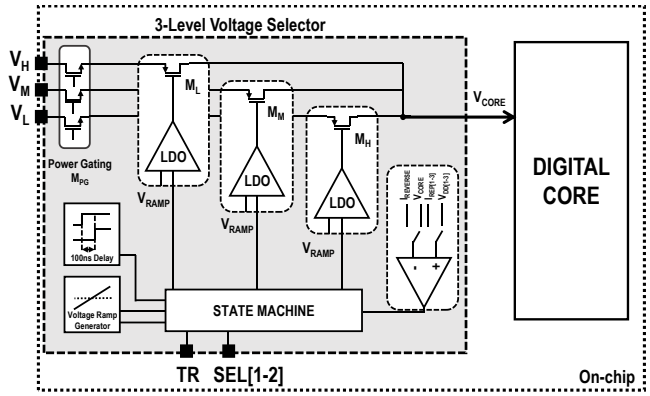

Fig. 2. Proposed 3 power-rail LDO-assisted Voltage Selector.

During transitions, the selected power switch acts as an LDO by using a super source follower structure (Section III) so the V_{CORE} follows V_{RAMP} in order to enforce the V_{CORE} slew rate. The LDO bandwidth maintains a 4Ω output impedance at 100MHz, thus preserving V_{CORE} from over/undershoot when the load current varies suddenly during voltage transitions.

To provide current leakage reduction in power gating mode, thick-oxide transistors $M_{PG,i}$ have been introduced in series with thin-oxide transistors M_i. The equivalent on-state resistance of M_i in series with M_{PG} is 1Ω worst case (125°C, worst process corner) outside the voltage transition in order to have less than a 50mV voltage drop when one V_i rail is selected.

B. Switching Sequencing

Figure 3 shows the sequencing for up- and down-voltage transitions between V_H and V_L. The TR digital signal triggers the beginning of the transition, starting the voltage ramp and the delay blocks.

If the up-transition is selected, the SW_H transistor toggles in LDO mode (super source follower mode) and SW_L transistor is still turn-on. To prevent cross-current between V_L and V_H, the current through SW_H is checked by turning on the comparator in current-mode, called CM-C, a topology which will be described later. At t_{RM}, the CM-C detects that the current I_L is negative, and so a charge flows towards V_L meaning V_L begins to receive energy. Then, the state machine turns off SW_L to stop the reverse current. Between t_{RM} and t_{RH}, SW_H is still in LDO mode to continuously turn on the path between V_H and V_{CORE} with a controlled slew rate (see later). The comparator is only activated between t_{RL} and t_{RM} to save power consumption when no transition occurs.

In a down-transition, SW_H switches from on-state to LDO mode (pull-down mode) until V_{CORE} reaches $V_L+\Delta V_L$ where ΔV_L=10mV. At t_{FL}, SW_H is turned off and SW_L is enabled in order to connect V_{CORE} to the final voltage V_L. Now, the shared comparator acts as a voltage comparator between t_{FH} and t_{FL} and is disabled outside.

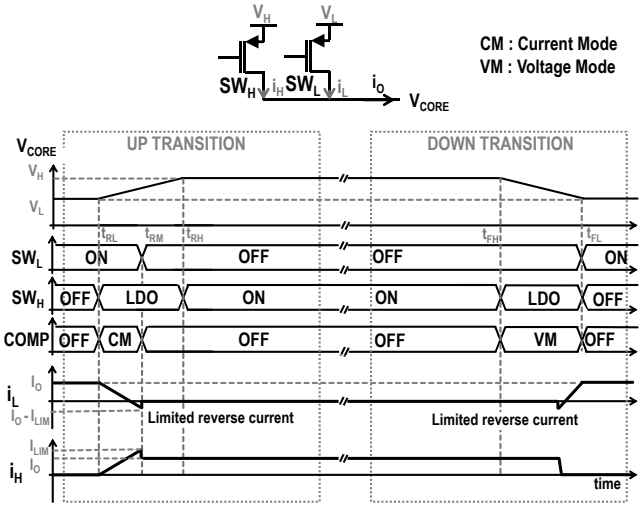

Fig. 3. Sequencing during up- and down-Transitions.

C. Energy Consumption during Voltage Transition

The energy cost of one transition has to be minimized to allow a high voltage transition rate and thus a better dynamic energy point tracking for each digital core. During the voltage transitions which last less than 100ns, LAVS consumes 300µW on average. Therefore, it costs less than 30pJ per transition which is negligible compared to a digital load activity (50mW@1V), if the voltage switching rate is lower to 10's of MHz. Outside the voltage transition, the LDO control and comparator are turned off to save quiescent power. When V_{CORE} is maintained on a voltage rail, LAVS shows a 32µW power consumption, less than 1% of the driven digital core. In sleep mode, i.e. no DVS is needed, LAVS consumes less than 3µW.

III. IMPLEMENTATION

Figure 4 shows the schematic of the voltage selector connected to the higher voltage rail V_H. The power switch M_H is driven by a super source follower (SSF) topology. During an

up-transition, M_{SSF} is biased by the ramp voltage and shifted by one threshold voltage. Then, the ramp generator is precharged to V_{CORE}-V_{TH} at the beginning of the transition to start the LDO reference voltage at V_{CORE} at the beginning of the transition. M_{SSF} derives negligible current (<100nA) from the digital core if $V_{CORE}<V_{RAMP}-V_{TH}$ to set V_{BIAS} and then modulate $V_{G,H}$ to set the voltage slew rate. There are two current sources (I=50µA) and a cascade transistor link V_{BIAS} to $V_{G,H}$. When V_{CORE} pulls up to V_H, $V_{G,H}$ is pulled down to zero in order to achieve the lowest on-state resistance for M_H. During down-transitions (pull-down mode), M_{PD} is connected to the ramp voltage and pulls down V_{CORE} if the core voltage decreases at a lower rate than the required slew rate (200nV/s) due to a low digital activity factor. R_{PD} is sized to ensure a discharge of 400pF equivalent core capacitor in 100ns. Outside down-transitions, M_{PD} is disabled.

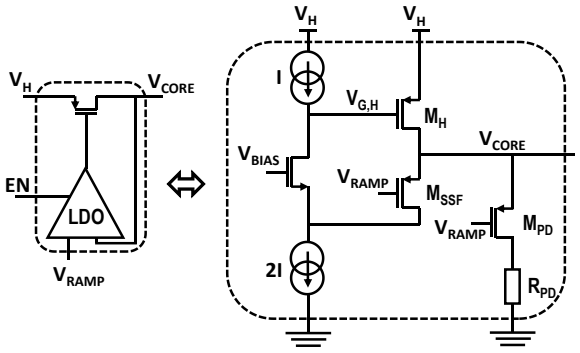

Fig. 4. Voltage Switches assisted by LDO during transitions.

Figure 5 shows the shared comparator composed of a fully-differential amplifier and second-stage folded-cascade operational amplifier followed by a Schmitt trigger. During the up- and down-transitions, LAVS power consumption is 300µ and 240µA, respectively. The comparison is made in a 2ns delay and 2mV offset at 3σ. In voltage mode, V_{CORE} is compared to the final desired voltage. In current mode, a voltage is generated by the reference current I_{REF} and the measured reverse current which are then compared.

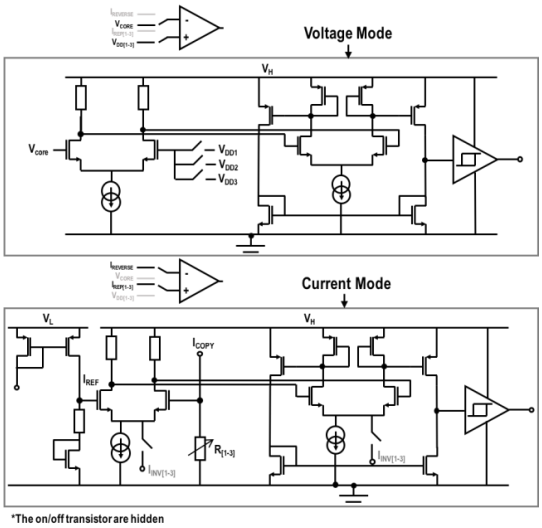

Fig. 5. Shared Comparator: Voltage and Current Mode.

The LAVS with an associated 0.2mm^2 digital core has been fabricated in FDSOI 28nm technology (Fig. 6). Three power rails (0.5, 0.75 and 1V) are received from three external DC-DC converters. The digital core is composed of a set of representative gates i.e. critical path replica, to mimic real digital core activity. The die area of LAVS is 0.027mm^2 (0.045mm^2 with power gating transistors) corresponding to 13% of the digital core area. No external component is needed e.g. no decoupling cap on the V_{CORE} node.

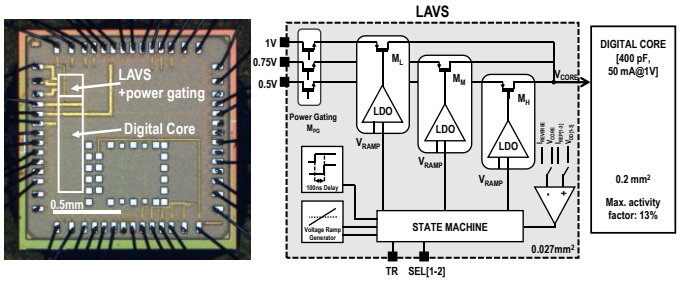

Fig. 6. LAVS with its Digital Load and Die Photograph.

IV. Measurement Results

The LAVS has been measured during up- and down-transitions for different workload conditions i.e. constant and variable activity factors. In Figure 7, the down-transition from 0.75-to-0.5V (V_M to V_L) shows a linear decrease of the V_{CORE} with a controlled 200ns/V slew-rate with only 15mV dynamic undershoot below V_L. The digital load has a constant 13% activity factor corresponding to a current variation of 21mA@0.75V and 4mA@0.5V. The transition lasts 50ns and costs 15pJ.

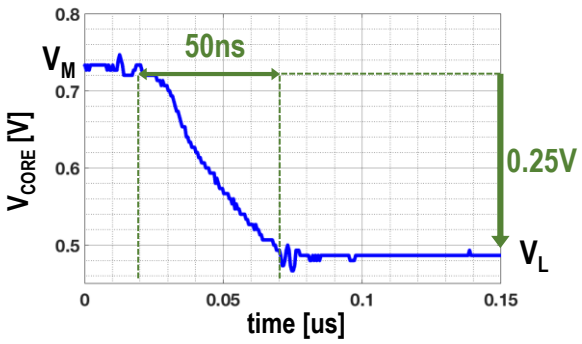

Fig. 7. Core Voltage during down-Transitions with Constant Activity Factor.

The up-transition from 0.75-to-1V is shown in Figure 8 where the digital load still has a constant activity factor i.e. 21-to-50mA current variation. The transition lasts 50ns thanks to the controlled slew rate produced by the SW_H in LDO operation (pull-down mode). V_{CORE} is kept higher than 0.95V (1V minus 5%) when the digital core rail is connected to V_H with the maximum activity factor (I_{CORE}=50mA@V_H). The maximum reverse current (not shown in Fig. 8) provided from V_M is below 20mA during the voltage transition.

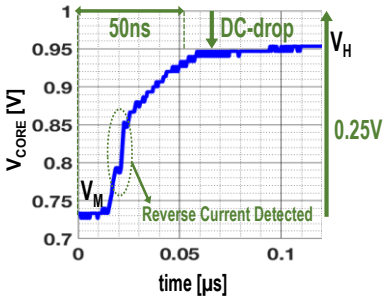

Fig. 8. Core Voltage during up-Transitions with Constant Activity Factor.

Figure 9 shows the V_H-to-V_L transition when the current varies from 0.3 to 50mA which mimics a workload variation. As SW_H acts as the LDO, a fast regulation is performed to smooth V_{CORE} due to the load transient whose equivalent is 4mV/mA (0.2V undershoot for a full current variation 0-to-50mA). The load transient response is measured without any extra decoupling capacitor on V_{CORE} (only the intrinsic 400pF of the digital load). LAVS maintains a minimal voltage operating point i.e. 0.5V to avoid blackout or timing violation in the digital load during the transition. The down-transition is done in 100ns equivalent to 200nV/s.

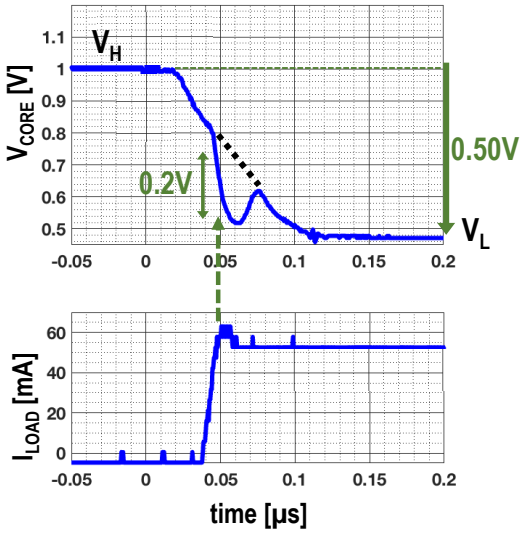

Fig. 9. Core Voltage during down-Transitions with Variable Activity Factor.

Table 1 compares the performance of the LAVS to the state-of-the-art. With a fully-integrated power tree option, the power density of our LAVS is two orders of magnitude higher than the best-in-class fully-integrated DC-DC converters in CMOS technologies without high-density capacitance options [1-3]. Compared to [4], we control the slew-rate i.e. 200ns/V of the voltage transition while maintaining sub-µs transition time and low area overhead (13% of digital load area) without turning off the load during transition.

TABLE I. COMPARISON WITH STATE-OF-THE-ART

Metric	[1]	[2]	[3]	This Work
Technology	22nm FinFET	28nm FDSOI	28nm FDSOI	28nm FDSOI
Digital System	Graphics core	Processor	Processor	**Multicore processor**
Technique	LDO/SC	SC	Simultaneous SC	**Voltage Selector**
Input Voltage	0.65 – 1.05	1.8	1, 1.8	**[0.5-1.0] x 3 rails**
Output Voltage	0.38 – 0.92	0.2 – 1.1	0.5, 0.67, 0.9	**[0.5-1.0] x 3 rails**
Slow-rate [ns/V]	-	134	**60***	200
Efficiency. Maximum power density [W/mm^2]	-	0.27	0.3	**5 without power gating**
Maximum load power [mW]	-	**196***	65	50
Quoted efficiency [%]	73 (SC), 84 (LDO)	72.5	80-86	**>95** (measured value)**

SC: Switched-Capacitor Converter
*extract from paper results.**An ideal voltage converter assumed in the voltage selector inputs.

V. CONCLUSION

We have demonstrated a compact and efficient 3-level voltage selector over 0.5 to 1V which acts as an LDO during the transition in FDSOI 28nm to perform fine grained DVS. The high-power density (5W/mm^2) and power efficiency (>95%) of LAVS compared to on-die DC-DC converters allows fine spatial DVS granularity with a small number of external DC-DC converters (here, three). The controlled 200ns/V slew-rate and 30pJ/transition also allow fine temporal DVS granularity i.e. 10's of MHz DVS rate. The digital core power rails can be switched by maintaining the digital activity which allows *hot switching*. The LAVS power consumption in active mode corresponds to 0.1% of the digital load contribution which thus enables a seamless integration in many distinct power regions.

REFERENCES

[1] S.T. Kim et al., "Enabling wide autonomous DVFS in a 22nm graphics execution core using a digitally controlled hybrid LDO/switched-capacitor VR with fast droop mitigation," *IEEE International Solid-State Circuits Conference*, p. 154–155, 2015.

[2] T. Souvignet et al., "A Fully Integrated Switched-Capacitor Regulator With Frequency Modulation Control in 28-nm FDSOI," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4984-4994, 2016.

[3] B. Zimmer et al., "A RISC-V Vector Processor With Simultaneous-Switching Switched-Capacitor DC-DC Converters in 28 nm FDSOI," *IEEE Journal of Solid State Circuits*, vol. 51, no. 4, pp. 930-942, 2016.

[4] Y. Pascal et al., "Efficiency Comparison of Inductor-, Capacitor-, and Resonant-Based Converters Fully Integrated in CMOS Technology," *IEEE Journal of Emerging Technology on Circuits and Systems*, vol. 5, no. 3, pp. 421-429, 2015

[5] G. Pillonnet et al., "Effect of CMOS Technology Scaling on Fully-Integrated Power Supply Efficiency," *IEEE International Conference on Integrated Power Electronics Systems*, 2016

[6] K. Craig et al., "A 32 b 90 nm Processor Implementing Panoptic DVS Achieving Energy Efficient Operation From Sub-Threshold to High Performance," *IEEE Journal of Solid State Circuits*, vol. 49, no. 2, pp. 545-552, 2014.

[7] Y. Akgul, "Energy-efficient control through power mode placement with discrete DVFS and Body Bias," *New Circuits and Systems Conference*, 2015