

Low energy switch block for FPGAs

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Low Energy Switch Block For FPGAs

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Abstract—We propose a new energy efficient method of designing switch blocks inside FPGAs using novel variations of the Dual Threshold CMOS (DTMOS) based switches instead of the conventional NMOS pass transistor or tri-state buffer based switches. By intelligently sharing the extra transistor needed for using DTMOS based switches, the area overhead is kept to a minimum. Sleep transistors are used to reduce sub-threshold leakage. Using our new, novel design, we obtain a 16% improvement in the power-delay product during the active mode per switch and a factor of 20 improvement in the stand-by mode, over conventional approaches. Extensive simulation results over benchmark circuits in CMOS 0.13 μ are presented to illustrate the superiority of the proposed techniques. Since the proposed techniques target the switches and multiplexers which are present in large numbers on FPGAs, the overall improvement in the power-delay product is significant for an application implemented on a FPGA having the proposed features.

I. INTRODUCTION

In the deep-submicron era, the usage of sub-wavelength lithography has made mask costs prohibitively expensive. It is expected to reach 2 million dollars for the 65 nm node. Against such a backdrop, the usage of field programmable gate arrays or FPGAs is rapidly gaining popularity, since they offer a tremendous advantage of hardware programmability. Also, the cost of a single mask set could be amortized over many different applications, making FPGAs cost effective. But there are many challenges in the field of FPGA design.

Hardware programmability and flexibility comes at the cost of having a switch dominated interconnect, which is responsible for most of the power consumed on FPGAs. Due to these limitations, orders of magnitude difference exists between FPGAs and ASICs in the power and delay figures[7]. Fig.1 shows the results of a study done on a state of the art FPGA, 0.15 μ Virtex II family from Xilinx[10]. The figure shows that the interconnect is the dominant energy consumer, with hex lines, double lines and long lines accounting for most of the power consumed.

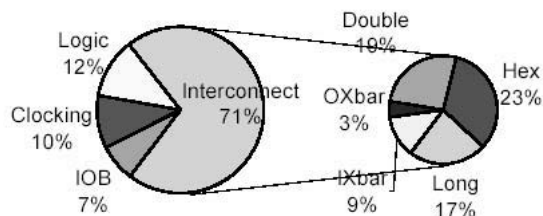


Fig. 1. Energy dissipation constituents

Interconnect accounts for greater than 70% of the energy consumed on all FPGAs. Thus, if the energy consumed by the interconnect is reduced, it would contribute greatly to a reduction in the overall energy consumed by FPGAs.

In the past switch block architectures for improving routability have been extensively studied. But the circuit design of the switch block for low power and high speed itself has received very little attention. The basic switches in the switch block were always assumed to be NMOS based or tri-state buffer based.

The work in [3] focuses on the introduction of a new switch box architecture for improving routability, but does not explore circuit implementation aspects of the switch box itself.

In [4] four issues are investigated: the circuit design of pass transistor and tri-state buffer routing switches, the best transistor sizes to use in both types of switch, how routing wires should be laid out (what metal width and spacing is best?), and electrically-heterogeneous FPGAs, in which some routing wires are tuned for density and some for speed.

In [5], [8], the techniques employed by Xilinx are described. Xilinx uses gate boosting technique to reduce the power dissipation in pass transistor based switches. The basic switch is assumed to be either NMOS pass transistor based or more recently tri-state buffer based. The conventional switch blocks are as shown in Fig.2. To overcome the threshold drop problem in pass transistor based switches, gate boosting is used where the gate voltage of the pass transistors is one threshold above the supply.

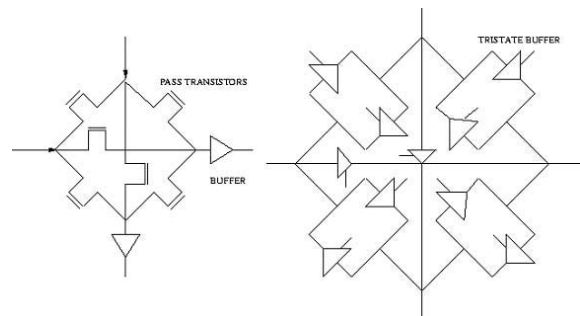


Fig. 2. Conventional Switch Block

Though the gate-boosting technique solves the problem of DC power dissipation, it has the following main disadvantages

- 1) To prevent damage to the pass transistor switches, normally thicker gate-oxide transistors have to be used otherwise device reliability problems arise in 0.18 μ m and below due to the thin gate oxides.
- 2) Since the gate input to the pass switch comes mostly from a SRAM based memory, gate boosting has implications on the configuration memory design as well

Recent architectures from Xilinx [5] and the Altera Stratix architecture [9] make use of buffers to eliminate the problem of static power dissipation in pass transistor switches. However, this approach has two main disadvantages. Replacing all pass transistor

switches with tri-state buffers yields a design with significant increase in area and power consumption. To reduce these problems, pass transistor switches are only partially replaced by buffers (on delay-critical paths for example). Other approaches compromise the point to point routability of the interconnect fabric by using dedicated short interconnect [5] or uni-directional buffers like DirectDrive in [9]. This reduction in routing flexibility over certain interconnect paths is overcome by providing more interconnect resources or larger channel widths [9] so that the overall routability of the design is ensured.

We show through our work, that there are methods other than replacing pass switches by buffers for reducing energy consumption without compromising routability. The proposed method using novel configurations of Dual Threshold MOS based switches overcomes many disadvantages mentioned above at a minimal increase in area. Though the basic operation of a DTMOS based switch in itself is well known [6], the novelty of our work lies in the variations over the basic concept and its applicability to the design of switch blocks in FPGAs. Another challenge faced by designers, with shrinking process technologies, is stand-by leakage in FPGAs. Reducing stand-by leakage has been addressed in [8] using software to turn-off series sleep transistor switches. Our approach also addresses the issue of reducing leakage in switch blocks.

Also through our work, we illustrate the type of switch configuration that needs to be chosen for meeting different performance constraints. For example, we make the main transistor(MT) of the DTMOS switch a high V_T transistor. So during the active mode of operation, the high V_T is reduced due to the body-source forward bias and during stand-by when the body-source voltage is zero, the threshold voltage is equal to the intrinsic high V_T of the MT. This reduces sub-threshold leakage power dissipation while maintaining an acceptable active power-delay product. So we can trade-off stand-by leakage versus active power-delay product using this variation. We propose other variations and study the trade-offs possible. It was shown in [1] that by using the encoded-low swing technique upto 40% improvement in power-delay product over schemes using low-swing alone and 70% improvement in the power-delay product over the schemes using encoding alone can be achieved. Combining the encoded-low swing technique with Dual Threshold MOS based switches in different configurations, a tremendous reduction in energy consumed over the interconnect can be obtained.

The rest of the paper is organised as follows. Firstly, a brief insight into the operation of the Dual Threshold MOS(DTMOS) switch is presented. Proposed variations of the basic DTMOS structure are then discussed. Then, an exhaustive comparison with conventional switches in power, delay and power-delay is presented. Also the trade-offs involved in choosing a switch are illustrated. Finally the conclusions are given. All the simulations are based on CMOS 0.13 μ process and are done using a transistor level simulator.

II. DTMOS OPERATION

Programmable interconnect consists of connection and switch blocks. A logic block input or output can connect to some or all of the wiring segments in the channel adjacent to it via a connection block of programmable switches. At every intersection of a horizontal and a vertical channel there is a switch block[2].

Instead of using the conventional NMOS based pass transistor switch, we use variations of the Dual Threshold MOS(DTMOS) based switch.

A. Basic operation of DTMOS switch

First the basic operation of the DTMOS switch is explained. The threshold voltage of a transistor can be expressed as

$$V_T = V_X + K\sqrt{V_{sb} + 2\phi_f} \quad (1)$$

$$V_{T0} = V_X + K\sqrt{2\phi_f} \quad (2)$$

The terms in these formulae are as follows. V_X is the process-related constant threshold voltage term, V_{T0} is the threshold voltage V_T at $V_{sb} = 0V$, K is a process parameter equal to $\frac{1}{C_{ox}}\sqrt{2N_A q\epsilon_0\epsilon_{si}}$ and is also known as the K-factor, N_A is the substrate dope concentration, V_{sb} is the source-bulk voltage and $2\phi_f$ is the band bending where inversion first occurs. It can be seen from Eqn.1 that we can vary the threshold voltage by varying the source bulk voltage. When a negative back bias voltage is applied to the bulk wrt the source, in the case of a NMOS transistor, the depletion region of the channel substrate junction increases, and the voltage needed to create inversion also increases. Thus the threshold voltage increases. When the bulk source voltage is positive, the threshold voltage of the NMOS transistor reduces. The DTMOS transistor uses this basic principle.

The DTMOS transistor in its basic form has the gate and the body terminals shorted as shown in Fig.3

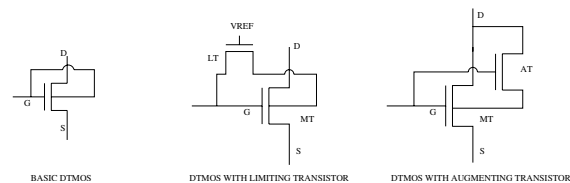


Fig. 3. DTMOS with limiting and augmenting switch

During the active mode of operation, when the gate voltage is positive, the body source junction has a forward bias. Since the body source voltage (V_{bs}) is positive, the threshold voltage reduces during the active mode of operation. When the gate voltage is zero (or the switch is not used), the body source voltage is zero and the DTMOS switch has a threshold equal to V_{T0} shown in Eqn.2. This gives the DTMOS based switch an advantage over the conventional NMOS switch. During the active mode of operation when the gate voltage of the main transistor is high, its threshold voltage is reduced. This makes the DTMOS based switch faster than the NMOS based switch. It also has a higher current drive due to reduced V_T .

The disadvantage of using the DTMOS in its basic form is that the gate voltage swing cannot exceed the cut-in voltage of the diode(0.5V) otherwise a large current would flow through the forward biased body-source and body-drain junctions.

B. DTMOS with limiting and augmenting transistor

To overcome 0.5V limitation of the DTMOS switch, some variations have been proposed in literature[6]. The variations are shown in Fig.3. With these variations the DTMOS switch can work upto the full swing voltage(1.2V in 0.13 μ process).

The DTMOS with the limiting transistor works as follows. As shown in Fig.3, there are two NMOS transistors namely MT(main transistor) and LT(limiting transistor). The gate of the LT is connected to a reference voltage supply (VREF). So the voltage at the body of the MT never exceeds $V_{REF} - V_T$. For the body source voltage not to exceed 0.5V, VREF should be appropriately chosen. For 0.13 μ

process, the nominal V_T is around 300mV, so VREF can range from 0.8V to 0.4V. This prevents the body source voltage from exceeding 0.5V at all times.

The DTMOS with the augmenting transistor works as follows. The DTMOS with the augmenting switch contains two transistors namely MT(main transistor) and AT(augmenting transistor). When the gate voltage of the MT is high, and the source voltage is high, the voltage at the body of the MT cannot exceed $V_{DD}-V_T$ due to the V_T drop across the MT. So the body source voltage of the MT cannot exceed $V_T(0.3V)$ which is less than the cut-in voltage($>0.5V$) of the body source diode junction. So if the MT of the augmenting DTMOS switch is a high V_t transistor, then the body-source voltage is higher than when the MT is a nominal or a low V_t transistor. Thus the threshold voltage of the augmenting DTMOS switch with a high V_t MT is less than that of the same switch with a nominal or a low V_t MT. The current drive of the augmenting DTMOS switch with a high V_t MT is high and the delay is less, but as expected the power consumption is more. This is confirmed in our simulations as well.

Thus, it can be seen that the basic DTMOS with the limiting or augmenting transistor enable it to be used for gate voltages higher than 0.5V.

III. PROPOSED VARIATIONS OF DTMOS BASED SWITCH

We propose many variations of the basic DTMOS based switch to achieve the lowest active energy consumption and least leakage in stand-by. Acronyms used to depict the various configurations (or variations) are explained briefly here.

In Table.I we explain whether the transistors we use, main transistor(MT), limiting transistor(LT), augmenting transistor(AT) in a particular variation are high, nominal or low V_T and whether we use a sleep transistor in the buffer following the switch box or not. We evaluate the performance of DTMOS based switch when the main transistor is high V_T . We experiment with this for both augmenting and limiting DTMOS switches. We measure the active power dissipation and also the stand-by power dissipation for all the variations. To reduce the stand-by power dissipation, we use a high V_T sleep transistor in some variations.

TABLE I
VARIATIONS OF DTMOS USED IN OUR EXPERIMENTS

Configuration name	MT	LT	AT	Sleep transistor
A	Nominal	-	Nominal	-
AHVT	High	-	Nominal	-
ASW	Nominal	-	Nominal	High
ASWHVT	High	-	Nominal	High
L	Nominal	Nominal	-	-
LHVT	High	Nominal	-	-
LSW	Nominal	Nominal	-	High
LSWHVT	High	Nominal	-	High

A. DTMOS with augmenting switch and its variations

The DTMOS based switch with a limiter as shown in variation 1 needs to have a reference voltage supply(VREF). If the reference voltage supply is to be avoided we can use a DTMOS based switch with an augmenting transistor.

1) *Augmenting switch(A)*: In this variation, we use a nominal V_t augmented DTMOS with no sleep transistor. The “A” switch consumes more energy than the equivalent switch based on limiting transistor (L). The delay through the “A” switch is more since the augmenting transistor has some delay before the body source junction of the main transistor is forward biased, hence the overall energy

consumed is more. The stand-by power dissipation of the “A” switch is also worse than the other switches. This is confirmed in our simulation results as well which are shown later.

2) *Augmenting switch with high V_t main transistor (AHVT)*: As explained in the operation of the augmenting DTMOS switch, the threshold voltage during the active mode of this switch is lower than the A switch, thus resulting in a higher power consumption and lower delay after the body-source junction is slightly forward biased. Another factor which can contribute to this switch consuming more power is that, in the active mode, due to the high V_t MT, the delay through the MT increases which delays the forward biasing of the body source junction of the MT by the AT. This results in an increase in short circuit power dissipation of the buffer following the AHVT.

3) *Augmenting switch with high V_t main and sleep transistor (ASWHVT)*: A high V_t transistor in the augmented DTMOS switch with a high V_t sleep transistor is studied in this variation. The sleep transistor in the buffer increases the delay of this switch. The overall active energy consumed by this switch is more the other augmenting based DTMOS switches. But the leakage or stand-by dissipation is less.

4) *Augmenting switch with high V_t sleep transistor (ASW)*: This variation is similar to the ASWHVT but with a nominal V_t MT. Thus, the delay through this switch is less and the power consumed is also less than the ASWHVT. The overall the energy consumed is less than ASWHVT. The power consumed is lesser than ASWHVT because of two reasons. Firstly, the overall threshold is more than the that of the ASWHVT, leading to lesser current drive and lower power consumption. Secondly, the time before which the MT is forward biased is less than the ASWHVT.

B. DTMOS with limiting switch and its variations

The DTMOS with a limiting switch and its variations are on the whole faster than their counterparts of the DTMOS with augmenting switch and its variations. For eg. The L switch is faster than the A switch, the LHVT is faster than the AHVT, the LSW is faster than the ASW and the LSWHVT is faster than the ASWHVT.

The overall power consumed for the DTMOS with limiting switches is lesser than that of the DTMOS with augmenting switches. This could be because the short circuit power dissipation through the buffer is lesser for the former than for the latter because the V_t drop through the former switch is lesser than the latter. The delay is less because the body source junction of the MT is forward biased faster than the augmenting based switches. Another reason why the delay is less is because the body source forward bias(which contributes to the reduction in the threshold voltage of the MT) in the augmenting based switches cannot exceed V_t , but in the limiting switch it is the difference between V_{DD} and the reference voltage supply(VREF) and it is typically more than the threshold voltage V_t (In our case $V_{REF} = 0.8V$).

The limiting transistor(LT) has a dedicated reference supply VREF and the time taken for forward biasing the body-source junction of the MT is independent of the delay through the MT itself which was not the case for augmenting transistor based switches. The limiter transistor based switches have the disadvantage that an extra reference supply is needed. But if this can be afforded, then, the limiting transistor based DTMOS switches have the best energy figures compared to the other variations in our experiments.

1) *Limiting switch (L)*: The L switch has the lowest power-delay product compared to all other switches but suffers from a higher stand-by power dissipation.

2) *Limiting switch with high Vt main transistor (LHVT):* As expected, the LHVT consumes more power and has a higher delay than the L switch due to the high Vt MT. The overall power-delay product is more than the L.

3) *Limiting switch with high Vt sleep transistor (LSW):* The LSW switch has a higher energy consumption than the L and LHVT switches but less than the LSWHVT. This is expected since the sleep transistor in the buffer increases the active energy consumption. But the stand-by power dissipation is less than L and LHVT but greater than LSWHVT.

4) *Limiting switch with high Vt main and sleep transistor (LSWHVT):* The LSWHVT switch consumes the least power. The power-delay of the setup using this switch is only worse than L, LSW and LHVT. But the stand-by leakage is very less.

IV. SIMULATION SETUP

The simulation set-up is as shown in Fig.4 and models the environment under which the switch has to operate in a typical FPGA. The circuit consists of the switch we are simulating (NMOS based or different variations of DTMOS based) followed by a wire which is based on distributed RC model. A buffer is placed after a certain length of the wire and the buffer drives a 5fF capacitive load. The length of the wire between the switch and the buffer is varied in our simulation setup (From $L=1\mu$ to 20μ). An input waveform is applied at the IN node and the power, delay and energy figures for this test set-up for different switches are simulated in a transistor level simulator.

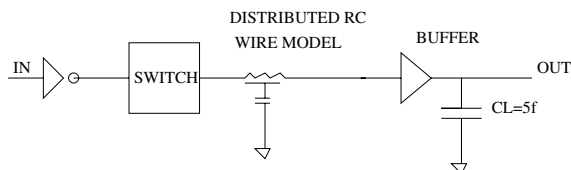


Fig. 4. Simulation set-up

V. SIMULATION RESULTS AND COMPARISONS

The results of the simulations are shown in Figs.5, 6, 7, 8.

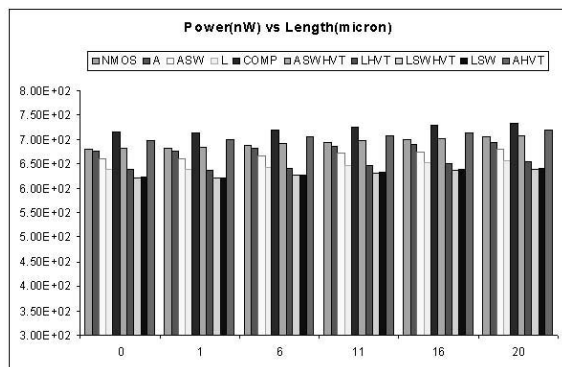


Fig. 5. Active power(nW) vs length(μ m)

Fig.5 is a plot of the power consumed over the circuit shown in Fig.4. Similarly, Fig.6 is a plot of delay that the signal encounters from the input (shown as IN in Fig.4) to output (shown as OUT in Fig.4). Fig.7 is a plot of the power-delay product for the different switches over the simulation set-up. Fig.8 shows the stand-by power consumption of the different switches. This is a plot of the power

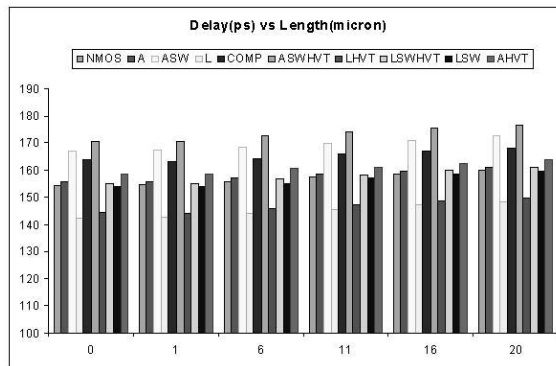


Fig. 6. Delay(ps) vs length(μ m) in active mode

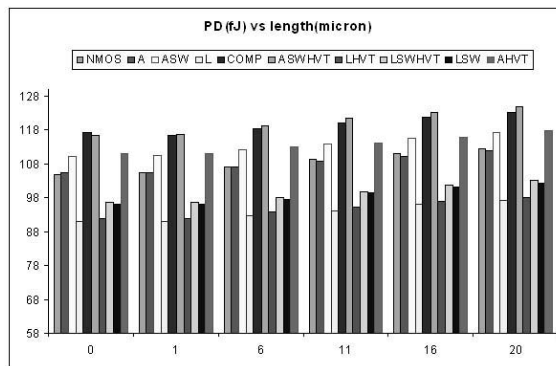


Fig. 7. Power-Delay vs length in active mode

consumed over the simulation set-up when the switch is not being used. The different switches we use for comparison are NMOS, A, ASW, L, COMP (which stands for complementary pass transistor switch), ASWHVT, LHVT, LSWHVT, LSW, AHVT.

From the Fig.5, it can be seen that due to the full threshold (Vt) drop across an NMOS pass transistor switch, the power consumed is high. The complementary pass transistor switch has the highest power consumption due to higher node capacitances. The proposed LSWHVT has the least power consumption. From Fig.6, it can be seen that the proposed LHVT switch and L switch are the fastest. The NMOS based switch is quite fast due to reduced node capacitances compared to the other switches which need more than one transistor but it is slower than the LHVT and the L switch. From Fig.7, it can be inferred that the proposed LHVT and L switch have the best power-delay product. The ASWHVT and the complementary pass transistor switch have the largest power-delay products. From Fig.8, it can be seen that the proposed LSW, LSWHVT, ASWHVT and ASW have the lowest stand-by power dissipation. It is because of the reduction in sub-threshold leakage due to the high Vt sleep transistor being turned off when the switch is un-used. Even though power-delay product of the NMOS switch is better than the ASW, AHVT and ASWHVT, the ASW, AHVT and ASWHVT have a much better stand-by performance than the NMOS based switch.

In the DTMOS based switches the limiting or augmenting transistor (LT or AT) can be shared by more than one main transistor (MT). This means that by sharing the LT or AT, the DTMOS based switch needs only one transistor per switch, thus reducing the area overhead. The COMP switch has the largest area compared to the other switches. It needs four transistors in total (inclusive of the inverter

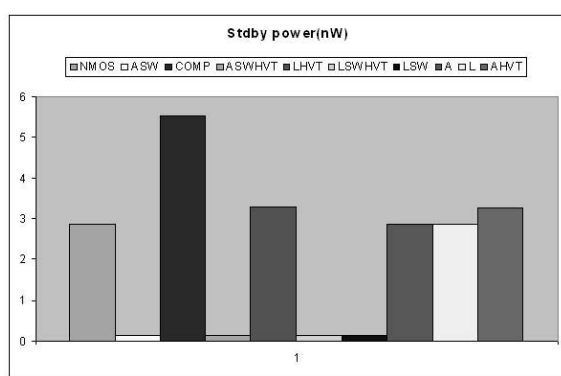


Fig. 8. Power vs supply voltages in stand-by

needed for generating the control signal and its inverse which control the NMOS and PMOS transistor). The NMOS switch is the smallest in size but as already seen, the power-delay product is much higher than the proposed variations.

VI. POWER-DELAY PRODUCT, STAND-BY DISSIPATION, AREA TRADE-OFF

From all the variations of the DTMOS that we studied, we can draw some conclusions. Some switches are better or not depending on whether power, delay, power-delay, stand-by dissipation is the criterion. We can choose any of the switches based on the requirements that we have. The Table.II shows the order of preference of the switches based on the criterion that we have. For eg., in the column entitled "Power", the power consumption of LSWHVT < LSW < LHVT < L ... < COMP, in the column entitled "Delay", the delay through L < LHVT < LSW < NMOS ... < ASWHVT. Similar trends are shown for Power-Delay with L having the least and ASWHVT having the largest Power-Delay product. LSWHVT has the least stand-by leakage and COMP has the highest stand-by leakage.

TABLE II
TRADE-OFFS IN CHOOSING THE SWITCH

Power	Delay	Power-Delay	Standby
LSWHVT	L	L	LSWHVT
LSW	LHVT	LHVT	ASWHVT
LHVT	LSW	LSW	LSW
L	NMOS	LSWHVT	ASW
ASW	LSWHVT	A	L
A	A	NMOS	NMOS
NMOS	AHVT	ASW	A
ASWHVT	COMP	AHVT	AHVT
AHVT	ASW	COMP	LHVT
COMP	ASWHVT	ASWHVT	COMP

VII. ONE VARIATION OF THE PROPOSED LOW ENERGY SWITCH BLOCK

One variation of the various possible implementations which overcomes some of the limitations of a conventional NMOS based switch box is shown in Fig9. Each of the NMOS pass transistors is replaced by a DTMOS with a limiter switch. In addition the buffers following the switches have a sleep transistor with a high threshold. The gate voltage of this sleep transistor is controlled by the configuration signal. If the switch is not selected, the sleep transistor is off, thus disconnecting the buffer from the gnd connection. This prevents leakage in standby.

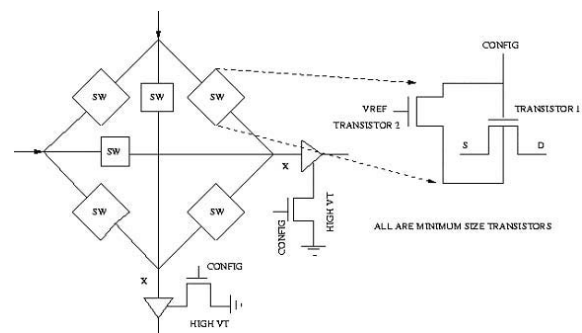


Fig. 9. Proposed Switch Block

VIII. CONCLUSIONS ON THE VARIOUS PROPOSED SWITCHES

It can be seen from Figs.5, 6, 7, 8 that the proposed switch based on the limiter with the main transistor high V_t and a sleep transistor in the buffer following the switch, LSWHVT, consumes the least power and the complementary switch, COMP, consumes the maximum power. Similarly, the switch based on the limiting transistor, L has the lowest delay and power-delay product whereas the switch based on the augmenting transistor with the main transistor high V_t and a sleep transistor in the buffer following the switch, ASWHVT has the highest delay and power-delay product. During stand-by the least power dissipation is of the LSWHVT switch and the maximum is of the complementary switch, COMP.

Table.II helps to choose the switch needed depending on the constraints. For eg., for high speed operation and for the best power-delay product, the L switch can be chosen. The LSW switch is slower than the L switch and has a slightly worse power-delay product but has lower stand-by dissipation. The NMOS switch is better in terms of the Power-Delay product than most of the augmenting based DTMOS switches except the A switch but is worse than all the DTMOS switches based on limiting transistors.

The area overhead is another important issue to be considered since there are many switches in the programmable interconnect fabric of a FPGA. The complementary pass gate (COMP) has the largest area overhead since in addition to a PMOS and a NMOS, an inverter is needed for generating the control signal (which controls the switch) and its inverse. The NMOS switch has the least area. All the DTMOS switches based on augmenting or limiting transistor need two transistors per switch, but the limiting or augmenting transistor could be shared by more than one switch thus reducing the area overhead. For eg., when datapath operations are being performed in a FPGA, the granularity of operation is higher. This involves a bus based communication between logic blocks. In one instance of this, when an eight bit addition is being performed, the eight bits of sum output and the carry signals need to be communicated to another block. This means that nine switches along the way from the source logic block to the destination logic block need to be switched on simultaneously. Only one augmenting or limiting transistor would then be needed for these nine switches.

A 10-16% improvement per switch in the power-delay product, over the conventional NMOS pass transistor can be achieved, by using the limiter based dual threshold MOS transistor switch (could be L, LSW, LHVT or LSWHVT). Since the interconnect fabric in a FPGA is composed of many thousands of switches, the overall improvement in the power-delay product can be significant if limiter based dual threshold MOS switches are used. By sharing the limiter transistor, the area overhead is kept low (For eg. one extra transistor

for every 8 transistors). In stand-by, if the LSWHVT or LSW switch is used, a factor of 20 reduction in the leakage power is obtained compared to the NMOS pass transistor switch. For the other two limiter based Dual Threshold MOS switches, namely, L and LHVT, the leakage is comparable to the NMOS pass transistor switch.

IX. CONCLUSION

Employing the proposed DTMOS based switches results in an energy-efficient FPGA architecture. A 16% improvement in the power-delay product during the active mode per switch and a factor of 20 improvement in the stand-by mode is obtained, using DTMOS and sleep transistor based switch blocks. The lowest power-delay product and the least stand-by dissipation compared to contemporary designs can be achieved using the proposed switches. Since the interconnect fabric of a FPGA has thousands of switches (inside multiplexers and switch boxes), the overall improvement in the power-delay product over the whole FPGA can be significant. Thus, the work described here significantly advances the state of the art in low energy FPGA design. The area overhead of the proposed switch-blocks is shown to be less if the extra transistor needed for DTMOS based switches can be shared intelligently. It was shown in this paper that the transistor can be easily shared especially in bus-based designs with dominant number of datapath operations of higher granularity. DTMOS based switches can be fabricated using conventional CMOS technology with well isolation, or using SOI technology.

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