Implementation of binary stochastic STDP learning using chalcogenide-based memristive devices

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Abstract—**The emergence of nano-scale memristive devices encouraged many different research areas to exploit their use in multiple applications. One of the proposed applications was to implement synaptic connections in bio-inspired neuromorphic systems. Large-scale neuromorphic hardware platforms are being developed with increasing number of neurons and synapses, having a critical bottleneck in the online learning capabilities. Spike-timing-dependent plasticity (STDP) is a widely used learning mechanism inspired by biology which updates the synaptic weight as a function of the temporal correlation between pre- and post-synaptic spikes. In this work, we demonstrate experimentally that binary stochastic STDP learning can be obtained from a memristor when the appropriate pulses are applied at both sides of the device.**

Index Terms—**Neuromorphic systems, STDP, memristors, stochastic learning, spiking neural networks**

I. INTRODUCTION

NEUROMORPHIC engineering has demonstrated in recent decades a tremendous potentiality to develop bio-inspired computing systems for high-speed processing with low-power consumption [1]. Different kinds of neural networks have been proposed, with Spiking Neural Networks (SNNs) being specially suited for low-power hardware implementation, given that neurons are active only when input spikes are received, which improves computational efficiency [2]. These networks mimic the main properties of the biological brain, like the massive parallel connectivity between layers of neurons. However, as the number of implemented neurons and synapses increases, the implementation of efficient learning algorithms becomes one of the critical bottlenecks in terms of resources, time and power consumption.

When memristive elements were first proposed theoretically [3] and later demonstrated experimentally [4], they opened a promising new strategy for emulating biological synapses, as the well-known learning mechanism Spike-timing-dependent plasticity (STDP) [5] could be obtained naturally when applying pre- and post-synaptic spikes at both terminals of a memristor [6], [7]. In order to reproduce different possible STDP rules, it is necessary to design spiking neurons which can generate programmable spike shapes [8], [9].

In this work, we have demonstrated experimentally an STDP rule on a silver-chalcogenide based memristor (commonly referred to as Neuro-Bit) [10] using the ArC ONE characterization platform [11]. To this end, we propose a combination of multi-spike pulse shapes for pre- and post-synaptic signals, taking advantage of the stochastic behavior of the device obtaining a learning probability curve that resembles a stochastic binary STDP rule (a specific kind of STDP rule where 1-bit weights change following a given probability [12]). This can be a very promising strategy to implement online learning on hybrid memristor-CMOS systems [13], providing learning capabilities with minimum nano-scale resources consumption.

II. MEMRISTORS

The memristor is a non-linear passive two-terminal component postulated by Chua [3] in 1971. According to circuit theoretical fundamentals, there are four basic electrical quantities [14]: (1) voltage difference between two-terminals v, (2) current flowing into a device terminal i, (3) charge flowing through a device terminal or integral of current $q = \int i(\tau)d\tau$, and (4) flux or integral of voltage $\phi = \int v(\tau)d\tau$. A two-terminal device is said to be canonical [14] if either two of the four basic electrical quantities are related by a static relationship. Describing the traditional devices in terms of these electrical quantities, the resistor presents a static relationship between voltage v and current i, the capacitor presents a static relationship between charge q and voltage v, and the inductor presents a static relationship between current i and flux ϕ. Ignoring the combinations of a quantity with its own time derivative, leaves one more possibility: charge q and flux ϕ. This last combination led Chua to postulate the existence of the missing two-terminal element: the memristor, as illustrated in Fig. 1. Following Chua's generalization of memristive systems [15], the concept of memristor can be extended to any device exhibiting resistive behavior whose resistance can change through some of the four basic electrical quantities (or combinations of them), while exhibiting memory for that resistance.

Decades after Chua's work, a team at HP Labs obtained a memristor experimentally for the first time, using a thin film of titanium oxide [4], starting a new race to fabricate robust memristive devices and integrate them over CMOS platforms to implement hybrid systems [13].

III. SPIKE-TIMING-DEPENDENT PLASTICITY

Spike-timing-dependent plasticity (STDP) learning algorithms were proposed in the 1990s [5], [16] as a particularization of the Hebbian learning rule formulated in the 1940s [17]. Considering a synapse with weight w which connects two spiking neurons, the change in the synaptic weight Δw is described as a function ξ of the time difference Δt between the post-synaptic spike at t_{post} and the pre-synaptic spike at t_{pre}. Fig. 2 represents different STDP learning functions proposed
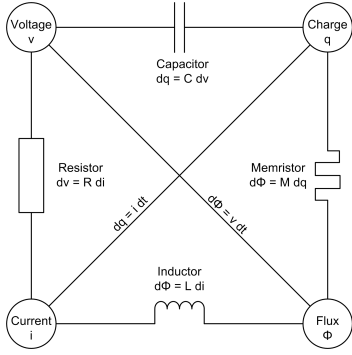
Fig. 1. Illustration of the four canonical elements in terms of the basic electrical quantities, with memristor on the right-hand side.
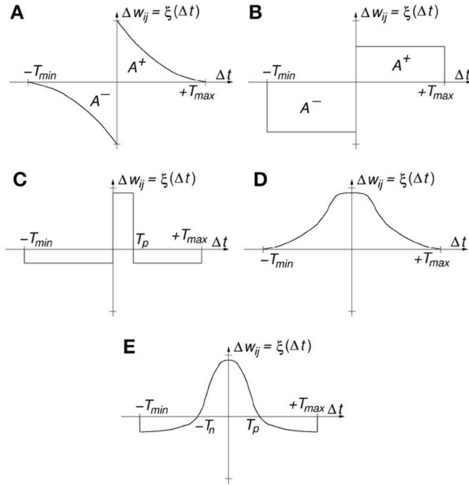

Fig. 2. Different time-based STDP functions.

for $\Delta w = \xi(\Delta t)$, with **A** showing the typical update function first measured in biology [18] and **B**-**E** showing other STDP learning functions that have also been observed in biology or used by computational neuroscientists [19]. In general, they all present some ranges of Δt values where the function produces synaptic potentiation (positive Δw) and some other ranges of Δt where it produces synaptic depression (negative Δw). Some functions present fixed potentiation or depression values for Δw, while some others follow certain curves. In general, they are all oriented towards obtaining continuous values of the synaptic weight w.

A. Binary stochastic STDP

Although STDP typically performs very small weight changes on synapses implying high-resolution implementations, several kinds of limitations (like hardware resources, memory or power consumption) recommend the reduction of weight resolution down to 1 single bit and including some kind of stochastic weight update [12]. That means that only '1' or '0' values are valid for each synaptic weight, with the algorithm changing a weight from '1' to '0' or vice versa following a probability given by the STDP rule [20], [21]. This strategy is especially interesting when implementing synapses with memristors, given the current difficulties to

control precisely the analog resistive value of these devices. Memristors are typically used in binary mode for in-situ computing to overcome sharp switching threshold, functional uniformity, intermediate state initialization and state decay [22]–[24]. This binary mode involves switching memristors between two possible resistive states, i.e., HRS (High Resistive State) and LRS (Low Resistive State). Therefore, we propose a binary stochastic STDP algorithm to be applied to memristive synapses. For that, some pre- and post-synaptic pulse shapes are defined in Section IV-C.

IV. EXPERIMENTAL RESULTS

A. Experimental setup

The experimental setup mainly comprises the ArC ONE platform and Neuro-Bit memristor, as shown in Fig. 3. ArC ONE platform is used to characterize a single or an array of selector-less memristor devices either directly on wafers or in packed samples [11], [25], [26]. The ArC ONE board has an mBED microcontroller driver, bias generating opamps, sense resistor bank, read/write feedback buffers, programmable current source for current pulsing, TIA read opamps, PLCC68 DIP socket, header pins, power management block, resistor banks and digital components like decoders, multiplexers and switches. The working principle of ArC ONE platform is to pick the active and default wordlines and bitlines and apply DC voltage pulses for the needed operation. The user can perform operations such as form, write, erase and read in a sequence or a closed-loop to plot I-V characteristics, to do endurance and retention tests.

Neuro-Bit, a silver-chalcogenide based two-terminal device has a layer of Ge_2Se_3 (30 nm), Ag_2Se (50 nm), and Ag (50 nm)- sandwiched between the top and bottom electrodes [27]–[32]. The 44-pin PLCC breakout board of Neuro-Bit has 20 bonded memristor devices [10]. The pre-programming resistance of the device is 50 MΩ. A positive voltage sweep from 0 to 1 V with compliance current values between 100 nA and 30 μA can cause the device to switch to LRS (also called as 'write' and typical LRS value = 8 kΩ) at a certain voltage (called V_{set}) by making the Ag^+ ions to migrate into the active chalcogenide, Ge_2Se_3 layer and create a low resistance path through the insulator. Similarly, a negative voltage sweep from 0 to -1 V with compliance current values between 100 μA and 10 mA can cause the device to switch to HRS (also called as 'erase' and typical HRS value = 13 MΩ) at a certain voltage (called V_{reset}) by removing Ag^+ ions back from the active chalcogenide layer. The device is read by applying a read voltage, V_{read} = 50 mV.

B. Device Characterization

The main challenges in using Neuro-Bit devices are the intrinsic variability and sensitivity of the device. Different samples of the device switch at different voltages V_{set} and V_{reset}, and with different compliance current. Besides, for a single device, different behavior might be observed in two or more cycles of 'write' or 'erase'. These variations attribute to the stochasticity of the synaptic device, which results in the escape of local minima during learning and inference [33].
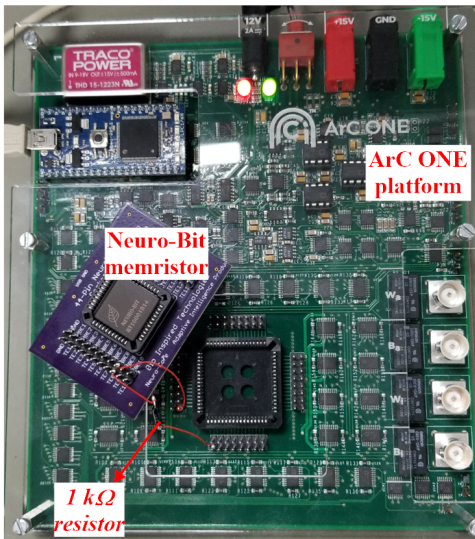
Fig. 3. A Neuro-Bit memristor connected to the active word-line and bit-line terminals of ArC ONE platform.
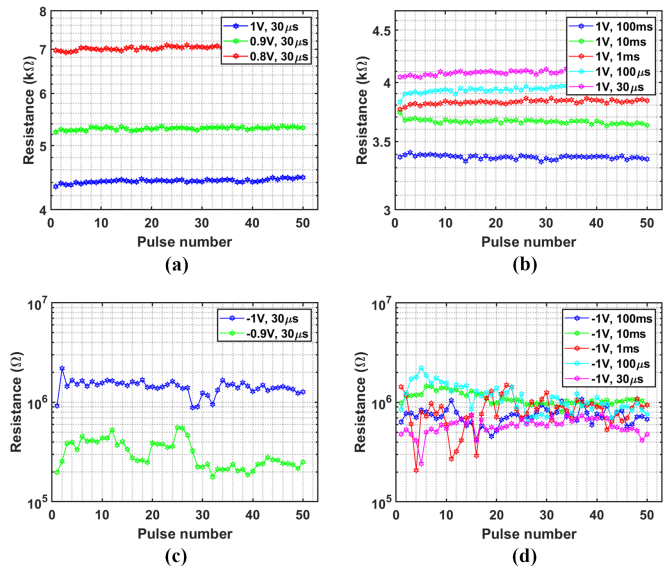

Fig. 4. Characterization of the device, showing the measured resistance after several Write and Erase pulses. (a) With the device initially in HRS, Write pulses are applied with a fixed width of $30\mu s$ and different amplitudes. (b) With the device initially in HRS, Write pulses are applied with a fixed amplitude of $1V$ and different widths. (c) With the device initially in LRS, Erase pulses are applied with a fixed width of $30\mu s$ and different amplitudes. (d) With the device initially in LRS, Erase pulses are applied with a fixed amplitude of $-1V$ and different widths.

Although the stochastic synapses raise reliability concerns in ANN, there are many embracing approaches such as- increasing the effective resolution of synaptic weights [34]–[36], using stochastic neurons [37], [38], etc. Neuro-Bit devices are also very sensitive. They can easily be permanently damaged when receiving voltage transients of few mV (including environmental noise), shorting the device or hanging it at LRS, when they are carelessly biased above the needed V_{set}, below the appropriate V_{reset} or without the required compliance current. Hence, it is always recommended to carefully set-up the experimental test-bench and to attempt 'write' and 'erase' operations with very conservative values for each Neuro-Bit memristor until the user is comfortable with its performance.

In order to characterize the Neuro-Bit memristor, the device is initially verified for I-V characteristic using HP4145 SPA, whose observation of DC voltage sweep measurements are documented in the user manual [10]. After observing some successful repetitive switching in a Neuro-Bit device in HP4145 SPA, we connected it to the active wordline and bitline of ArC ONE platform through a 1 kΩ resistor (as a safety precaution to limit current during LRS) to characterize its switching using DC voltage pulses, as shown in Fig. 3. We varied both amplitude and pulse-width of the 'write' and 'erase' DC pulses using the ArC ONE Control GUI interface. Fig. 4 shows the LRS and HRS results for 50 'write' and 'erase' pulses for different pulse-widths and amplitudes. The measured value for LRS is in the range of 3 to 7 kΩ, which is quite similar to the typical value of 8 kΩ provided in the user manual. A high variability at HRS is observed, with values between hundreds of kΩ and 2 MΩ, smaller than the typical value of 13 MΩ. This difference is given by the limited precision of the measurements for such large resistance values.

C. STDP tests

The main goal of this work is to demonstrate experimentally an STDP rule on Neuro-Bit memristor using the ArC

ONE platform. As illustrated in Fig. 5(a), we use a single memristor to model a synapse connecting a pre- and a post-synaptic neuron. Each neuron generates pre-synaptic pulses V_{pre} which propagate forward and post-synaptic pulses V_{post} which propagate backwards. Therefore, the voltage across the synapse will be given by the difference $V_{pre} - V_{post}$. As described in Section III, an STDP rule updates the synaptic weight according to the time difference Δt between V_{pre} and V_{post}. In this work, we propose the pulse shapes shown in Fig. 5(b), where V_{pre} is a positive pulse with amplitude $0.5V$ and width $1.5ms$, and V_{post} is a train of 3 negative pulses with amplitude $-0.5V$, width $30\mu s$ and separation $0.75ms$. While the positive pulse in V_{pre} starts at the onset time t_1, the first negative pulse in V_{post} is delayed $1.5ms$ since the onset time t_2. With these particular shapes, we guarantee that the voltage applied to the memristor $V_{pre} - V_{post}$ will only reach $1V$ for a certain range of time difference Δt. As we observed during the characterization of the device, a pulse with $1V$ amplitude and $30\mu s$ width is enough to write the memristor, i. e., to set its resistance to LRS, while pulses with $0.5V$ amplitude should not affect its state. An example is shown in Fig. 5(c), where a time difference of $\Delta t = 1ms$ is considered. In this case, a pre-synaptic pulse is generated at time $t_1 = t_2 + \Delta t$, while a post-synaptic pulse is generated at time t_2. With this particular time difference, the resultant voltage applied to the memristor is shown below, with two highlighted positive pulses with amplitude $1V$ and width $30\mu s$, which should write the state of the device. In this case, the third $30\mu s$ pulse should not affect the device.

In order to reproduce the STDP rule, it was necessary to apply combinations of V_{pre} and V_{post} pulses to the Neuro-Bit
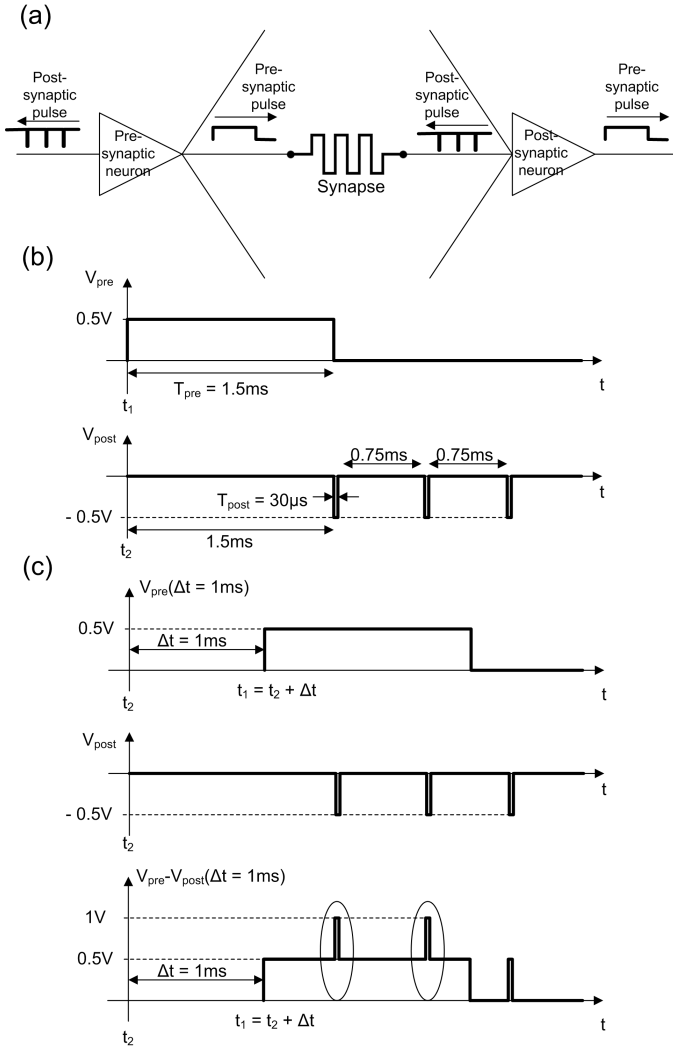
Fig. 5. (a) Illustration of the STDP rule applied to a synapse connecting two neurons. (b) Proposed pulse shapes for pre- and post-synaptic pulses. (c) Calculation of the applied pulse to the memristor ($V_{pre} - V_{post}$) with a time shift of $1ms$.

Fig. 6. Probability of 'writing' the memristor for different values of Δt between pre- and post-synaptic spikes, after testing the same stimulus 100 times.

memristor while sweeping the time difference between them Δt using the ArC ONE platform. For the proposed pulses, a sweeping range from 0 to $8ms$ was considered, with $0.1ms$ steps. For each value of Δt, the memristor was initially reset to HRS, then applied the pre- and post-synaptic pulses, and afterwards the resistance was read and stored. If the measured resistance was lower than 50 kΩ, we considered the device was at LRS; otherwise, we assumed HRS. We repeated the whole process 100 times, and we calculated the probability of writing for each value of Δt. The obtained result is shown in Fig. 6. If the behavior of the memristor were deterministic, we would expect to obtain 100% probability for the range $0 < \Delta t < 3ms$ (shifting V_{post} up to 3ms provides coincidence with at least one of the narrow pulses in V_{pre}), and 0% otherwise. However, the stochasticity inherent to the device produced the STDP rule shown in the figure, with a maximum value of around 90% around the middle of this range. For a certain range around $\Delta t = 1.5ms$, there are at least 2 pulses with $1V$, therefore increasing the probability of writing. For values of
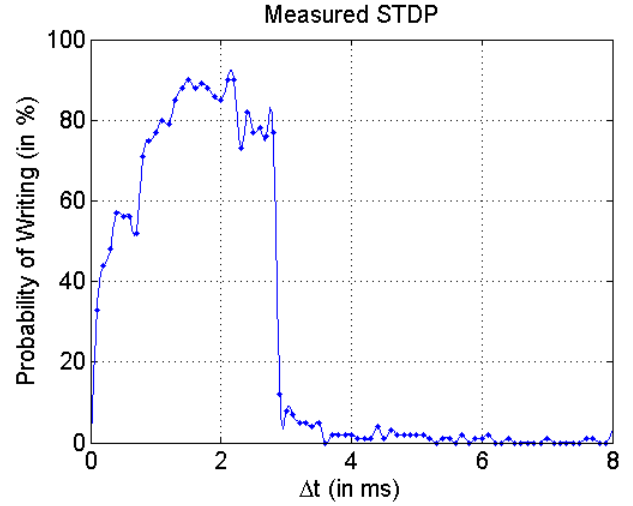
Δt outside the desired range, we observe a probability slightly larger than 0 (around 1 or 2%), representing the chance that the device can be written with applied voltages as low as $0.5V$.

In this example, we have obtained experimentally a binary stochastic STDP rule by using some specific pulse shapes, whose parameters can be adapted to modify the desired rule. Different STDP rules can be obtained by choosing the appropriate pulse shapes.

V. CONCLUSION

A silver-chalcogenide based memristor (Neuro-Bit) has been characterized using ArC ONE platform, identifying the minimum pulse width and amplitude needed to write and erase the state of the device. Using this knowledge, an STDP learning rule has been measured experimentally by applying the appropriate pulses to both terminals of memristors, emulating the pre- and post-synaptic spikes in a biological system. This result demonstrates that different STDP rules can be implemented in hybrid memristor-CMOS systems, which can be crucial to perform large-scale online learning with minimum nano-scale resources consumption.

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