17.7 An Energy-Aware Multiple-Input Power Supply with Charge Recovery for Energy Harvesting Applications

Nathaniel J. Guilar[1,2], Rajeevan Amirtharajah[1], Paul J. Hurst[1], Stephen H. Lewis[1]

[1]University of California, Davis, CA
[2]Agilent Technologies, Santa Clara, CA

Energy harvesting systems such as self-powered wireless sensor nodes rely on a diverse set of energy sources in their continuously changing environment for power. A highly flexible power supply with multiple sources is needed to deal with large variation in environmental conditions. This paper describes an integrated power management system for use with multiple energy harvesters, which employs energy awareness and charge recycling. Previous multiple-input power management systems only allow energy to be harvested from a single source at a time [1] (typically the source with the largest voltage) thereby wasting the energy from the other energy harvesters. In order to increase the total energy available, the work presented here allows the system to gather and add together voltages from multiple sources at the same time.

Figure 17.7.1 shows a simplified block diagram for the proposed power management system. The system has two inputs: an AC input (V_{vibe}) and a DC input (V_{solar}). The AC input can be driven by a multiple-electrode piezoelectric transducer for vibrational energy harvesting [2], while the DC input can be connected to photodiodes for solar energy harvesting or to a thermoelectric generator [3]. The system also has two outputs: a high-ripple output (V_{int}) and a low-ripple output (V_{out}). The low-ripple output uses an additional stage of regulation, and therefore requires more energy to operate. Since the power supply regulates energy for multiple loads with differing requirements, allowing a precision-efficiency tradeoff is desirable. This tradeoff is accomplished by a sliding mode (SM) DC/DC controller.

For the AC/DC converter in Fig. 17.7.1, the rectified voltage from the piezoelectric generator functions not only as the input to a switched-capacitor (SC) boost converter, but also as the control signal V_{ct} into a VCO, which dictates the boost converter's switching frequency f_{ct}. As the piezoelectric disk vibrates, the VCO output frequency varies, and the current drawn from the disk is proportional to its generated voltage V_{vibe}. When the generated voltage from a piezoelectric disk is near zero, the majority of the disk's energy is held in kinetic form. Open circuiting the load seen by the piezoelectric disk during zero crossings allows the disk to retain more of its kinetic energy. Near maximum deflection, the piezoelectric disk exchanges this preserved kinetic energy for increased potential energy, generating a larger peak voltage. The rectified voltage from the vibrational source is then added to the voltage from the solar source by wiring multiple capacitors in series, similar to a SC charge pump.

Figure 17.7.2 shows a schematic of the SM DC/DC converter, which employs a charge recycling technique. The controller first samples the error signal V_e, filters it, determines the polarity of the filter output, and drives the output transistors (MN and MP) in the opposite direction of the error. The controller converges to a steady-state limit cycle with a constant frequency and duty cycle. In general, this frequency depends on the ratio between the harvested energy voltage and the desired output voltage. For loads requiring low ripple such as the ADC in Fig. 17.7.1, an analog FIR filter (g–kz^{-1}) is employed before the comparator to provide a phase lead component in the loop, reducing the ripple by increasing the limit cycle frequency.

Energy recycling is a technique for recovering and reusing stored charge [4], and is effective on highly capacitive nodes where the recycled energy is greater then the required overhead. The buck converter output and the buffer stages are ideal for energy recycling due to the large parasitic capacitance at the drains of MP and MN, which drive the large off-chip L and C required for the output filter. Typically, a buck converter discharges its stored output energy through an NMOS transistor to ground. Instead, transistor MN of the energy recycling buffer here connects the output to an energy-storage device, e.g., a piezoelectric transducer, to store the recycled energy in the mechanical domain. Piezoelectric transducers have very high Q, making them excellent energy storage elements. NMOS clamping transistor MC later forces the inverter output to ground. This configuration produces pulses of recycled charge at every switching edge. Returning the recycled energy back into the energy harvesting source from which it was originally generated forms a positive feedback loop. Tuning of the charge recycling feedback loop can be accomplished through a comparator and multiplexer such that the returned energy adds constructively with the disk's vibrations, yielding a net increase in generated energy.

Figure 17.7.3 shows a block diagram of the passive SC FIR filter used in the SM controller. Passive SC channels work in a time-interleaved manner to generate the analog input to a dynamic comparator (V_{FIR}). Using a passive filter instead of an active one allows the controller to operate over a wide range of supply voltages (V_{supply}). The upper 3 channels are time interleaved and together create the kz^{-1} term. Here, k can be varied to change the phase lead provided by the filter, to control the limit cycle frequency of the SM controller and limit its dependence on the duty cycle [5]. Two additional time-interleaved gain-boosting channels generate a proportional term with a differential gain of g. On ϕ_1 the error signal V_e is sampled onto multiple parallel capacitors C_g. During ϕ_2 the capacitors are stacked in series producing a gain of g=6 (neglecting parasitics, and with kz^{-1} channels turned off), which helps reduce the effect of comparator offset. Every sampling period charge from a kz^{-1} channel is combined with charge from a gain-boosting channel to produce the comparator input.

Of chief importance for a regulator that handles multiple loads is to have a fast transient response. Otherwise, considerable time and energy are spent switching between subsystems with different voltage and ripple requirements. Figure 17.7.4 shows a measured waveform for the output of the SM controller as it switches between the four load circuits, which were emulated using resistors and switches. Sensitive analog load circuits such as the ADC may require small ripple, while the digital circuits in the DSP could be designed to handle large ripple. The transient cycle concludes with a higher voltage RF transmitter operating for a short burst of transmitted data. This plot demonstrates the flexibility of the discrete-time SM controller and its large-signal response, which is stable for a wide range of ripple and amplitude combinations.

Figure 17.7.5 plots the measured power dissipation for the power management system including clock generation with and without energy recycling. A 10% decrease in dissipated power is observed when engaging the charge recycling loop. Figure 17.7.6 highlights the measured performance for the AC/DC and DC/DC converters. The prototype DC/DC converter has a slightly lower efficiency than a previous reported work, which was designed in a more-advanced CMOS technology [6], but can function over a wider voltage range and employs charge recycling. Figure 17.7.7 shows the die micrograph.

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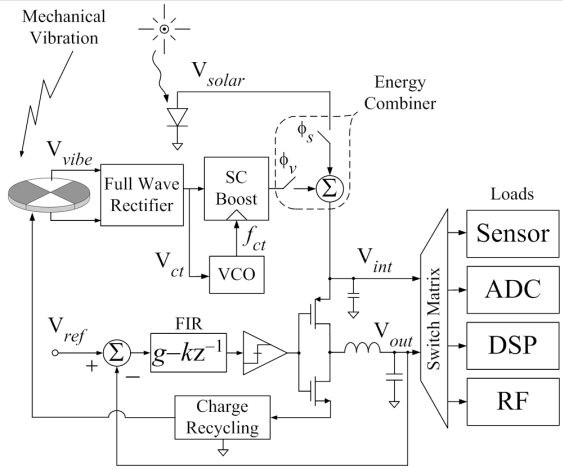

Figure 17.7.1: Simplified block diagram of power management system. Harvested mechanical and solar energies are combined to generate intermediate voltage *Vint*. Operating frequency of the switched-capacitor boost regulator is determined by an energy-aware voltage controlled oscillator. Further regulation by a sliding mode DC/DC controller produces the low-ripple output *Vout*.

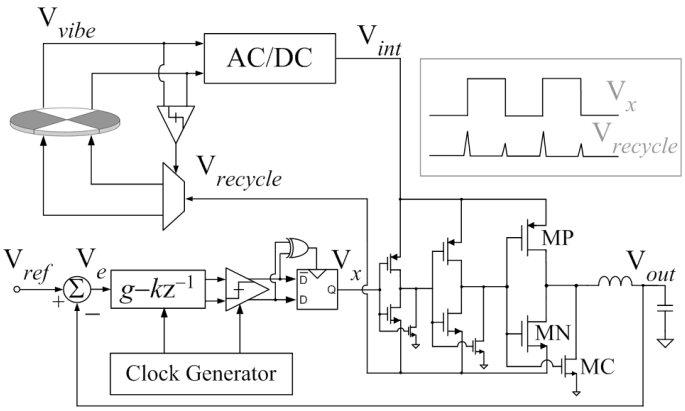

Figure 17.7.2: Schematic of discrete-time sliding-mode DC/DC converter with charge recycling buffer. Charge recycling is employed in the buck converter to form a positive feedback loop around the piezoelectric disk.

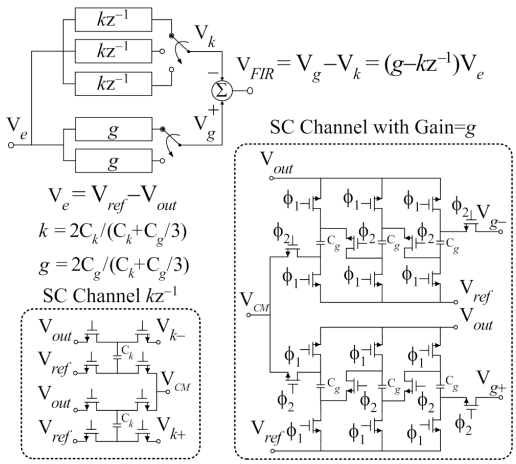

Figure 17.7.3: Passive time interleaved FIR filter. A single SC channel is expanded. Only NMOS switches are shown for simplicity. ϕ_1 and ϕ_2 are nonoverlapping clocks. V_{CM} is the common-mode voltage at comparator input. To save power, the top three channels can be turned off when the kz^{-1} term is not needed. Clocking for kz^{-1} channel not shown for simplicity.

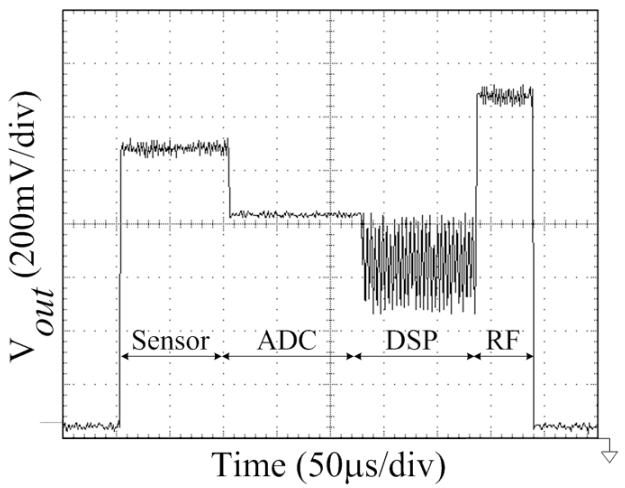

Figure 17.7.4: Measured output voltage of DC/DC controller as it switches between powering the functional blocks in Fig. 17.7.1 (V_{int} = 2V). The digital block can tolerate a higher ripple than the analog blocks, hence the controller can trade efficiency for ripple.

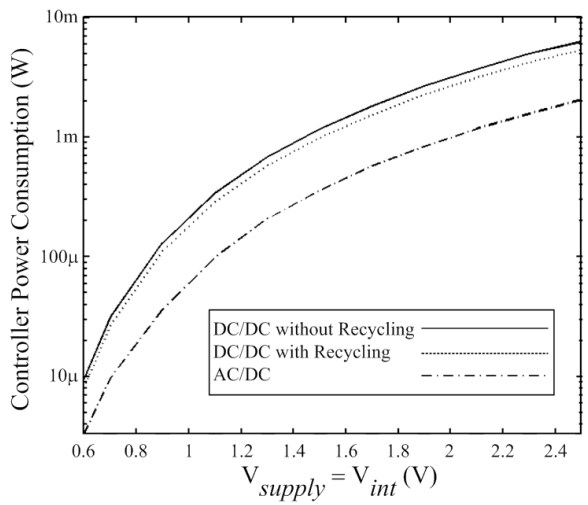

Figure 17.7.5: Measured AC/DC and DC/DC controller power consumption vs. supply voltage. Curves shown for DC/DC converter with and without charge recycling. A 10% decrease in power consumption is observed when charge recycling is used.

Specification (Unit)	AC/DC	DC/DC
CMOS Technology (μ m)	0.25	
Quiescent Current (µA)	0.012 (V_{int} = 0.6V)	
Nominal Process V_{DD} (V)	2.5	
Regulated Supply Voltage (V)	0.076 to 2.5	0.068 to 2.25
Total Die Area (mm²)	0.15	0.22
Max Power Efficiency* (%)	84.1 (V_{int} = 0.6V)	74.5 (V_{out} = 0.6V)
Offset (mV)	N/A	5.3
Overshoot (%)	N/A	1
Min Voltage Ripple (mV)	N/A	9.8 (V_{out} = 2V) 50 (V_{out} = 0.6V)
Transition Rate (V/µs)	N/A	2.22 (V_{out} = 2V) 0.4 (V_{out} = 0.6V)
Clock Generation Power (µW)	4.5	13
Controller Power (µW)	0.9 (V_{int} = 0.6V)	3 (V_{out} = 0.6V)
Delivered Power (µW)	74	78

Figure 17.7.6: Summary of measured IC results. *Includes controller and clock generation power.

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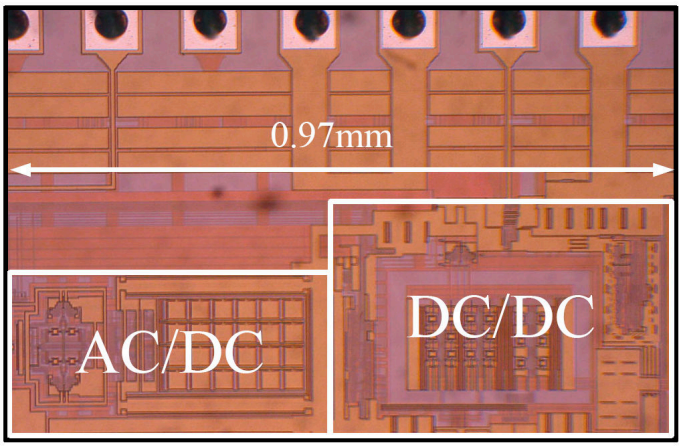

Figure 17.7.7: Die micrograph.

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