HHS Public Access

Author manuscript

IEEE J Solid-State Circuits. Author manuscript; available in PMC 2015 August 13.

Published in final edited form as:

IEEE J Solid-State Circuits. 2015 February ; 2015: .

27.6. A 0.7pF-to-10nF Fully Digital Capacitance-to-Digital Converter Using Iterative Delay-Chain Discharge

Wanyeong Jung, **Seokhyeon Jeong**, **Sechang Oh**, **Dennis Sylvester**, and **David Blaauw**

University of Michigan, Ann Arbor, MI

Capacitance sensors are widely used to measure various physical quantities, including position, pressure, and concentration of certain chemicals [1–6]. Integrating capacitive sensors into a small wireless sensor system is challenging due to their large power consumption relative to the system total power/energy budget, which can be as low as a few nW [4]. Typical Capacitance-to-Digital Converters (CDCs) use charge sharing or charge transfer between capacitors to convert the sampled capacitance to voltage, which is then measured with an ADC [1–6]. This approach requires complex analog circuits, such as amplifiers and separate ADCs, increasing design complexity and often increasing power consumption. Moreover, the initial capacitance to voltage conversion essentially limits the input capacitance range because of output voltage saturation. This paper presents a fully-digital CDC that is based on the observation that when a ring-oscillator (RO) is powered from a charged capacitance, the number of RO cycles to discharge the capacitance to a fixed voltage is naturally linear with the capacitance value. This observation enables a simple, fully digital conversion scheme that is inherently linear. As a result, the proposed CDC performs conversion across a very wide capacitance range of 0.7pF to over 10nF with < 0.06% linearity error. The CDC senses 11.3pF input capacitance with 35.1pJ conversion energy and 141fJ/c-s FoM, which marks the lowest conversion energy and FoM reported.

Figure 27.6.1 explains the proposed conversion method. The top node of sensed capacitor *CT* is directly connected to the supply node of a ring oscillator. This node is initially charged to V_{HIGH}, and is then discharged gradually as the inverter RO oscillates. As signals in the RO transition, the RO draws some charge from C_{SENSE}, gradually lowering V_{CT}. As a result the RO propagation delay increases, which is compared to a constant delay reference. The RO transition count until the period delay becomes longer than the reference delay is recorded by a counter, which becomes the output code D_{OUT}.

Since RO delay only depends on V_{CT} (neglecting noise initially), D_{OUT} is equal to the number of RO transitions while V_{CT} is discharged from V_{HIGH} to some constant voltage, V_{LOW}. During conversion, at any particular V_{CT} value the amount of charge withdrawn per RO transition only depends on V_{CT} at that time. Therefore, the number of transitions required to reduce V_{CT} by a certain small voltage is proportional to input capacitance C_{SENSE}. As this is true at any V_{CT} level, the output code D_{OUT}, the sum of transition counts across all continuous small intervals from V_{HIGH} to V_{LOW}, is also proportional to C_{SENSE}. As the RO draws charge directly from C_{SENSE} without initial capacitance to voltage conversion, the CDC input capacitance range is essentially unlimited, constrained only by the counter size. This is desirable when the C_{SENSE} range is uncertain at design time.

Furthermore, energy used to charge C_{SENSE} is reused to oscillate the RO, reducing overall power consumption.

Figure 27.6.2 shows the detailed implementation of the CDC circuit and its operation. Here an inverter chain is used in place of an RO to discharge C_{SENSE} – it is a 16-stage chain that is identical to the reference delay generator. Because of the identical structures, conversion stops when V_{CT} drops below V_{LOW}. The number of stages in the inverter chain is chosen for optimal SNR per conversion energy, where the energy to charge C_{SENSE} is balanced with the energy consumed by other blocks. The two propagation delays are compared by three delay comparators, which have a similar structure to an RS latch. The bottom comparator compares the propagation delay of falling edges, and the middle one compares the rising edges. Whenever the reference delay is shorter than the C_{SENSE} discharge delay chain, the comparators output pulses once, increasing counts stored in the *sub1* and *sub2* counters. A third counter tracks the main oscillation triggering signal. After each comparison, the next edge generator block triggers the next discharge and delay comparison, maintaining oscillation. All blocks except the C_{SENSE} delay chain operate at V_{LOW}, and a level converter drives the two delay chain inputs with V_{HIGH}.

As shown in the timing diagram of Fig. 27.6.2, conversion starts by precharging C_{SENSE} to V_{HIGH}. This is followed by *Sense* rising, triggering the first edge to propagate through the two delay chains. The top comparator takes in a slightly delayed version of the reference delay and determines when to finish the overall conversion, which occurs when V_{CT} becomes lower than V_{LOW} by some margin. As V_{CT} approaches V_{LOW}, the bottom two delay comparators pulse CK_1 and CK_2. They initially pulse sporadically, due to noise, and then more frequently as V_{CT} crosses V_{LOW}. Just before conversion finishes, these two comparators pulse every cycle. When the top comparator pulses *Finish*, *Sense* is turned off and oscillation stops. Final D_{OUT} is the total count of comparator outputs for which $V_{CT} > V_{LOW}$, and is calculated as $2\times D_{MAIN} - (D_{SUB1}+D_{SUB2})$.

The use of three comparators is designed to increase SNR by averaging noise over many comparisons when V_{CT} is near V_{LOW}. Comparing both rising and falling edges doubles the number of comparisons. By extending the conversion to where V_{CT} falls some margin below V_{LOW}, comparisons are performed through the whole noisy region around V_{LOW}, whereby false "$V_{CT} < V_{LOW}$" decisions above V_{LOW} are stochastically compensated by false "$V_{CT} > V_{LOW}$" decisions below V_{LOW}. Simulation shows that energy increases by 3% compared to the standard approach of stopping conversion immediately after the first comparison triggers, while overall conversion noise is square-rooted. In addition, the distribution of D_{OUT} using this scheme is centered at the number of exact counts from V_{HIGH} to V_{LOW}, thereby improving output code linearity.

The CDC measures the capacitance between one input node and ground, but some applications require the capacitance value between two input nodes excluding parasitic capacitance to ground. We accomplish this through three conversions, as shown in Fig. 27.6.3. First, node B is connected to ground and the capacitance between node A and ground is measured, which includes parasitic capacitance C_{PA}. Second, nodes A and B are flipped and $C_{SENSE} + C_{PB}$ is measured. Finally, both A and B nodes are connected to V_{CT} to

measure $C_{PA} + C_{PB}$. By adding the first two codes and subtracting the third, the parasitic capacitance is canceled out. While this requires three conversions, parasitic capacitance typically remains unchanged or changes slowly (Fig. 27.6.5, bottom) and the parasitic cancelation can be performed infrequently, amortizing its overhead.

The output code varies as temperature or supply voltage changes. This code deviation is removed by one-point calibration (Fig. 27.6.3). In a calibration phase, V_{CT} is connected to an internal reference capacitor with known capacitance C_{REF} and the ratio of C_{REF} to corresponding D_{OUT} is stored. In subsequent normal conversion, digital output codes are converted to actual capacitance value by multiplying the code and the stored ratio. If the supply voltage changes sufficiently slowly, this calibration can be re-done occasionally.

The CDC is fabricated in 40nm CMOS and tested with V_{HIGH}=1.0V and V_{LOW}=0.45V. Core circuit area without testing circuits and internal capacitors is 0.0017mm^2. Fig. 27.6.4 shows the test chip has a very wide input capacitance range from 0.7pF to 10nF with a small linearity error of < 0.06%. Measured output noise percentage reduces as C_{SENSE} increases due to noise averaging. At 11.3pF, the CDC has 0.109% resolution, 35.1pJ total conversion energy (including both V_{HIGH} and V_{LOW}), and 141fJ/c-s FoM. FoM increases monotonically with the sensed capacitance. Fig. 27.6.4 also shows output code sensitivity to temperature improves by 145× (from 2247ppm/°C to 15.5ppm/°C) due to calibration. Results with an actual pressure sensor (Fig. 27.6.5) demonstrate 1.39mmHg resolution with parasitic cancelation. Figure 27.6.6 summarizes CDC performance and compares to prior work.

Acknowledgments

The authors thank TSMC University Shuttle Program for chip fabrication and NSF for research support.

References

1. Cong P, et al. A Wireless and Batteryless 10-Bit Implantable Blood Pressure Sensing Microsystem With Adaptive RF Powering for Real-Time Laboratory Mice Monitoring. IEEE J Solid-State Circuits. Dec; 2009 44(12):3631–3644.
2. Ha H, et al. A 160nW 63.9fJ/conversion-step Capacitance-to-Digital Converter for Ultra-Low-Power Wireless Sensor Nodes. ISSCC Dig Tech Papers. Feb.2014 :220–221.
3. Oh S, et al. 15.4b Incremental Sigma-Delta Capacitance-to-Digital Converter with Zoom-in 9b Asynchronous SAR. VLSI Circ Symp Dig Tech Papers. Jun.2014 :222–223.
4. Ghaed MH, et al. Circuits for a Cubic-Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor. IEEE Trans Circuits and Systems I: Regular Papers. Dec; 2013 60(12):3152–3162.
5. Tan Z, et al. A 1.2-V 8.3-nJ CMOS Humidity Sensor for RFID Applications. IEEE J Solid-State Circuits. Oct; 2013 48(10):2469–2477.
6. Tan Z, et al. An energy-efficient 15-bit capacitive-sensor interface based on period modulation. IEEE J Solid-State Circuits. Jul; 2012 47(7):1703–1711.

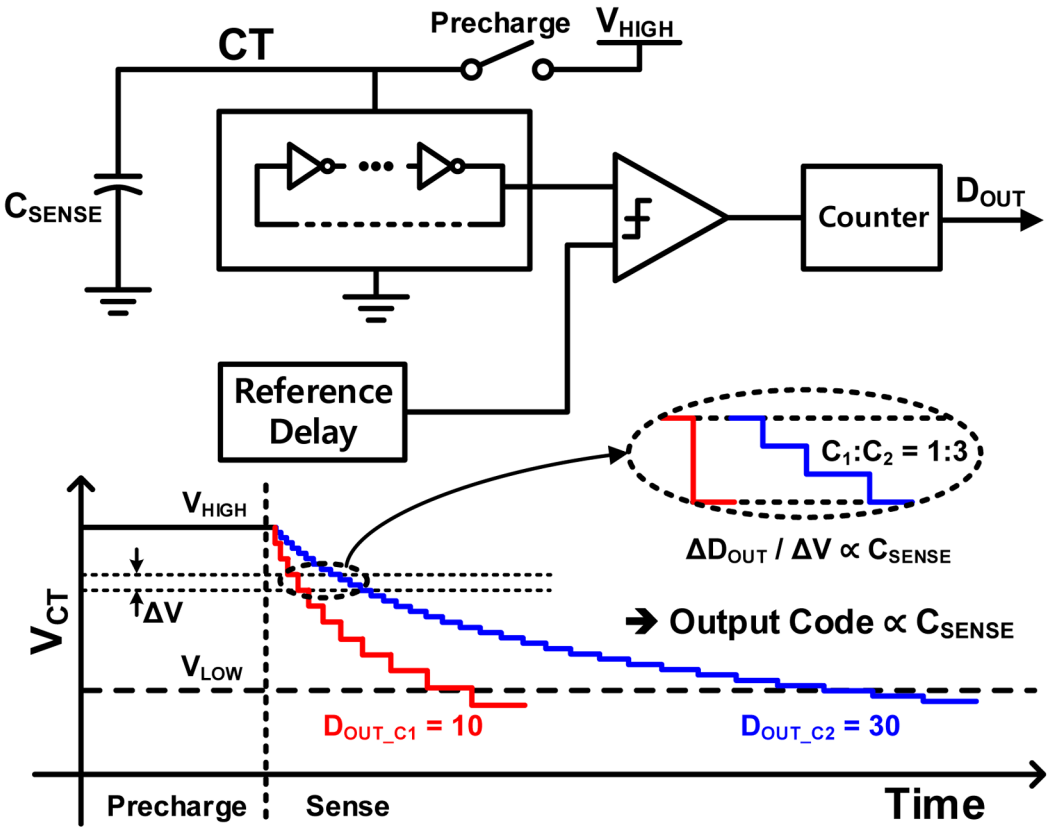


Figure 1.
Basic structure and operation scheme of the proposed CDC.

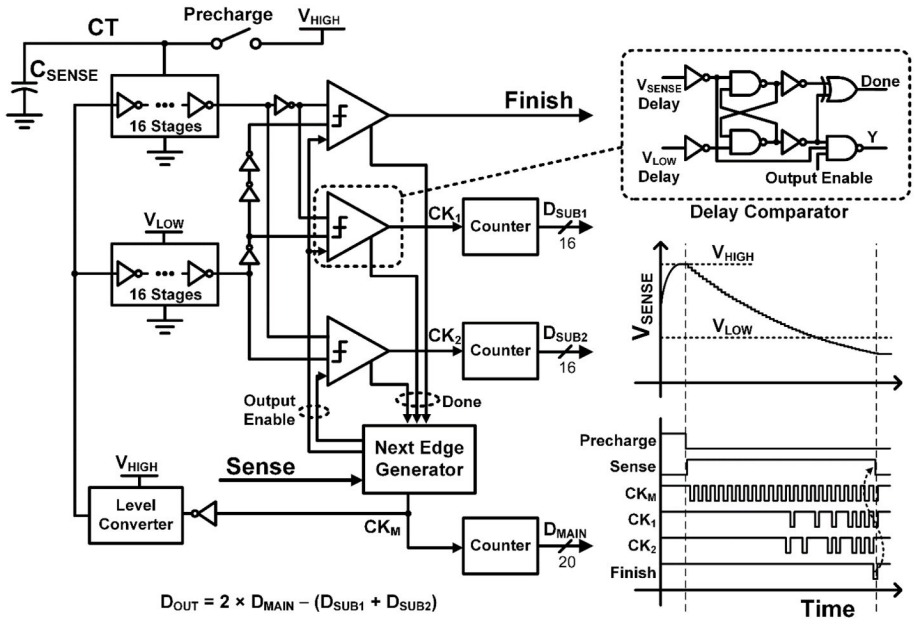


Figure 2.
Detailed implementation of the CDC.

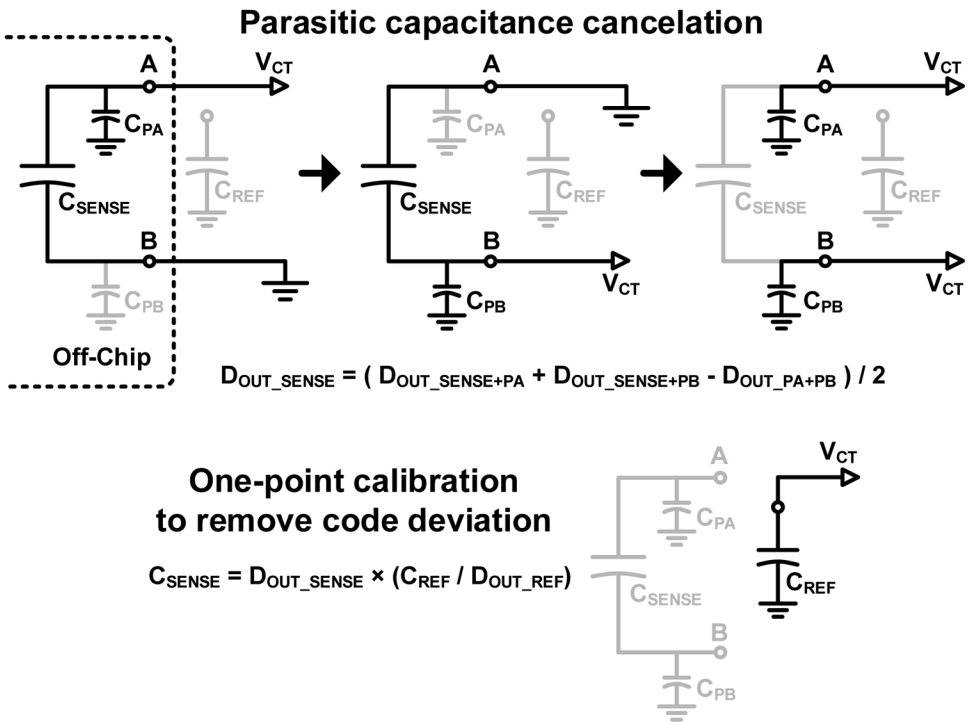


Figure 3.
Techniques for removing parasitic capacitance (top) and code deviation due to voltage and temperature sensitivity (bottom).

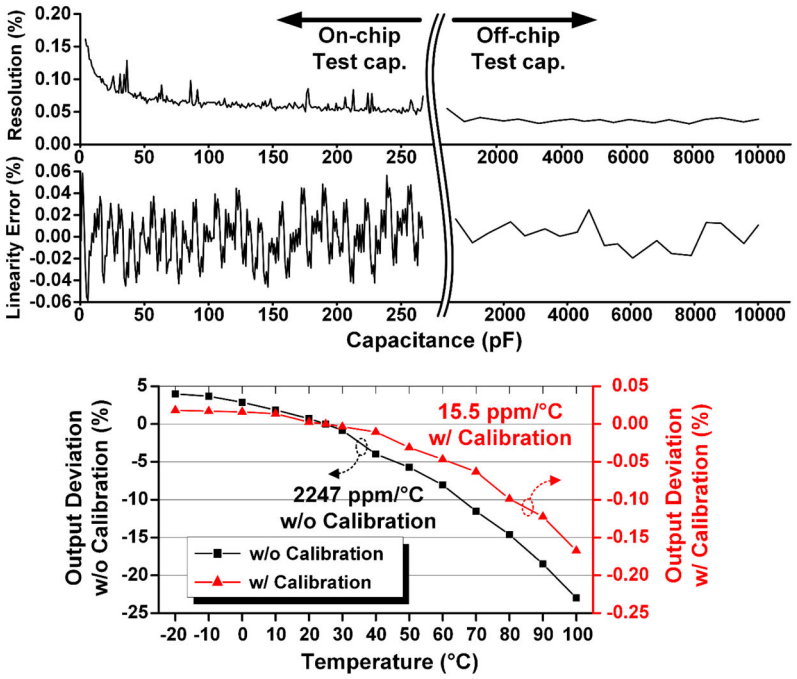


Figure 4.
CDC resolution and linearity error (top), and its output temperature sensitivity (bottom).

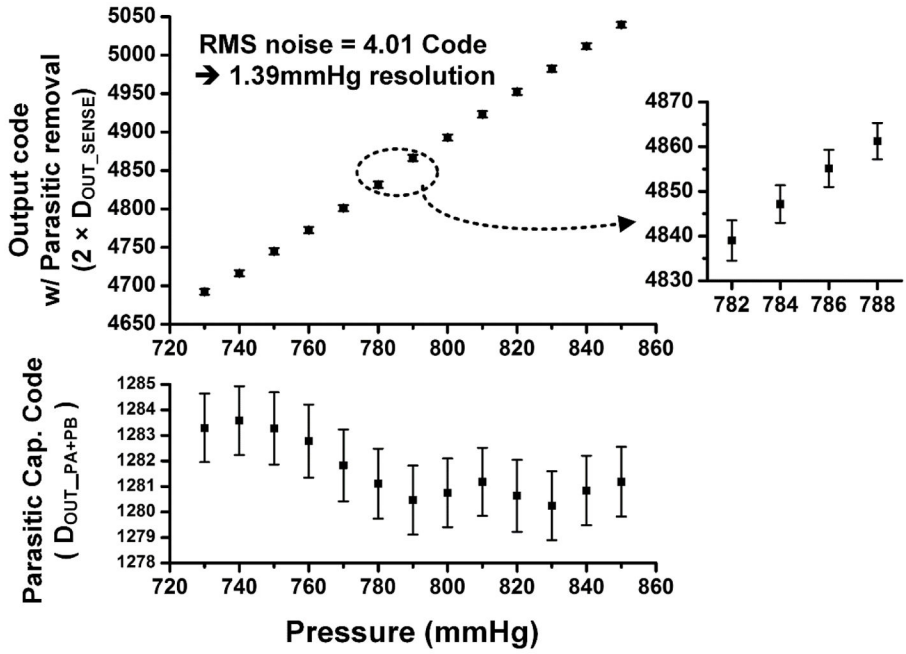


Figure 5.
Measured result with capacitive pressure sensor w/parasitic cancelation (top).

	[1] JSSC 09	[2] ISSCC 14	[3] VLSI 14	[5] JSSC 13	[6] JSSC 12	This work
Technology	1.5μm CMOS	0.18μm CMOS	0.18μm CMOS	0.16μm CMOS	0.35μm CMOS	40nm CMOS
Method	CDS + Cyclic ADC	CDS + SAR	SAR + ΔΣ	ΔΣ	Period Modulation	Iterative Delay-Chain Discharge
Input range	N/R	2.5 – 75.3pF	0 – 24pF	0.54 – 1.06pF	N/R	0.7pF – 10nF
Resolution	75aF	6.0fF	0.16fF	70aF	N/R	0.109% [1] (12.3fF)
Meas. Time	0.5ms	4ms	230μs	0.8ms	7.6ms	19.06μs [1]
Power	36μW [5]	160nW	33.7μW	10.3μW [5]	211μW [5]	1.84μW [1]
Conversion Energy [2]	18nJ	640pJ	7.75nJ	8.26nJ	1.61μJ	35.1pJ [1]
FoM [3] (fJ/c-s)	22000	181	175	3900	139000	141 [1,4]

1 Measured when sensing 11.3pF capacitance w/o parasitic cancelation or calibration.

2 Conversion Energy = Power * (Meas. Time)

3 FoM = (Conversion Energy) / $2^{(20 \log (\text{Input range} / 2\ \text{Sqrt}(2) / \text{Resolution}) - 1.76) / 6.02}$

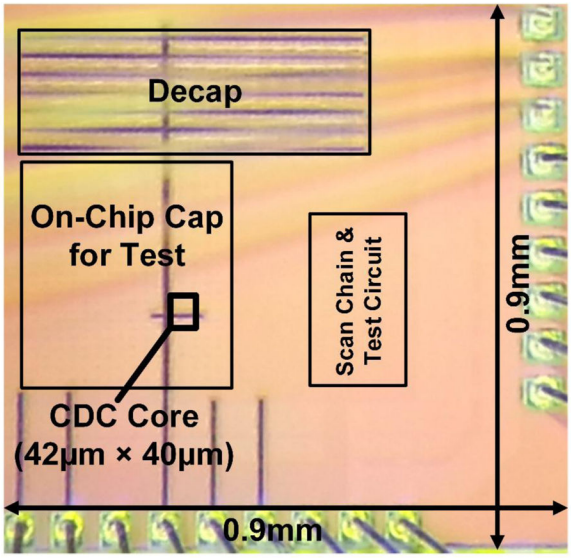
4 Input range is assumed to be 0.7pF – 11.3pF for this calculation

5 Estimated number from the paper

N/R: Not reported

Figure 6.

Performance summary and comparison.



Number of Gates in CDC Core

	Core w/o Counter	Counter	Total
Inverter	63	104	167
Buffer	4	0	4
Pass Transistor	2	0	2
Transmission Gate	1	0	1
Nand2	25	52	77
Nand3	4	0	4
Level Converter	3	0	3
Flip-Flop	0	52	52

Figure 7.
Die micrograph of the 40nm CMOS test chip.