Guest Editorial
Special Section on the 2014 IEEE Custom Integrated Circuits Conference (CICC 2014)

THIS Special Section of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS (TCAS-I) consists of expanded versions of six papers presented at the Custom Integrated Circuits Conference (CICC), held in San Jose, CA, USA, in September 2014. These papers were selected among those which belong to the area of interest of TCAS-I and which demonstrated the highest quality according to the feedback and scores given by CICC TPC members. The submitted follow-up manuscripts were peer reviewed and a final selection was done based on the results of the review process. This section complements the special issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. The papers are briefly described below and organized according to their main topics. The guest editors thank the authors for their contribution and the reviewers for their prompt and constructive feedback.

I. ANALOG MODELING AND CIRCUIT DESIGN

The first two papers of this section deal with analog modeling techniques. In the first one, Lu *et al.*, from IBM, propose a model of the resistance of local interconnects used in FinFET technologies. The model considers the parasitic resistances in source/drain regions of FinFET transistors, covering both unmerged and fully merged structures. A comprehensive analysis of the mathematical expressions included in the model is presented and the derived compact model is used in the extraction layout flow of a 14-nm technology.

In the second paper, Jang *et al.*, from Seoul National University, present a way to simulate injection-locked oscillators (ILOs) in an event-driven logic simulator such as System Verilog, based on a perturbation projection vector (PPV) model. This approach allows to simulate the nonlinear phase response of ILOs by representing analog signals as linear combinations of complex exponential basis functions, thus computing the system response algebraically in the Laplace S-domain. As a result, the transient simulation is drastically reduced without sacrificing accuracy.

In the next paper, Zarate-Roldan *et al.*, from Texas A&M University, present a power management unit (PMU) consuming less than 3 μW for an energy harvesting system based on a thermoelectric generator array. The proposed PMU structure is made up of a boost DC-DC switching converter followed by a low dropout voltage regulator, achieving -40 dB switching-noise suppression with 57% end-to-end efficiency.

In the last paper of this section, Kundu *et al.*, from Intel Corp., Purdue University, Qualcom Inc. and Carnegie Mellon University, present a clock-skew tolerant 16$\times$ time-interleaved SAR ADC intended for WiGig (60-GHz WLAN) standard requirements. The chip, integrated in 40 nm CMOS, achieves an ENOB of over 6 bit when clocked at 2.64 GS/s with a power consumption of 39 mW.

II. RF CIRCUITS

This section includes two papers related to different applications of RF circuits and systems. In the first paper, Elhadidy *et al.*, from Texas A&M University, present a wide-band PLL-based complex dielectric spectroscopy system integrated in 0.18 μm CMOS. The proposed sensing system utilizes two ring oscillators for precise permittivity measurement over a 0.7–6 GHz frequency range. Characterization of materials permittivity is achieved with frequency-shift measurements between a sensing oscillator and an amplitude-locked loop. The system occupies 6.25 mm^2 area and features a 3.7% maximum permittivity error.

Finally, Choi *et al.*, from Columbia University, present a pulsed 33-GHz radio transmitter integrated in 32-nm SOI CMOS. The chip operates with an electrical power supply of only 130 mV, dissipating 3.1 nW. These power levels—achieved through extreme-duty-cycling (10^{-6}) of an LC millimeter-Wave oscillator—are comparable to those present in cellular and intracellular membranes, what makes the presented chip especially suited for implanted medical devices.

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His main research interests are in the field of analog and mixed-signal integrated circuits, including analysis, behavioral modeling, and design automation of such circuits. In these topics, Dr. de la Rosa has participated in a number of National and European research and industrial projects, and has coauthored 5 books and some 200 international peer-reviewed publications, including journal and conference papers and book chapters.

Dr. de la Rosa is a Member of the Executive Committee of the IEEE-Spain Section, and a member of the Analog Signal Processing Technical Committee of the IEEE Circuits and Systems Society, where he serves as the Secretary of the Spanish Chapter. He serves as Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS, where he received the 2012–2013 Best Associate Editor Award and served as Guest Editor of the Special Issue on Custom Integrated Circuits Conference (CICC) in 2013. He is also a member of the Steering Committee of IEEE MWSCAS and he has also served and is currently serving as a review committee member of IEEE ISCAS conference. He participated and is currently participating in the organizing and technical committees of diverse international conferences, among others IEEE ISCAS, MWSCAS, IEEE ICECS, IEEE LASCAS, IFIP/IEEE VLSI-SoC, and DATE. He served as TPC chair of IEEE MWSCAS 2012, IEEE ICECS 2012, and IEEE LASCAS 2015.

Patrick Chiang received the B.S. degree in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 1998, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 2001 and 2007, respectively. He is currently an associate professor at Oregon State University, Corvallis, OR, USA.

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He is the recipient of a 2010 Department of Energy Early CAREER award and a 2012 NSF-CAREER award, for energy-efficient interconnects and robust near-threshold computing. He is an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and on the technical program committee for the IEEE Custom Integrated Circuits Conference and Asian Solid-State Circuits Conference. His research group has published more than 100 conference/journal papers in the area of energy-efficient circuits and systems, including: energy-efficient wireline and wireless transceivers, silicon photonics and 25 G optoelectronic transceivers, reliable near-threshold computing, and energy-constrained biomedical sensors.

Lawrence T. Clark (SM'01) received the B.S. degree in computer science from Northern Arizona University, Flagstaff, AZ, USA, in 1984, and the M.S. and Ph.D. degrees in electrical engineering from the Arizona State University, Tempe, AZ, USA, in 1987 and 1992, respectively.

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Prof. Clark has been awarded over 100 patents and has published over 110 refereed technical papers and seven book chapters. He has been an Associate Editor of TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS and twice Guest Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS. He is a Member of the IEEE Computer Society and ACM.