A Current-Mode Capacitively-Coupled Chopper Instrumentation Amplifier for Biopotential Recording with Resistive or Capacitive Electrodes

Hui Wang, *Student Member, IEEE*, and Patrick P. Mercier, *Senior Member, IEEE*

***Abstract*—This paper presents a high-density, low-noise analog front-end (AFE) for capacitively-coupled neural recording applications. Conventional capacitively-coupled AFEs, when chopper-stabilized, require large coupling capacitors or servo loops to minimize $1/f^2$ input-referred noise and chopper-induced offsets, limiting channel density. In this paper, a current-mode capacitively-coupled chopper instrumentation amplifier (C^4IA) with embedded delta-sigma ADC is presented that enables an area-efficient low-noise design via chopper-stabilized current-mode amplification. In this design, 60 channels are implemented in a 2×2 mm^2 180 nm CMOS chip, and each channel consumes 4 μW, achieves an input referred noise of 160 nV/$\sqrt{Hz}$, and an ADC ENOB of 8.5 bits.**

***Index Terms*—Neural recording, analog front-end, chopping, instrumentation amplifier, current-mode, non-contact.**

I. Introduction

MODERN neural recording devices strive to increase channel density in order to simultaneous track the activities of large populations of neurons. Most current approaches tend to separate electrodes from electronic front-ends [1], which require complex packaging and limit achievable global electrode density across the entire brain, as area occupied by electronics is area that cannot be occupied by more electrodes. To maximize global electrode density, an alternative approach involves integrating electrodes directly on top of small modular CMOS chips by coating the chip and top-metal electrodes with a biocompatible encapsulant [2], [3]. Placing analog front-ends (AFEs) directly underneath these capacitive electrodes [3] can then offer high global electrode density along with natural DC offset rejection. However, capacitive electrodes, when used in conjunction with conventional chopping circuits for area-efficient flicker-noise reduction, suffer from a parasitic switched-capacitor resistance at the amplifier input that presents two important area-reduction challenges: 1) the parasitic resistance introduces offsets that must be canceled through a servo loop with large passives; and 2) noise of the parasitic resistance, when input-referred, results in a $1/f^2$ shape, which requires large coupling capacitors or an unattainably large parasitic resistance to minimize its effect [4].

To minimize area and noise in a capacitively-coupled AFE, this paper presents an architecture that uses both input coupling capacitors and chopper-stabilization without large input-referred chopper-induced noise or servo loops. This is achieved by placing the chopper after the coupling capacitor but outside of the feedback loop of the first amplifier, resulting in current mode amplification. The proposed current-mode capacitively coupled chopper instrumentation amplifier (C^4IA) is then converted back to voltage mode signals via a capacitive integrator, and digitized with an area-efficient delta-sigma ADC for a complete AFE that can be both small and offer low-noise/power. This paper describes the AFE design, and presents measurement results from a 60-channel chip.

Hui Wang and Patrick P. Mercier are with the Department of Electrical and Computer Engineering, University of California at San Diego, 9500 Gilman Dr., 0407, La Jolla, CA (e-mail: huiwang@ucsd.edu; pmercier@ucsd.edu).

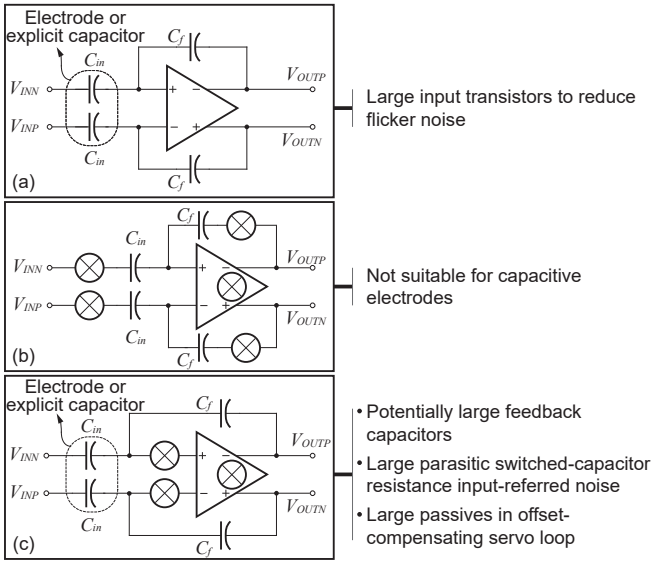


Fig. 1. Conventional capacitively-coupled analog front-end architectures.

II. Current-Mode Capacitively Coupled Chopper Instrumentation Amplifier (C^4IA)

A. Conventional Capacitively-Coupled AFEs

The most common instrumentation amplifier for neural recording is based on the capacitive feedback topology illustrated in Fig. 1(a) [5]. Since local field potential (LFP) neural signals have significant low-frequency content, conventional capacitive feedback AFEs use large input devices to minimize flicker noise at the cost of channel density.

Chopper-stabilization is a popular technique to reduce input device sizes [6], [7]. In AC-coupled AFEs, choppers can be placed in one of two locations: before or after the input coupling capacitors, C_{in}. Chopping before C_{in} (Fig. 1(b)) is not generally appropriate for capacitive electrodes, as explicit

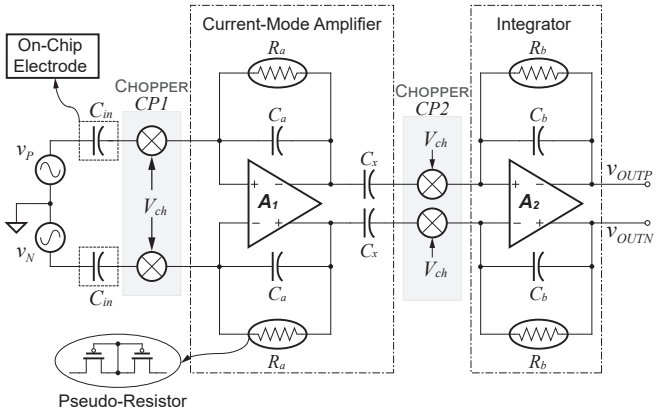


Fig. 2. Schematic of the proposed C^{4}IA structure.

coupling capacitors are then needed (instead of incorporating into the electrodes themselves). Instead, most AC-coupled chopper-stabilized AFEs place the choppers after C_{in} as shown in Fig. 1(c) [4]. However, the choppers together with the parasitic gate capacitance of the amplifier form a relatively low-impedance parasitic switched-capacitor resistance that, when reflected across C_{in} to the input, presents significant $1/f^2$ noise. In addition, the parasitic resistance introduces DC-offsets, which must be stabilized within a servo-loop that typically requires large filtering capacitance. All of these issues serve to limit channel density.

B. Current-Mode Capacitively Coupled Chopper Instrumentation Amplifier (C^{4}IA): Design Details & Analysis

Design Details: To enable chopping in an AC-coupled architecture, in the proposed design the choppers are placed after the input coupling capacitors, but outside of the feedback loop of the amplifier, as shown in Fig. 2. Specifically, the neural signal passes through coupling capacitors, C_{in}, which due to the virtual ground of amplifier A_1, effectively converts to a current signal and passes through feedback capacitors, C_a, though not before being up-converted to frequency f_{ch} by chopper $CP1$. After passing through C_a, the signal is converted back to a voltage, and then passed through another set of coupling capacitors, C_x, which, due to the virtual ground of amplifier A_2, converts the signal back to a current, though not before being chopped back down to baseband by $CP2$. The output signal is created by passing the baseband current signal through feedback capacitors C_b, creating output voltages $V_{OUT,P/N}$. Since the virtual ground conditions *after* the coupling capacitors and choppers convert input voltage signals to currents, the proposed design is considered to be a current-mode amplifier, as in [8]. Note that though [9] also placed the first chopper outside of the feedback loop, the amplification is achieved in the voltage domain, necessitating a complex amplifier to accommodate the large voltage swing across the third chopper.

C^{4}IA Analysis: To show that the C^{4}IA can amplify neural signals while enabling low-noise capacitively-coupled chopper-stabilization, this subsection analyzes the overall signal and noise transfer functions. To simplify analysis, Fig. 3(a) shows a single-ended representation of the circuit in Fig. 2; an equivalent block diagram is shown in 3(b). Since the choppers fall outside of the amplifier feedback, the analysis in [4] does not apply and block diagram components must be frequency-translated. For example, when a current, $i = v(s)sC$, is chopped at frequency f_{ch}, the resulting signal observed at the chopping frequency band can be represented by $v(s\pm jw_0)(s\pm jw_0)C$, where '$-$' is for up conversion and '$+$' is for down conversion. The effect on capacitively coupled input signals (Fig. 3(c) and Fig. 3(e)) can then be effectively modeled by the block diagrams in Fig. 3(d) and Fig. 3(f), respectively. With this in mind and typically $C_{in} \gg C_a \gg C_{p,1}$, the node impedance at the input of the first amplifier (Fig. 3(b)), Z_a, is given by:

$$Z_a \approx \frac{1}{(s-j\omega_0)C_{in}+G_a} = \frac{1}{C_{in}(s+\omega_{in,1})}, \tag{1}$$

where $\omega_{in,1}$ is defined in Fig. 3(g). Similar analysis applies to the calculation of Z_b. To further simplify Fig. 3(b), the transfer functions of the op-amps, $A_1(s)$ and $A_2(s)$, are modeled as having large DC gains, $A_{1,0}$ and $A_{2,0}$, and a single dominant pole at $\omega_{1,0}$ and $\omega_{2,0}$, respectively. Therefore, the block diagram in Fig. 3(b) can be simplified as depicted in Fig. 3(f) for $v_{IN}(s)$ to $v_{INT}(s)$, and in Fig. 3(g) for $v_{INT}(s)$ to $v_{OUT}(s)$. The loop gains, $LG_1(s)$ and $LG_2(s)$ are shown in Fig. 3(g) and (h), respectively. Since the first stage (Fig. 3(f)) operates at a higher frequency band (chopping frequency band), the low pass corner frequency of the overall system, ω_{lp}, is determined by the bandwidth of $LG_1(s)$, which is dominated by the unity gain bandwidth of the first stage operational amplifier. Since the loop gains in Fig. 3(g) and (h) are much larger than unity in the frequency of interest ($< \omega_{lp}$), the closed-loop transfer functions, $H_{CL,1}(s)$ and $H_{CL,2}(s)$, thus can be approximated by the inverse of the feedback factor, which is given in Fig. 3(g) and (h). The end-to-end transfer function is then given by:

$$H(s) = \frac{sC_{in}}{(s+j\omega_0+\omega_{hp,1})C_a}\frac{(s+j\omega_0)C_x}{(s+\omega_{hp,2})C_b}, \tag{2}$$

where $\omega_{hp,1}$ and $\omega_{hp,2}$ are defined in Fig. 3. Since the chopping frequency $\omega_0 \gg \omega_{hp,1}$:

$$H(s) \approx \frac{sC_{in}C_x}{(s+\omega_{hp,2})C_bC_a}. \tag{3}$$

As indicated by (3), the high pass corner frequency is determined by $\omega_{hp,2}$ with a zero at the origin.

The transfer function for each noise source $(v_{n,Ra}, v_{n,A1}, v_{n,Rb}, v_{n,A2})$ referred to the input are given by:

$$\frac{v_{IN}(s)}{v_{n,Ra}(s+j\omega_0)} = \frac{G_a}{sC_{in}}, \tag{4}$$

$$\frac{v_{IN}(s)}{v_{n,A1}(s+j\omega_0)} = \frac{s+j\omega_0+\omega_{in,1}}{s} = \frac{s+\frac{1}{R_aC_{in}}}{s}, \tag{5}$$

$$\frac{v_{IN}(s)}{v_{n,Rb}(s)} = \frac{(s+j\omega_0+\omega_{hp,1})C_aG_b}{s(s+j\omega_0)C_{in}C_x}, \tag{6}$$

$$\frac{v_{IN}(s)}{v_{n,A2}(s)} = \frac{(s+\omega_{in,2})(s+j\omega_0+\omega_{hp,1})C_a}{s(s+j\omega_0)C_{in}}. \tag{7}$$

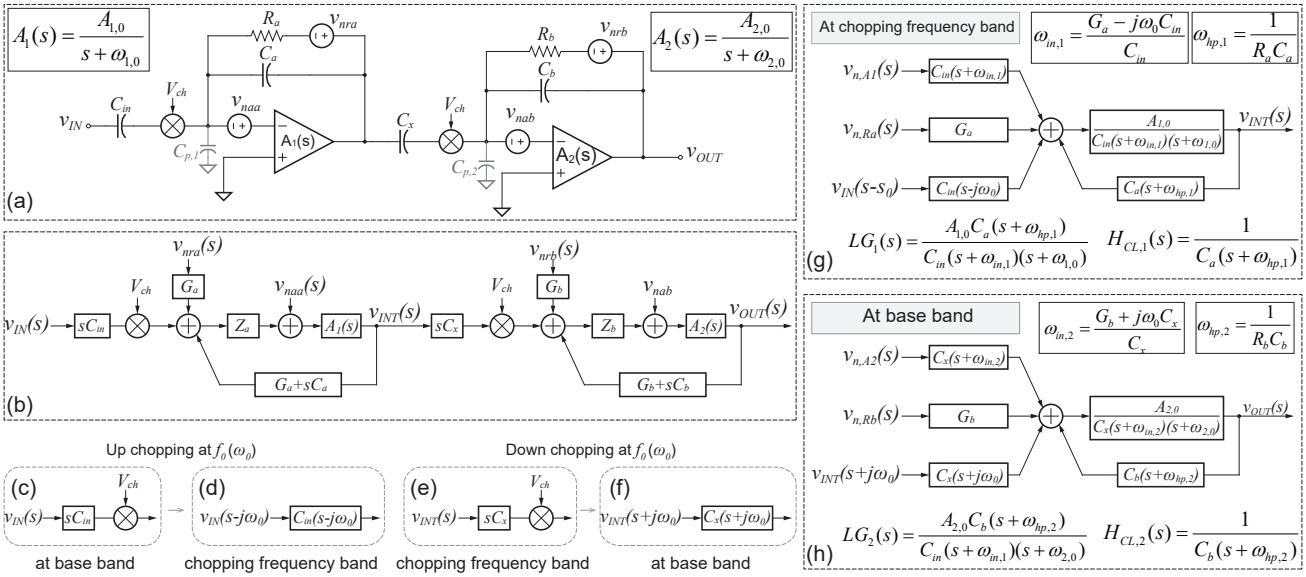


Fig. 3. Equivalent single-ended model of the C^{4}IA. (a) Block diagram of the single-ended model. (c-d) Frequency translation of v_{IN}. (e-f) Frequency translation of v_{INT}. (g) Block diagram from v_{IN} to v_{INT} at chopping frequency. (h) Block diagram from v_{INT} to v_{OUT} at base band.

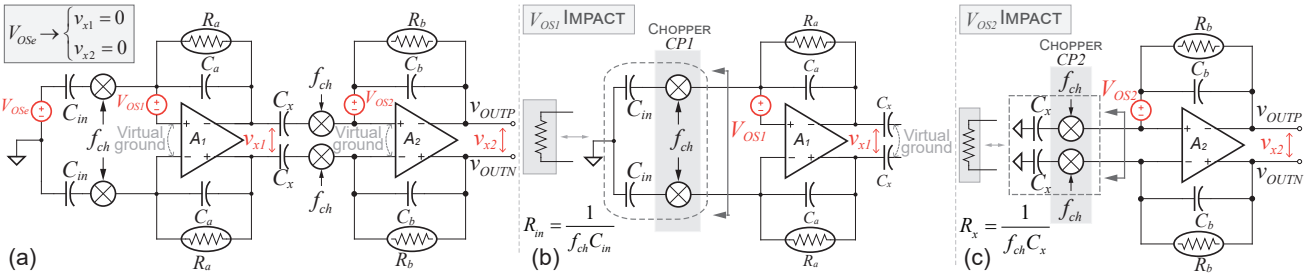


Fig. 4. Simplified offset model of the proposed structure (a), effect of V_{OS1} on A_1 and A_2 (b), and effect of V_{OS2} on A_1 and A_2 (c).

Since R_a and R_b are large white noise generating bias resistors (MOS-bipolar pseudoresistors), (4) indicates that R_a contributes negligible noise, while the noise of R_b is suppressed by the gain of the current-mode amplifier as shown in (6). Equation (5) indicates that the low frequency noise component of the first-stage operational amplifier is moved out of the frequency band of interest, which is in good accordance with the function of chopping action. In addition, (5) reveals a $1/f$ noise for frequency below the corner frequency $\omega_{n,corner} = 1/R_aC_{in}$. By appropriately choosing the values of C_{in}, R_a, C_b, and R_b, $1/f$ noise can be moved out of the bandwidth of interest, i.e., $\omega_{n,corner} < \omega_{hp,2}$ in (3). Meanwhile, the noise of the second-stage operational amplifier is significantly suppressed since C_{in} is much larger than C_a when referred to the input as shown in (7).

Capacitors C_{in} and C_x in the proposed topology are serving to continuously modulate the signal via the chopping action of $CP1$ and $CP2$ which are operating in continuous time instead of periodically sampling and holding input voltages, thus avoiding kT/C noise [6]. Importantly, chopper $CP1$ is located immediately next to the virtual ground node of A_1, and thus the parasitic switched-capacitor resistance in [4], which ultimately creates large $1/f^2$ noise when input-referred (and can only be reduced by employing very large input coupling capacitors), is shorted out and therefore significantly reduced.

C. C^{4}IA Offset Analysis

The C^{4}IA architecture naturally rejects electrode offset voltages, V_{OSe} in Fig. 4(a), due to its capacitively-coupled nature. However, the input-referred offset voltages of A_1 and A_2, V_{OS1} and V_{OS2}, can still potentially affect the operation of the circuit and should be considered carefully.

For example, V_{OS1} can get amplified due to the switched capacitor resistance R_{in} introduced by chopper $CP1$ and C_{in}, as shown in Fig. 4(b), and $R_{in} = 1/f_{ch}C_{in}$. Note that V_{OS1} is isolated from A_2 by C_x and thus does not affect the operation of A_2. Similar analysis applies to V_{OS2}, where, as shown in Fig. 4(c), V_{OS2} gets amplified at the output of A_2 due to the switched capacitor resistance R_x introduced by $CP2$ and C_x. Fortunately, the output can then also be AC-coupled so as to not affect the operation of a following circuit. The total offset voltages at outputs of A_1 and A_2 due to V_{OSe}, V_{OS1}, and V_{OS2}, as shown in Fig. 4, can thus be calculated by:

$$\begin{cases} v_{x1|total} = V_{OS1}(1 + 2f_{ch}C_{in}R_a) \\ v_{x2|total} = V_{OS2}(1 + 2f_{ch}C_xR_b) \end{cases} \tag{8}$$

While AC coupling capacitors block offsets between stages, (8) shows that the offset should still be sufficiently small so as

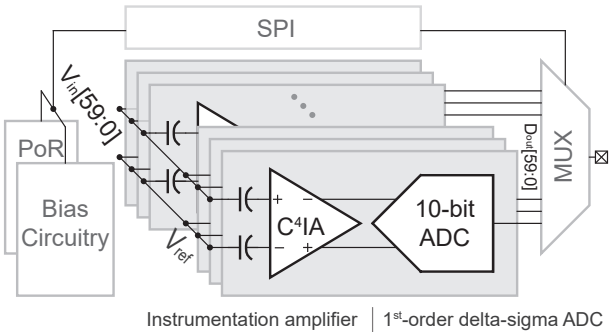


Fig. 5. Architecture of the fully integrated neural acquisition platform.

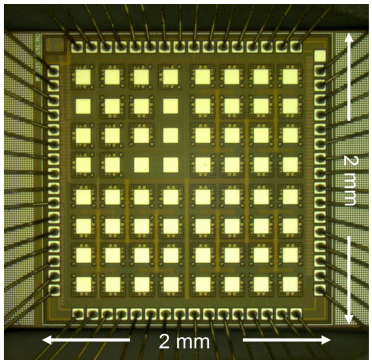


Fig. 6. Micrograph of the 60-channel neural acquisition chip.

to not saturate the output of the amplifiers. Design techniques such as symmetric/common centroid layouts can suppress the output offset voltages of A_1 and A_2 to ensure appropriate DC operating points.

III. Neural Acquisition Platform Architecture

The architecture of the overall neural acquisition platform is shown in Fig. 5. In this design, 60 C^{4}IAs are each integrated with an area-efficient first-order delta-sigma ADC for digitization. Since neural signals have relatively low bandwidth, delta-sigma ADCs with first-order noise shaping can easily achieve large oversampling ratios (OSRs) of 128 or more at low-power, resulting in a much more area-efficient design than a SAR ADC (even if analog multiplexing between channels is employed). The digital outputs of the 60 channels can then be digitally multiplexed and serialized. Bias generators are implemented on chip to provide bias for all 60 channels and on-chip power-on-reset (PoR) blocks ensure the circuit enters a correct initial state at power up.

IV. Chip Fabrication & Experimental Results

A die photograph of the 60 channel chip, implemented in 180nm SOI, is shown in Fig. 6. The active electronics of each channel occupy 0.03 mm^2, and lie directly underneath 0.1 mm $\times$ 0.1 mm electrodes implemented in top metal. The center electrode is used as a reference, while the area underneath three other central electrodes are used to implement peripheral circuitry (e.g., mux, bias generators, PoR, etc.). High-k materials coating the top-metal electrodes such as TiO_2 and PEDOT-PSS offer capacitive densities $>$ 100 nF/mm^2, enabling $>$ 1 nF

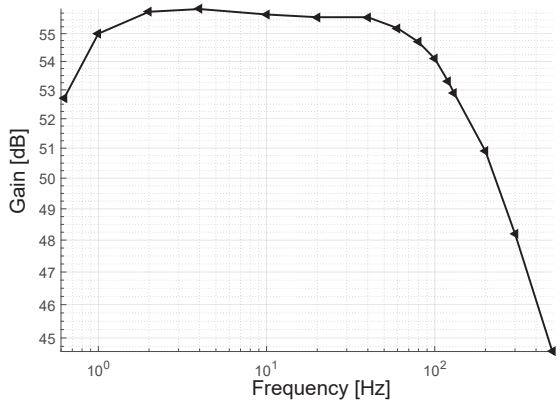


Fig. 7. Measured gain transfer function of the proposed C^{4}IA.

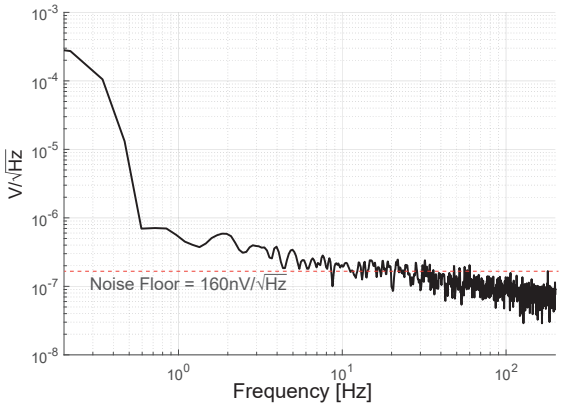


Fig. 8. Measured input-referred noise spectrum of the proposed C^{4}IA.

of C_{in} per electrode. The C^{4}IA gain is adjustable by tuning C_x (Fig. 2), implemented as a 3-bit binary weighted array, to compensate for the variation of input capacitance C_{in}. To facilitate benchtop testing, 1 nF discrete capacitors are used to characterize the analog front-end. Unfortunately, the layout of amplifiers A_1 and A_2 were not performed as carefully as they could have been, resulting in larger input-referred offset voltages than originally expected (post-layout Monte Carlo analysis reveals offset voltages of 620 μV). Simulation and measurements with these offset voltages tend to rail the amplifier outputs, as described in Section. II-C. To compensate, off-chip resistors are employed to help stabilize the loops for benchtop measurements. Simulation results reveal that offset voltages under 100 μV, easily achievable with more careful layout, would obviate the need for these resistors.

Operating from a 0.8 V supply, the proposed C^{4}IA consumes 4 μW and the ADC consumes 0.8 μW. Fig. 7 shows the measured transfer function, where a gain of 56 dB is observed. It shows a band pass characteristics which is in accordance with the analysis in Section II with a high pass corner frequency of 0.6 Hz and a low pass corner of 130 Hz. Fig. 8 shows the measured input-referred noise where an input-referred noise power spectral density (PSD) of approximately 160 nV/$\sqrt{Hz}$ is observed. Large flicker noise and/or DC offsets are observed at frequencies $<$ $\sim$0.5 Hz, which is

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF NEURAL ACQUISITION INSTRUMENTATION AMPLIFIERS

	DC-Coupled			AC-Coupled		
	JSSC2007 [6]	**JSSC2011 [7]**	**JSSC2015 [1]**	**JSSC2003 [5]**	**JSSC2010 [4]**	**This Work**
Supply Voltage (V)	1.8	1	0.5	5	1	**0.8**
Amp. Power (μW/ch)	2	1.8	2.3	0.9	3.5	**4**
Noise PSD (nV/$\sqrt{Hz}$)	100	60	58	290	130	**160**
Bandwidth (Hz)	0.5-250	0.5-500	1-500	0.025-7.2k	0.5-100	**0.6-130**
NEF	4.6	3.3	4.76$^{£}$	4	9.4	**13.7**
PEF	38.1	10.89	11.3$^{£}$	80	88.3	**187.7**
Area (mm^2/ch)	1.7*	0.1‡	0.025	0.16‡	0.3†	**0.03**$^{⋆}$
ADC resolution (bits)	None	None	15	None	12	**10**
Number of Channels	1	1	64	1	1	**60**
Electrode Type	Separate Resistive Electrode	N/A	Separate Resistive Electrode	Separate Platinum-Tipped Electrode	Separate Resistive Electrode	**On-chip Capacitive Electrode**
Compatible with Capacitive Electrodes	No	No	No	Yes	Yes	**Yes**
Technology	0.8 μm	65 nm	65 nm	1.5 μm	0.18 μm	**0.18 μm**

* With on-chip capacitor; $^{£}$ Include ADC; † Input capacitor C_{in} and servo loop filter passives are not included.
‡ ADC area is not included; $^{⋆}$ In this prototype, off-chip resistors are employed in the measurement to help stabilize the loop.

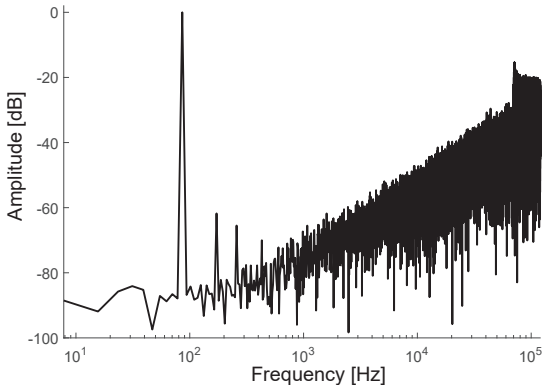


Fig. 9. Measured power spectrum of the ADC with an OSR = 128.

in good accordance with (5). Unfortunately, a lower than designed chopper frequency (f_{ch} = 2 kHz) was used in the measurement to help relieve the aforementioned offset challenge. This frequency was not quite enough to amplify signals beyond the corner frequency of A_1, and thus some $1/f$ noise is still observed at mid-band in Fig. 8. However, chopping does reduce the overall magnitude of this noise by over 50×, which is sufficient to meet the needs of the present application. Importantly, in-band $1/f^2$ noise was not observed anywhere, confirming that the proposed architecture addresses the issue of significant noise from input-referred switched-capacitor resistance in [4], in good accordance with previous analysis. Note that while the proposed topology exhibits a promising area reduction (e.g., 10× smaller), thereby enabling high-density fully-integrated capacitively monitoring of the biopentential signals, this comes as a trade-off with power efficiency factor (PEF), since A_1 must operate at a higher frequency due to chopping (with a unity gain bandwidth of 2.7 MHz). Table I summarizes the measured performance and compares the proposed design to state-of-the-art DC-and AC-coupled designs. The ADC is measured to achieve an ENOB of 8.5 bits when operating at an OSR of 128. The measured output power spectrum of the ADC is shown in Fig. 9.

V. CONCLUSIONS

This paper presented a 4 mm^2 60-channel capacitive neural recording chip that achieves both small area and low-noise through a current-mode chopper-stabilized AFE architecture. Implemented in 180 nm, each AFE channel, consisting of a C^{4}IA and a first order delta-sigma ADC, consumed 4.8 μW, and had an input-referred noise PSD of 160 nV/$\sqrt{Hz}$. Unlike conventional AC-coupled chopper-stabilized architectures, which necessitate large capacitors to achieve low-noise and stable operation, the proposed C^{4}IA approach enables chopping with capacitive coupling in an area-efficient manner.

VI. ACKNOWLEDGMENT

The authors would like to acknowledge the Center for Brain Activity Mapping and the University of California MRPI program for financial support.

REFERENCES

[1] R. Muller *et al.*, "A Minimally Invasive 64-Channel Wireless μECoG Implant," *IEEE Journal of Solid-State Circuits*, no. 1, pp. 344–359, 2015.
[2] M. Eickenscheidt *et al.*, "Electrical stimulation of retinal neurons in epiretinal and subretinal configuration using a multicapacitor array," *Journal of Neurophysiology*, vol. 107, no. 10, pp. 2742–2755, 2012.
[3] S. Ha *et al.*, "A 16-channel wireless neural interfacing SoC with RF-powered energy-replenishing adiabatic stimulation," in *2015 Symposium on VLSI Circuits (VLSI Circuits)*. IEEE, Jun 2015, pp. C106–C107.
[4] N. Verma *et al.*, "A Micro-Power EEG Acquisition SoC With Integrated Feature Extraction Processor for a Chronic Seizure Detection System," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 804–816, Apr 2010.
[5] R. Harrison and C. Charles, "A low-power low-noise cmos for amplifier neural recording applications," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, 2003.
[6] T. Denison *et al.*, "A 2 μW 100 nV/rtHz Chopper-Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials," *IEEE Journal of Solid-State Circuits*, no. 12, pp. 2934–2945, 2007.
[7] Q. Fan *et al.*, "A 1.8 μW 60 nV/$\sqrt{Hz}$ Capacitively-Coupled Chopper Instrumentation Amplifier in 65 nm CMOS for Wireless Sensor Node," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1534–1543, 2011.
[8] G. Ferrari *et al.*, "Transimpedance Amplifier for High Sensitivity Current Measurements on Nanodevices," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1609–1616, May 2009.
[9] T. Yoshida *et al.*, "A 1V supply 50nV/Hz noise PSD CMOS amplifier using noise reduction technique of autozeroing and chopper stabilization," in *Digest of Technical Papers. 2005 Symposium on VLSI Circuits, 2005.*, pp. 118–121.

TCAS-II-01449-2017 Manuscript – Response to Reviewers Comments

Title: A Current-Mode Capacitively-Coupled Chopper Instrumentation Amplifier for Biopotential Recording with Resistive or Capacitive Electrodes

Authors: Hui Wang, Patrick P. Mercier

Thank you for taking the time to read our paper and providing some useful feedback - we truly appreciate it. You will find our responses below in blue, bolded font.

Reviewer 1

Technical Comments to the Author

In this submission, the authors have modified the manuscript accordingly to previous questions and concerns. There are, however, some important points needs to be clarified before acceptance. I would highly suggest that the authors can reduce some analysis that is similar in ref4 and explain the difference/advantage/purpose/issues.

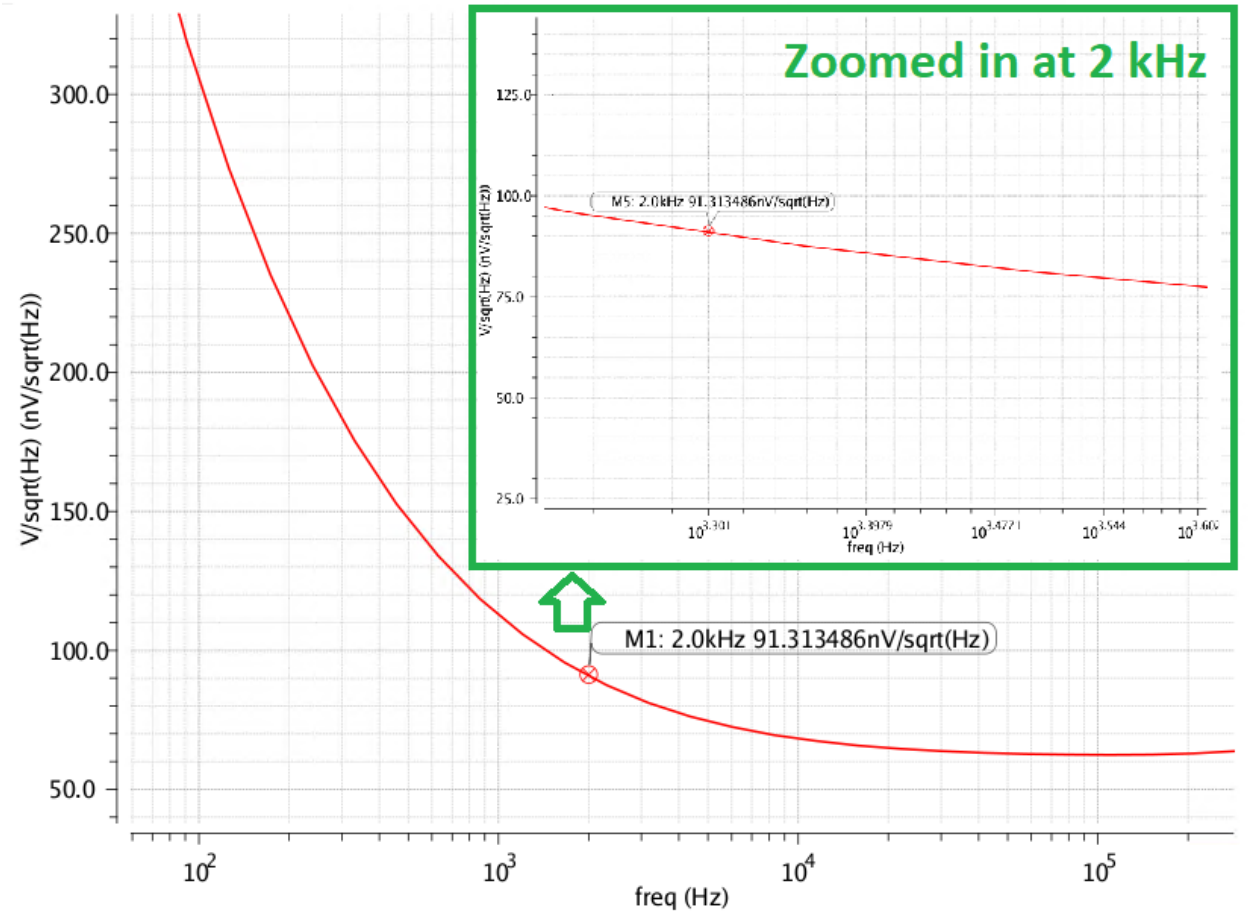
Thanks for your suggestions – we have deleted the original Equations (1) and (3) to reduce the length of analysis here to instead better focus on the differences.

1. The most critical issue is in result Fig 8, while the author claims that the flicker noise is filtered out above 0.5 Herts. But it seems that below 0.5 Hz it is DC leakage during sampling and FFT? Also there is clear, almost 1/f Slope for the voltage from 1 to 100 Hz? The claims on the flicker noise reduction is then very confusing.

Thanks for your comment. The 1/f noise (and DC content) at frequencies below 0.5 Hz is expected as predicated by Equation (5) which reveals 1/f noise for frequency lower than high pass corner frequency, which can be introduced by DC leakage as you pointed out.

Also, there is indeed some 1/f noise above 0.5Hz, but it's at a much lower amplitude than if it were directly from the amplifier. The reason for this is that the employing chopping frequency of 2 kHz is lower than we originally designed for, in order to help relieve the offset challenge as indicated by Equation (9). This lower-than-desired frequency does not enable up-converted amplification at the thermal noise floor of the input referred noise of the first amplifier, $v_{n,A1}$, and instead amplification occurs close to, but on the left hand side, of its noise corner frequency (simulated $v_{n,A1}$ is shown below). Thus, chopping is not perfectly effective at eliminating the amplifier's 1/f noise. We point out, however, that it still helps – rather than seeing 1/f noise content from the amplifier at 0.5-160Hz, which would be large, we see it's 1/f noise content at 2-2.16kHz, which is much lower when folded down into baseband after down-chopping. Since $v_{n,A1}$ is the dominant noise source of the AFE (as indicated by Equation (5)), the noise from 2 kHz to 2.16 kHz of $v_{n,A1,}$ which is not white, will appear in the input referred noise of the overall system. However, this still helps, and the chopping action reduces the overall noise power contributed by $v_{n,A1}$ by over 50x, since the amplifier's integrated noise power from 0.5 to 160 Hz of is 62.2 $(\mu V)^2$(input-referred), and noise power from 2 kHz to 2.16 kHz is 1.2 $(\mu V)^2$(input-referred).

New text was added in the measurement section to include the above discussion to be very clear where the displayed noise sources are coming from.



2. The KT/C noise is till not explained well. To be clear it is the noise of parasitic resistance in the chopper. In the response letter the authors referenced the T.Denison JSSC2008. However it is mainly about the sampling noise. Please either reference or give analysis and explain why the chopper noise can be ignored rather than ref4. Also authors claimed that the 1/f^2 noise is not found, proving the chopper noise is not presented. However without knowing the detail of chopper frequency and thermal noise level of gm it is difficult to argue this noise is covered by the thermal noise of feedback or A1. Also more interestingly when the noise power is 1/f^2, the voltage magnitude density is 1/f (maybe it is the reason in question 1?).

Thanks for the comment. As pointed out by T. Denison JSSC2008, the capacitors C_{in} and C_x do not introduce kT/C noise since they are serving to continuously modulating the input signal, instead of sampling and holding the input signals. I think we both agree on this.

We believe your question is thus primarily related to the noise of the parasitic switched-capacitor resistance generated by the chopper. In [4], the chopper is placed right before the inputs of the amplifier, and since the chopper moves charge back and forth between the inputs of the amplifier, which has finite parasitic capacitance, the voltage on the capacitance of the two amplifier terminals is not equal to each other at all times. As a result, a net current (modeled by the switched-capacitor resistance) results that flows between the terminals of the op-amp. This parasitic resistance can be modeled to generate thermal-equivalent noise (at frequencies below the chopping frequency), which, when input-referred across the coupling capacitor, becomes colored, as effective 1/f^2 noise.

This is the principal challenge with capacitively-coupled chopped-amplifiers in area-constrained applications, as the only way to reduce this 1/f^2 noise is to employ very large coupling capacitors, which was the solution utilized in [4]. This is in fact the primary reason for the present work, which proposed an alternative AFE architecture to overcome this challenge.

Specifically, in the proposed topology, the chopper is placed outside the feedback loop. The two inputs of the amplifier are now at virtual ground, thus effectively shorting out the parasitic capacitance, and therefore the effects of any switched-capacitor resistor. This is also in accordance with Fig. 8 since: 1) the input referred noise at 1 Hz is ~500 nV/sqrt(Hz) and ~50 nV/sqrt(Hz) at 100 Hz. Therefore, the noise power reduces by 100x (i.e., noise voltage reduces by 10x) from 1 Hz to 100 Hz, indicating that is 1/f noise, not 1/f^2 noise; 2) in the implementation, the switched-capacitor resistor (ignoring the virtual ground condition) would be equal to $1/f_{ch}C_p$, which is ~1 GΩ which (C_p = 490 fF and f_{ch} = 2 kHz), alone, would introduce ~650 nV/sqrt(Hz) input referred 1/f^2 noise at 1 Hz according to [4] with input capacitors C_{in} = 1 nF. However, this is not observed in Fig. 8, which instead shows a *total* input referred noise of ~500 nV/sqrt(Hz) at 1 Hz, and a 1/f shape, as expected, and not a 1/f^2 shape, were it from the switched-capacitor resistor. For these reasons, we think that the proposed AFE is indeed not adversely affected by the noise of the parasitic switched-capacitor resistor, especially given that we are employing small coupling capacitors. Again, this was the primary motivation for the entire design.

We do appreciate your comment, as the explanation of this was clearly not as well done as it could be. Per your comments, the last paragraph of Section II.B was rewritten and new text was added in the measurement section to more clearly describe what is happening here.

3. It is still confusing to call it current mode. Explanation(pg2,lin37-40) given is not enough to support the claim. By removing the choppers, the proposed front end is essentially a two stage ac couple amplification, without any small signal current (except gm) passing the transistors to form current mode operation.

Thanks for the comment. We rewrote the first paragraph of Section II.B by explicitly saying that the neural signal passes through coupling capacitors, C_{in}, which due to the virtual ground of amplifier A1, effectively converts to a current signal and passes through feedback capacitors, Ca, though not before being up-converted to frequency f_{ch} by CP1. After passing through C_a, the signal is converted back to a voltage, and then passed through another set of coupling capacitors, C_x, which, due to the virtual ground of amplifier A2, converts the signal back to a current, though not before being chopped back down to the baseband current signal through feedback capacitors C_b, creating output voltages $V_{OUT,P/N}$. Since the virtual ground conditions after the coupling capacitors and choppers convert input voltage signals to currents, the proposed design is considered to be a current mode amplifier, as in [8]. You're right that if the choppers are removed, these are just capacitive feedback amplifiers, which can be analyzed as either voltage mode or current mode. The fact that amplification occurs at a different frequency thanks to the chopping action makes it more convenient to analyze the circuit in the current mode. The following references employed similar current-mode structure for current sensing/recording:

G. Ferrari et al., "Ultra-low-noise CMOS current preamplifier from DC to 1MHz," Electronics Letters, vol. 45, no. 25, p. 1278, 2009.

M. Taherzadeh-Sani et al., "A 170-dB CMOS TIA With 52-pA Input-Referred Noise and 1-MHz Bandwidth for Very Low Current Sensing," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 5, pp. 1756–1766, May 2017.

D. Bianchi et al., "CMOS current amplifier for AFM impedance sensing on chip with ZeptoFarad resolution," in Proceedings of the 2013 9th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME).

M. Crescentini et al., "Noise Limits of CMOS Current Interfaces for Biosensors: A Review," IEEE Transactions on Biomedical Circuits and Systems, vol. 8, no. 2, pp. 278–292, Apr 2014.

G. Ferrari et al., "Transimpedance Amplifier for High Sensitivity Current Measurements on Nanodevices," IEEE Journal of Solid-State Circuits, vol. 44, no. 5, pp. 1609–1616, May 2009.

C.-Y. Wu et al., "A CMOS power-efficient low-noise current-mode front-end amplifier for neural signal recording." IEEE transactions on biomedical circuits and systems, vol. 7, no. 2, pp. 107–14, Apr 2013.

Some minor comments,

1. Explain the chopping frequency.

Thanks for pointing this out. The chopping frequency is 2 kHz and the related text is updated.

2. The font size in Figure 3/4 can be increased to show properly.

Thanks for the suggestion – the font size in Figs 3/4 is increased per your comments.

3. The bandwidth of proposed amplifier should be included, as it is important to analysis the results for power and chopper, give NEF of 13 and PEF of 187.

The unity gain bandwidth of the two amplifiers are 2.7 MHz and 450 kHz, respectively. The related text is updated accordingly.