ANALOG DEVICES

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APPLICATION NOTE

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Sampled Systems and the Effects of Clock Phase Noise and Jitter

by Brad Brannon

ABSTRACT

As higher resolution data converters capable of direct IF-sampling come to market, system designers need help making performance/cost trade-off decisions on low jitter clock circuits. Many of the traditional methods used to specify clock jitter are not applicable to data converters or at best reveal only a fraction of the story. Without a proper understanding of how to specify and design the clocking circuit, optimal performance of these new data converters may not be achieved. A simple jitter specification is rarely sufficient for making an informed clock selection. Rather, it is important to know the bandwidth and spectral shape of the clock noise so that this can be properly accounted for during the sampling process. Today many system designers are not adequately specifying the phase noise and jitter requirements for the data converter clock and, as a result, system performance is degraded. Picoseconds of clock jitter quickly translate to dBs lost in the signal path. However, in the opposite extreme, some designers may be paying too much for an expensive clock source simply because they are unclear on how clock noise affects the converter and ultimately their product's performance. Note that the most expensive clock generator does not always yield the best system performance. This application note explains many of the trade-offs related to jitter, phase noise, and converter performance. Once these trade-offs are understood, the best clock for the application may be selected and optimal performance at the lowest cost will result. After explaining how the sampling process works in a data converter, real application examples are given to illustrate the clock selection process.

HISTORY

One of the issues that arises most often regarding ADC applications is that of providing an encode source. As most engineers are aware, proper selection of the encode clock is most critical in attaining the best performance from the selected data converter. This is especially true with the sampled analog input frequencies continuing to increase as seen in recent years.

However, as the converters have moved closer to the antenna in these signal chains, the engineers using them have moved from the "mixed signal designer" to the "RF designer." Likewise, the design techniques and supporting components have also changed and the focus has shifted from time domain characteristics to frequency characteristics. In past times, the encode clock was just that—a clock. For IF and RF sampling systems, the encode source is now considered more of a local oscillator than a clock for reasons discussed in this application note. As such, many designers expect clock requirements to be specified in the frequency domain, just as they are for RF synthesizers.

While it is difficult to provide for direct correlation between clock jitter and phase noise, this application note provides some guidelines for designing or selecting encode sources from either a clock jitter or phase noise perspective. There are a number of articles available on translating between phase noise and jitter, and this application note may be useful in the validation of the process.

JITTER DEFINED

Since the primary purpose of a data converter is to take regular time samples and produce an analog, or to take an analog continuum and produce a series of regular time samples, stability of the sampling clock is very important. From a data converter perspective, this instability is called clock jitter and results in uncertainty as to when the analog input is actually sampled. Although there are several methods to measure clock jitter directly, as the clock stability requirements tighten up the requirement to measure sub-picosecond timing variations dictate that indirect measurement be used. From a converter perspective, note that the encode bandwidth can extend over many hundreds of MHz. Therefore, when considering the bandwidth of the noise that constitutes jitter for a data converter, the range is from dc to the encode bandwidth that exceeds far beyond the typical 12 kHz to 20 MHz numbers often quoted for standard clock jitter measurements.

Since the concern with jitter is reduced wideband converter noise performance, it is easy to estimate clock jitter by observing the degradation in noise performance of a converter. SNR limitations due to jitter can be determined by the following equation:

$$SNR = -20\log\left(2\pi f_{analog} t_{jitter_{rms}}\right) dB \quad (1)$$

where:

f is the analog input frequency.

t is the jitter.

Given a frequency of operation and an SNR requirement, the clock jitter requirement can be determined as follows.

$$t_{jitter} = \frac{10^{\frac{-SNR}{20}}}{2\pi f_{analog}} \quad (2)$$

If jitter was the only limitation to converter performance, sampling an IF signal of 70 MHz while maintaining an SNR of 75 dB will require a clock jitter of 400 femtoseconds.

Since data converters, especially ADCs, can easily be used to compute an SNR using FFT techniques, it is a simple lab experiment to determine the degradation in SNR as the analog input frequency increases while using a clock under test. This gives an indication of the jitter of the combined encode clock plus the contribution of the ADC itself. By subtracting the noise contribution of the ADC from the total noise, it is possible to estimate the noise due to jitter. Once the noise is known, the time jitter can be calculated. This procedure is outlined in Application Note AN-501 on the Analog Devices website.

This method does have two drawbacks. First, if windowing is used during the FFT processing, the spectral resolution becomes blurred by the impulse response of the window. Second, for most reasonable FFT sizes, the spectral resolution is quite limited. For example, if an encode rate of 61.44 MSPS is used and a 64K FFT is performed, each FFT bin represents a bandwidth of about 938 Hz. It is reasonable to expect that clock noise within several FFT bins will be lost to spectral blurring resulting in the loss of information several kHz on either side of the fundamental where much of the phase noise exists. Even in the case where synchronous FFTs are performed and windows are not used, the limitation of at least one FFT bin is still imposed, representing about 1 kHz. From a close-in phase noise point of view, much of the energy is usually contained in the first few kilohertz around the clock source. Therefore, by using the FFT method for estimation of jitter, much of the clock noise is lost in the method. However, since the goal is usually wideband SNR, this is generally an acceptable test in the measurement of the wideband performance of the ADC.

PHASE NOISE DEFINED

Types of Noise

A sampling signal can be represented by a modified sinusoidal function as shown in Equation 3. This equation shows an amplitude modulation, frequency modulation, and phase modulation term. While the sampling process can be considered a multiplication in time and convolution in the frequency domain, the sample source is often hard limited using differential comparison techniques. This minimizes amplitude effects on the sampling process, provided there is sufficient drive from the encode source to drive the sampling switches so AM to PM distortion is not a problem. Experimental data shows AM modulation, both at low and high modulation levels, are significantly less important than either the phase or frequency terms with similar modulation levels. Furthermore, the effects of phase and frequency noise yield similar degradations in the sampling process, the difference being only that phase modulation is identical to frequency modulation with the derivative of the modulating signal [4], in this case, Gaussian noise of which the derivative is also Gaussian distributed, resulting in nearly identical results [4].

$$f_{sample} = A_t \sin\left(\left(w_t t\right) + \phi_t\right) \quad (3)$$

The equation shows that amplitude, angular frequency, and phase are all time-dependent. This can be visualized in several ways. Strictly in the time domain, the signal appears as a Gaussian noise source. On the unit circle, the problems become more apparent. On the unit circle, the encode clock rotates around at a uniform angular rate. Each time it passes through zero phase, a new sample is taken with the ADC. Any noise on the clock will modulate where the tip of that vector lies and thus change where the zero crossing occurs. If the noise causes the leading edge to come earlier, the sample process will occur before it should. Likewise, if the noise happens to be on the trailing edge, then the encode will occur later in time. As can be seen, the noise vector can result from amplitude, phase, and frequency.

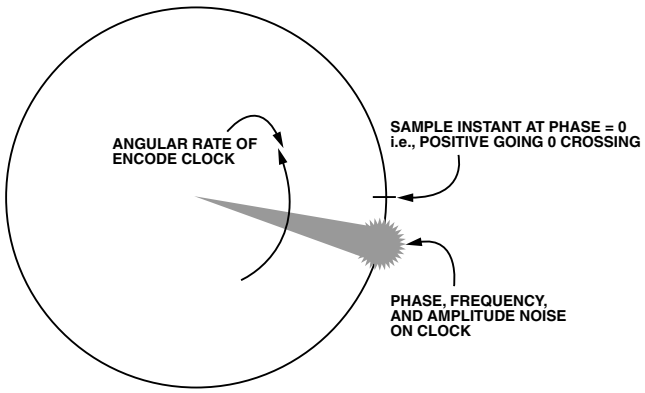


Figure 1. Sample Clock in the Polar Domain Showing What Clock Jitter May Look Like

Another traditional manner of observing clock jitter is by looking at it spectrally, as shown in Figure 2. In this diagram, much of the noise is clustered near the clock signal. However, because of jitter the ideal impulse in the frequency domain is actually spread out, as shown in the skirting. Much of the energy is distributed close to the desired frequency, although much is also contained in the wide bandwidth. Because phase noise can often

extend to very high frequencies, and since the ADC encode pin typically has a bandwidth much higher than the converter sample rate, this noise will impact the converter performance.

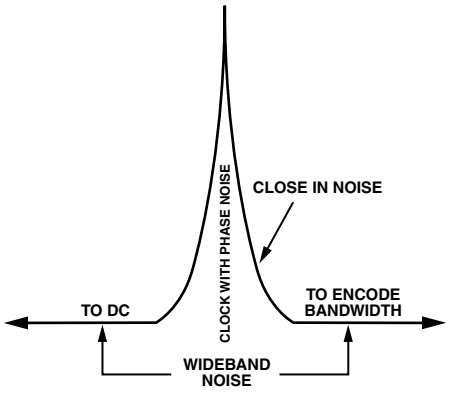


Figure 2. Sample Clock in the Frequency Domain Showing What Clock Jitter May Look Like

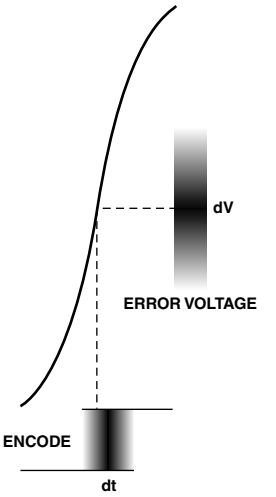


Figure 3. Sample Clock in the Time Domain Showing What Clock Jitter May Look Like

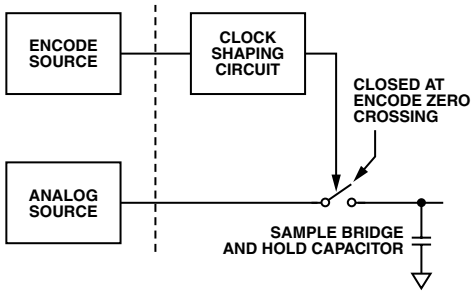


Figure 4. Typical Sampling Circuit of an ADC

Effects of Phase/Frequency Modulated Sample Time

As stated previously, the sampling process is a multiplication process in time and, therefore, a convolution process in the frequency domain. While it is clear that a mixer multiplies two analog signals in the time domain with the results being the convolution of these two in the frequency domain, it may be less clear that the sampling process is also a multiplication in time process.

Consider the sampling process. While it is clear that the analog input is continuous in time, the sampling clock, while its origin may be sinusoidal, is eventually used to drive a sample bridge with a unit pulse of constant amplitude and finite duration at the zero crossing of the encode signal. The results of this process are then the multiplication of the unit pulse with the analog input in the time domain and, therefore, convolution in the frequency domain.

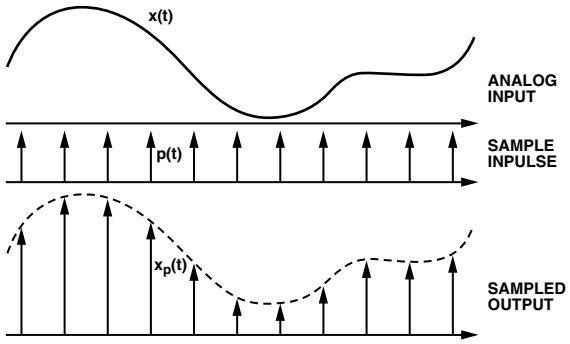


Figure 5. Analog Input, Sample Pulses and Resulting Sampled Output

In Figure 5, x(t) represents the continuous time analog input waveform, p(t) represents the ideal sampling function, and $x_p(t)$ represents the sampled output.

Using these terms, the output samples can be represented by the following:

$$x_p(t) = x(t)p(t) \tag{4}$$

Where:

$$p(t) = \sum_{n=-\infty}^{+\infty} \delta(t - nT) \tag{5}$$

In the frequency domain, this can be represented as

$$X_p(w) = \frac{1}{2\pi}\left[X(w) \times P(w)\right] \tag{6}$$

Since p(t) is a pulse train in time, it is also a pulse train in the frequency domain as represented by the following:

$$P(w) = \frac{2\pi}{T} \sum_{k=-\infty}^{+\infty} \delta(w - kw_s) \tag{7}$$

Substituting this into the previous equation gives

$$X_p(w) = \frac{1}{T} \sum_{k=-\infty}^{+\infty} X(w - kw_s) \tag{8}$$

Equation 8 indicates that the sampled analog input spectrum is repeated indefinitely for integer multiples of the sample rate w_s.

While the convolution between the clock and the analog input is true on the full spectrum as demonstrated above, it is also true on a microscopic scale as well. The same is true for the details of the spectrum centered

closely around the clock as they become convolved with the detailed spectrum centered closely on the analog signal. Specifically, any phase noise associated around the clock becomes convolved with the analog input to distort the spectral shape of the digitized analog signal. Because it is difficult to observe the phase noise around a clock, a sinusoidal phase modulation can be used to simulate the effects of a discrete frequency line of phase noise.

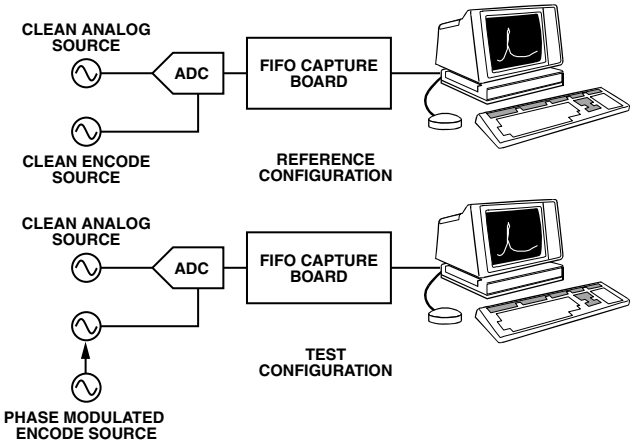


Figure 6. Various Configurations of Experimental Data Capture

Figure 7 shows the spectral nature of the encode source. For this example, the clock source is a 78 MSPS source with 100 kHz phase modulated with 0.001 radians of deviation applied. Given the relatively low level angle of modulation, only the first element of the sidebands is visible above the noise floor. The first sideband is about –66 dBc relative to the main carrier power of the encode. With an encode peak-to-peak voltage of 2 V, the rms value is 0.707 V rms. Based on this, each spurious tone is 0.3543 mV rms.

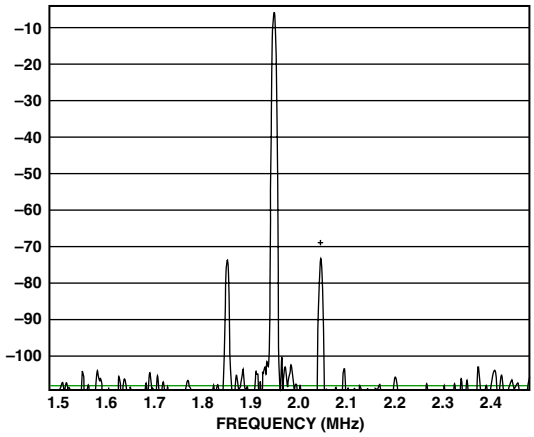


Figure 7. Spectrum of Phase-Modulated Encode Source

With the PM modulated signal applied to the clock port of the ADC, a pure CW tone was applied to the analog input port. The results, shown in Figure 8, indicate the replication of the sidebands of the clock on the analog signal as expected by convolving the PM modulated clock source with a pure CW tone. While this plot represents a single k term in Equation 8, it is replicated for other values of k.

The question is how to predict what level the phase noise will be. For sinusoidal inputs, the phase noise term out of the ADC can be predicted by

$$V_{phase\_noise\_ADCout} = v_{phase\_noise\_ADCin} \times \left[\frac{\frac{d(v_{signal})}{dt}}{\frac{d(v_{clk})}{dt}} \right] \quad (9)$$

This equation assumes that the phase noise voltage is the single sideband voltage and correlates to the voltage of one of the sidebands in Figure 7. Equation 9 can be simplified for most applications as follows:

$$V_{phase\_noise\_ADCout} = v_{phase\_noise\_ADCin} \times \frac{v_{signal} \times f_{signal}}{v_{clk} \times f_{clk}} \quad (10)$$

This simplified equation applies to a sampling system like that shown in Figure 4 and assumes that the encode signal is in a sinusoidal form. If the encode signal is in the form of a logic signal, the slew rate will not be dependent on the frequency of the encode signal and should be determined from the manufacturer's data sheet or direct measurement. Using either equation, it is simple to predict the output spurious level if the clock spurious voltage and frequency are known as well as the voltage and frequency of the analog input. Furthermore, the ratio of the signal voltage to clock voltage and the signal frequency and spurious frequency both directly impact the resultant spurious. Once the ratio of the signal voltage to the clock voltage has been established, it is a direct prediction as to the resulting spurious level for a given input spurious. For this example, the ratio between the clock voltage and the signal voltage is 1:1.

In the simplified form of the equation, $v_{phase\_noise\_ADCin}$ is the level of the phase-modulated single sideband signal, or a single frequency line of the phase noise modulated on the clocking signal. V_{clk} is the rms level of the clock, v_{signal} is the rms level of the main analog signal, f_{clk} is the frequency of the clock, and f_{signal} is the frequency of the main analog signal. Equation 10 may be reworked slightly as shown in Equation 11 to show the various relationships to other external dependent and independent variables, such as analog signal level and encode clock level.

$$\frac{V_{phase\_noise\_ADCout}}{v_{signal}} = \frac{v_{phase\_noise\_ADCin}}{v_{clk}} \times \frac{f_{signal}}{f_{clk}} \quad (11)$$

Because many clock designers work in terms of dBc, Equation 11 may now be transformed into log format and easily used to compute required or anticipated phase noise performance. In this equation, the first term ($Noise_{ADCout}$) is the resulting noise in dBc where the reference is the main output signal level (i.e., results in

dBc). The second term ($Noise_{CLKin}$) is noise on the clock in dBc relative to the main clock level and represents a noise or signal energy at a given offset. The third term is the log ratio of the analog input frequency to the sample rate.

$$Noise_{ADCout} = Noise_{CLKin} + 20\log\left(\frac{f_{signal}}{f_{clk}}\right) \quad (12)$$

In Equation 12, the clock (previous spectral plot) has a spectral line that is –66 dBc. This is the value to be used for $Noise_{CLKin}$. To determine the relative output, the relationship between the analog and encode frequencies must be known. In the following examples, the analog frequencies are set to 30.62 MHz and 108.62 MHz, respectively. Therefore the level of the spurs on the output spectrum may be computed using Equation 12.

$$-66\,\text{dBc} + 20\log\left(\frac{30.62\,\text{MHz}}{78\,\text{MHz}}\right) = Noise_{ADCout} = -74.1\,\text{dBc} \quad (13)$$

and

$$-66\,\text{dBc} + 20\log\left(\frac{108.62\,\text{MHz}}{78\,\text{MHz}}\right) = Noise_{ADCout} = -63.1\,\text{dBc} \quad (14)$$

As shown in Figure 8, the results are exactly as predicted by the previous equations. Therefore, this equation can be a useful tool in predicting how the converter will respond to a given analog and encode stimulus.

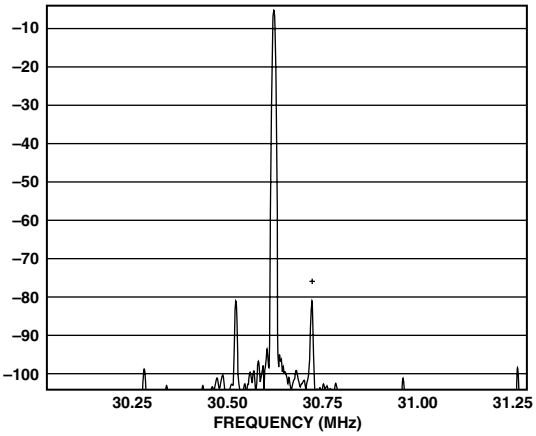


Figure 8. 30.62 MHz CW Tone Sampled by Phase-Modulated Encode Results in a Level of –74 dBc

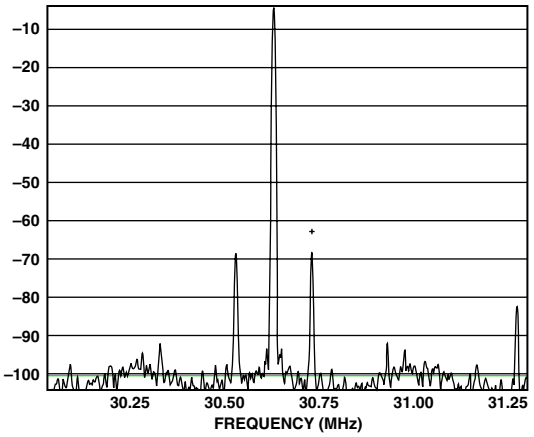


Figure 9. 108.62 MHz CW Tone Sampled by Phase-Modulated Encode Results in a Level of –63 dBc

In Figure 9, it is interesting to note the degradation between the two measurements. If either the SNR (dominated by the side tones) or the spurious alone are compared, the degradation as the frequency increases is as expected, due to jitter. It would be expected that as the input frequency increases for each doubling of the input frequency (doubling of the analog input slew rate), the energy due to jitter is expected to increase by 6 dB. In the example here, the change from 30.62 MHz to 108.62 MHz, is a ratio of 3.55 which ideally represents an increase in noise of $6 \times \log_2$ (108.62/30.62) or 10.9 dB. Between these two measurements, the spur level changed from –74 dBc to –63 dBc or 11 dB, exactly what was expected.

Thus, it is clear that not only is the wideband noise of the clock important as documented in previous applications notes, but the close in noise is important as well and it follows the same behavior as the wideband noise. However, the overall impact is somewhat different. Whereas the noise outside of the channel bandwidth increases the overall noise more or less uniformly, the close in noise causes reciprocal mixing and affects only nearby signals.

From this example, two regions around the clock can be defined. The first starts at the center frequency of the clock and ends at one-half the desired channel bandwidth in both directions. (In some cases, this may be the entire Nyquist band; in others, it may be somewhat less than the Nyquist band. This depends on the end application.) The second region starts one-half of the desired channel bandwidth away from the clock and ends at the bandwidth of the encode logic (including both internal and external limited—often limited by devices like transformers) for the data converter in one direction and dc in the other. In most cases, the bandwidth of the encode circuitry extends to several hundred MHz and even into the GHz range on high dynamic range converters. The spectrum that is passed by the encode circuitry is the spectrum that is convolved with the desired analog input during the sampling process.

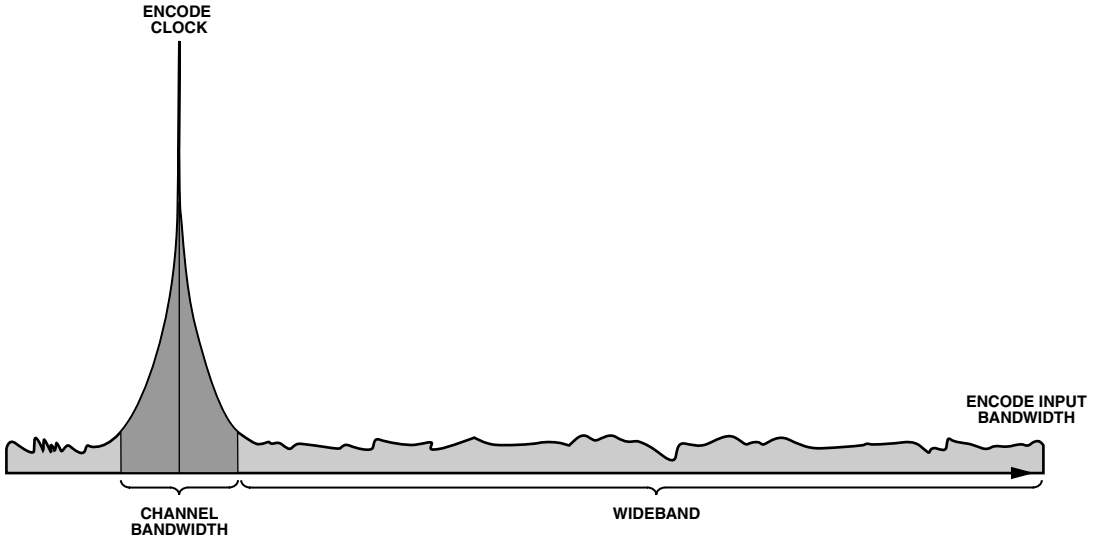


Figure 10. Typical Spectrum of encode clock, represents dc to bandwidth of encode input of ADC, typically >750 MHz. Not shown to scale.

It should be clearly understood that the encode signal is convolved with the desired analog input causing the spectral shape of the clock to be expressed on the analog signal itself, as shown in Figure 10. However, because the ADC is a sampled system, the wideband noise of the sample clock is also aliased within the band of interest. This causes all of the wideband noise that enters the encode port to be aliased within the Nyquist band. This can result in a significant accumulation of the noise and a significant reduction in SNR.

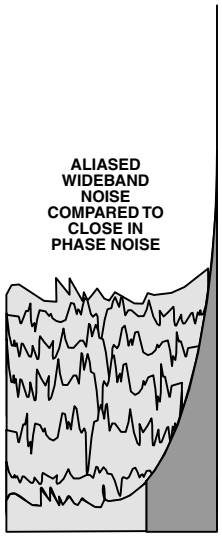


Figure 11. Typical Spectrum of Encode Clock after Sampling. The Encode Bandwidth (750 MHz) is Aliased into the Nyquist Band.

As shown in Figure 11, all of the wideband noise is aliased within the Nyquist spectrum causing an accumulation of that energy, potentially increasing beyond the power contained within the close in phase noise. In fact, if the encode bandwidth is 750 MHz, the noise from this bandwidth will alias over 24 times with a 61.44 MSPS clock. The effect is that the noise spectral density caused by wideband jitter (remember at low analog frequencies, NSD is determined by quantization and thermal noise as well) is increased by almost 14 dB. In contrast, by definition, the close in noise (defined to be the bandwidth of the signal of interest) cannot alias and therefore only contributes once. The implications for implementation are that although a fast slewing edge is important for accurate clock edge placement; limiting the amount of wideband noise on the clock can be of equal importance to maximizing converter performance, thus making the balance between the two often tricky.

For IF sampling systems where jitter is an issue, the limitation to SNR based only on jitter can be determined by the equation

$$SNR_{FS} = -20\log\left(2\pi f_{analog} t_{jitter_{rms}}\right) \quad (15)$$

where:

f is the analog input frequency.

t is the jitter.

Solving this equation for t will put this equation in a form that given an SNR requirement, the clock jitter requirement can be determined.

$$\frac{10^{\frac{-SNR_{FS}}{20}}}{2\pi f_{analog}} = t_{jitter_{rms}} \quad (16)$$

However, for many applications, the jitter alone is not sufficient to specify performance of the clock source. It is often desired to represent the clock phase noise using spectral density at given offsets from the center frequency as is traditionally done for PLL and VCO circuits.

There are two types of phase noise to consider. The most commonly referred to close in noise is 1/f noise. This is the noise that is closest in to the central frequency of the clock and experiences rapid decay as the offset frequency is increased. As already determined, the convolutional process of ADC sampling will simply mirror this effect on the output and, therefore, the 1/f clock noise is primarily important in terms of phase error on the signal of interest and the effects of reciprocal mixing of adjacent and alternate channels back into the desired channel. Once the 1/f noise has reached the noise floor, as previously shown, the focus then changes to the wideband thermal noise that ends up falling in band. If the 1/f noise satisfactorily meets the requirements of reciprocal mixing, then the focus can be on the wideband thermal noise.

For this section it is assumed that the noise limitations of the sampling process are completely in the wideband noise of the clock (as opposed to 1/f noise to be discussed separately), then it is possible to determine what the wideband limitations to the clock source are and to equate that to the traditional clock jitter equations.

To determine the wideband spectral density of the encode clock, the required output spectral density must first be determined.

$$ADC_{spectral\ density} = -SNR_{FS} - 10\log_{10}\left(\frac{samplerate}{2}\right) \quad (17)$$

If the traditional equation for jitter is substituted into the equation for SNR, this gives a direct method for determining spectral noise density with reference to jitter.

$$ADC_{spectral\ density} =$$

$$20\log_{10}\left(2\pi f_{analog} t_{jitter_{rms}}\right) - 10\log_{10}\left(\frac{samplerate}{2}\right) \quad (18)$$

Since this is wideband, it is valid for offset frequencies from the point where the 1/f noise intersects the noise floor to the Nyquist rate (or dc on the lower side). Since high performance converters have encode bandwidths of between 500 MHz and 1000 MHz, noise on the encode input will be aliased back into the Nyquist band many times. Therefore, to determine the actual clock spectral density, an estimate must be made on the unaliased spectral density of the noise. Since the noise is assumed to be Gaussian and noncoherent, a close approximation may be made by remembering that each time the spectrum is doubled, the noise will double (or half if undoubled).

An estimate can therefore be made by the following equation:

$$\begin{aligned} Clock_{spectral\ density} &= 20\log_{10}\left(2\pi f_{analog} t_{jitter_{rms}}\right) \\ &-10\log_{10}\left(\frac{samplerate}{2}\right) \\ &-3\log_2\left(\frac{\frac{clock\ bandwidth}{samplerate}}{2}\right) - 20\log\left(\frac{f_{analog}}{f_{samplerate}}\right) \end{aligned} \quad (19)$$

Using this equation, it is possible to determine the required wideband spectral density of the clock. It should be noted that the results are valid based on a narrow band single tone input to the ADC. The relationship to other waveforms is outside the scope of this discussion; however, the narrow band sine wave is almost always the worst-case condition for a band limited analog input and quite useful in the analysis. On the other hand, spread spectrum signals like CDMA2000 and WCDMA are much less strenuous and usually lead to much better performance than expected for narrow band sources.

As shown, Equation 19 is useful for determining what the required spectral density is for a required jitter. Therefore, given an IF frequency and a jitter specification, it is easy to approximate clock spectral density. For example, if the IF frequency is 108.62 MHz, the jitter is 0.2 ps, the sample rate is 61.44 MSPS, and the clock bandwidth is 350 MHz (limited by transformer coupling), then the clock noise spectral density is

$$\begin{aligned} Clock_{spectral\ density} &= 20\log_{10}\left(2\pi \times 108.62\,MHz \times 200\ f_S\right) \\ &-10\log_{10}\left(\frac{61.44\,MHz}{2 \times 1\,Hz}\right) \\ &-3\log_2\left(\frac{350\,MHz}{61.44\,MHz/2}\right) \\ &-20\log\left(\frac{108.62\,MHz}{61.44\,MHz}\right) \end{aligned} \quad (20)$$

This evaluates to a NSD of –167.7 dBc/Hz. It is difficult to judge how much noise jitter contributes over and above thermal and quantization noise. In reality, most of the time jitter is the dominant contributor at high frequencies. In that case, the NSD will be higher. A quick check of a typical data sheet shows that at these analog frequencies, the SNR dominated by jitter would approach 73 dBFS. Therefore, the expected NSD of such a clock would approach –168 dBc/Hz average over about a 350 MHz span indicating that it probably is higher closer to the clock frequency and lower at the extreme.

The alternate to this equation is to solve it for clock jitter. Therefore, given the required clock noise spectral density and all other terms, the required clock jitter can be estimated. This equation takes the form of

$$t_{jitter_{rms}} = \frac{10^{\left(\frac{Clock_{spectral\ density}+10\log_{10}\left(\frac{samplerate}{2}\right)+3\log\left(\frac{clock\ bandwidth}{samplerate/2}\right)+20\log\left(\frac{f_{analog}}{f_{samplerate}}\right)}{20}\right)}}{20\pi f_{analog}} \quad (21)$$

Phase Noise and Jitter

Because there is a direct relationship between phase noise and jitter, it is possible to relate one to the other. When dealing with data converters, the wideband noise is generally considered to be most important. The following figure shows the wideband noise characteristics of a typical crystal clock oscillator. Note that the close in noise ($1/f^n$) has been omitted from this calculation. While these numbers are important in the overall system, they are less important for the noise performance of the ADC (albeit very important for EVM and reciprocal mixing).

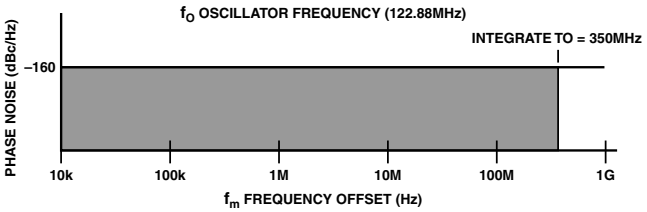


Figure 12.

To determine the jitter, the first step is to determine total noise power by integrating the noise over the bandwidth, in this case from 10 kHz frequency offset to 350 MHz. Since 10 kHz is small compared to the 350 MHz, the lower limit barely affects the calculation for the case of wideband white noise. Integration in the log domain is simple addition. Therefore, the total noise power is

$$noise_{integrated} = -160\ dBc/Hz + 10\log\left[350\times10^6 - 10\times10^3\right] = -74.56\ dBc \quad (22)$$

The goal is to determine the angle of modulation. This must be done based on the observed power of the phase noise. Because the modulation phasor is 90 degrees relative to the main carrier, this forms a small angle which can be inferred by determining the noise voltage relative to the main signal voltage. Since the modulation angle is assumed to be small, the angle is approximately equal to the slope which is determined by the two measurable quantities, carrier voltage and noise voltage. Because our measurements are power, these must be converted to volts. This can be accomplished by multiplying the power by the impedance and taking the square root. Because we actually need a ratio of two powers across the same load, the impedance falls from the equation. Likewise, since the power is in dBc, and the main signal is our reference, it can easily be shown that the remaining term is only that of the measured phase noise which must be converted from dBc to power. Taking the square root will provide the angle as shown in the following example. Because phase noise usually occurs on both sides of the clock, the single sideband numbers typically used must be doubled to account for the noise in the opposite sideband. This is shown in the following equation as a factor of 2 under the square root, assuming that the sidebands do not correlate for wideband noise.

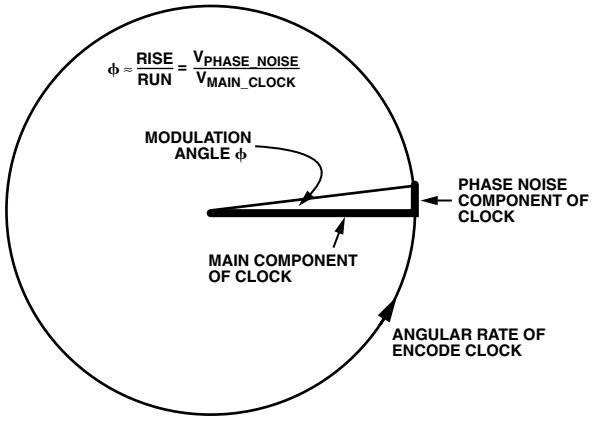


Figure 13.

$$phase\_jitter_{rms} = \sqrt{2\times10^{noise_{integrated}/10}} = \sqrt{2\times10^{-74.56/10}} = 2.655\times10^{-4}\ radians \quad (23)$$

Since this is a rotating vector, the phase jitter in radians must be divided by angular frequency, $2\pi f_{clk}$, to determine the time required to slew through the phase angle. This results in jitter rms.

$$time\_jitter_{rms} = \frac{phase\_jitter_{rms}}{2\pi f_{clk}} = \frac{2.655\times10^{-4}}{2\pi122.88\times10^6} = 0.343\ ps \quad (24)$$

With this basic understanding, more complex examples can be considered. In this case, the different regions of the curve may be integrated separately and then added together to provide the total jitter results.

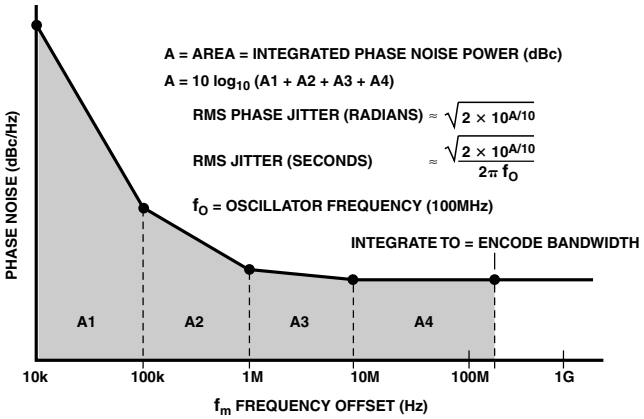


Figure 14.

In this example, four points (and three areas) along the curve are defined. In determining the area of any one region, the "average" noise density may be calculated using the trapezoidal rule for area; specifically, that the average noise power is halfway between the two corners. Better accuracy in the 1/f region can be achieved using Leeson's equation to predict the area under the curve, but for first order this method is accurate enough. For example, in the region between 100 Hz and 1000 Hz, the corners are at –120 dBc/Hz and –150 dBc/Hz; the midpoint is –135 dBc/Hz. Using this as the height term and the base as 900 Hz, the noise in this region is

$$\text{noise}_{\text{integrated}} = \left(\frac{-120-150}{2}\right)\text{dBc/Hz} + 10\log[1000-100] = -105.46\ \text{dBc} \quad (25)$$

Using the earlier equations for converting to phase jitter and then to time jitter give a result of about 10 femtoseconds of jitter in the first region. The other regions may be determined in the same manner. The results are 193 femtoseconds.

While wideband jitter can be determined in terms of wideband SNR and noise spectral density as shown, close in noise is different. Close in phase noise (i.e., $1/f^n$) is best determined in terms of reciprocal mixing. Reciprocal mixing occurs when a stronger signal is near the desired weaker signal. If the clock (or local oscillator) phase noise is mixed with the undesired signal, it will serve to increase the noise floor of the desired signal. If the phase noise is large enough, it can overpower the desired weak signal, and cause loss of that signal, as shown in Figure 16a and Figure 16b.

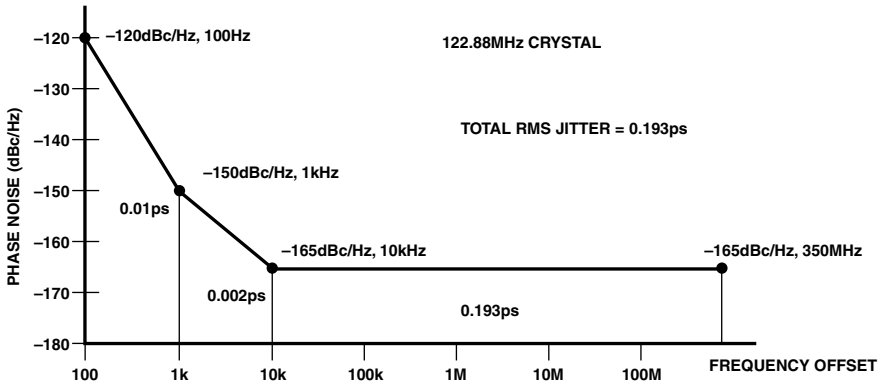
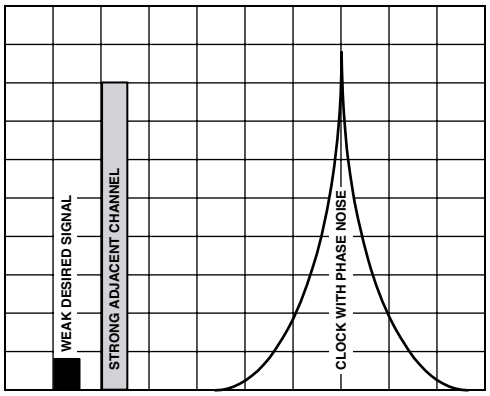
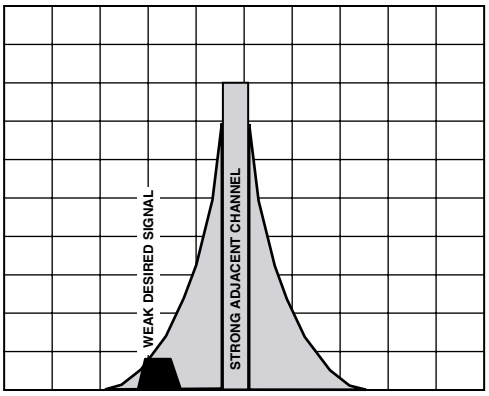


Figure 15.



RELATIVE SPECTRUM OF ANALOG AND SAMPLING SIGNALS

Figure 16a.



RELATIVE EFFECTS OF SAMPLE CLOCK ON ANALOG SIGNAL.
RECIPROCAL IS ALSO TRUE

Figure 16b.

In Figure 16a, the relative spectral densities of the signals involved are shown. Note the skirted shape of the clock signal. When this clock is used to sample the analog input, this skirt is convolved onto all of the analog signals being converted. The result is that all of the signals take on this general shape. As shown, the strong nearby signal now overpowers the weak desired signal, making it impossible to further process the signal.

Because all requirements are different, general requirements for close in phase noise are not possible to determine. However, once standards about the spacing and level of typical signals have been determined, it is possible to then set phase noise requirements.

For example, based on the GSM requirements in 05.05, the following specifications can be estimated. These are based on the specified minimum sensitivity and include meeting an overall noise figure of 4 dB and requiring that the antenna-referenced phase noise of the clock source be 6 dB below the effective noise spectral density. It should be noted that many times the reference sensitivity of a typical receiver is much better than the required minimum. Additionally, any selectivity prior to being sampled (or mixed) will ease the requirement in most cases dB for dB.

Phase Noise from Adjacent Channels

Similarly the requirements for CDMA2000 may be determined. Because CDMA2000 is such a wide band, it is assumed that the spectral density of the phase noise meets the conditions at the nearest corner and proceeds to improve across the bandwidth of the channel. These assumptions were chosen in order that no portion of the channel would be disrupted or otherwise impede the benefits of a distributed communications channel. Therefore, it is assumed that the noise due to phase noise is equal to the kT/Hz noise at the nearest corner (–174 dBm/Hz).

Table I. Phase Noise from Adjacent Channels

GSM per 05.05 in Wideband Application	Offset	Performance*
Adjacent 1 +9 dBc	100 kHz to 300 kHz	~ –101 dBc/Hz
Adjacent 2 +41 dBc	300 kHz to 500 kHz	~ –133 dBc/Hz
600 kHz blocker –26 dBm	500 kHz to 700 kHz	~ –151 dBc/Hz
800 kHz blocker –16 dBm	700 kHz to 2.9 MHz	~ –161 dBc/Hz
3 MHz blocker –13 dBm	2.9 MHz to band edge	~ –164 dBc/Hz

*This number assumes that the noise due to phase noise is equal to 6 dB below the thermal noise of the overall receiver. Typical noise figures are 4 dB; therefore, total thermal noise is –170 dBm/Hz referenced to the antenna, and equivalent phase noise would be 6 dB below this, or –176 dBm/Hz.

Table II.

CDMA2000 per spec	Offset	Performance*
+50 dBc at 750 kHz	125 kHz	~ –107 dBc/Hz
+87 dBc at 900 kHz offset	275 kHz	~ –144 dBc/Hz

*Allows the noise due to phase noise to equal kT noise for the stated reference sensitivities.

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