Hierarchical Krylov Subspace Reduced Order Modeling of Large RLC Circuits

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Outline

- Introduction and Motivation
- Review of subspace projection based MOR
- Hierarchical projection MOR: hiePrimor
  - Partitioned MNA and reduction
  - Moment matching connection
  - Analysis of passivity preservation
  - Circuit partitioning
- Summary

Introduction and Motivation

- Massive circuits are reduced by approximate compact models before simulations.
- Explicit moment matching and Krylov subspace
- Hierarchical and parallel techniques
- Passivity preservation

Review of subspace projection based MOR

- Circuit formulation

$$C\dot{\mathbf{x}}_n = -G\mathbf{x}_n + B\mathbf{u}_m$$
$$\mathbf{i}_m = L^T\mathbf{x}_n$$

  - n is number of state variables ,
  - m is the number of ports,
  - x_n is the vector of state variables ,
  - C is storage element matrix,
  - G is conductance matrix,
  - B is position matrix for input ports,
  - L is position matrix for output ports.

Krylov subspace

- Block moments

$$H(s) = M_0 + M_1 s + M_2 s^2 + \ldots$$

$$A = -G^{-1}C \qquad R = G^{-1}B$$

$$M_i = L^T A^i R$$

- Block Krylov subspace

$$\begin{aligned} Kr(A,R,q) &= colsp[R, AR, A^2R, \ldots, A^{k-1}R, \\ &\quad A^k r_0, A^k r_1, \ldots, A^k r_l] \\ &\quad k = \lfloor q/m \rfloor, \qquad l = q - km. \end{aligned}$$

Krylov subspace projection based MOR

- Reduction of original system

$$colsp(X) = Kr(A, R, q)$$

$$\tilde{C} = X^T C X \qquad \tilde{G} = X^T G X$$

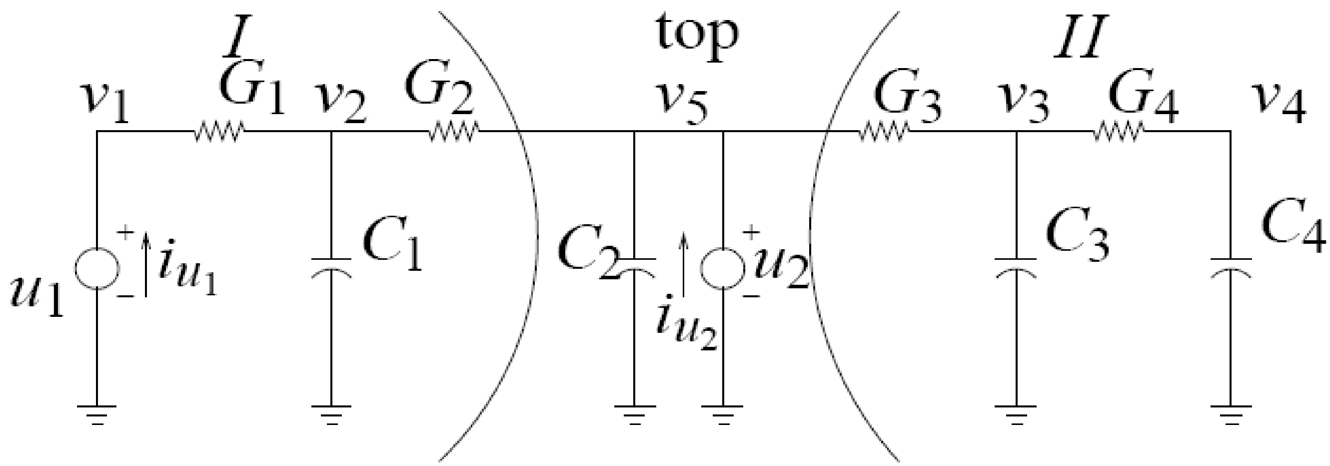
$$\tilde{B} = X^T B \qquad \tilde{L} = X^T L$$

$$\tilde{C}\dot{\tilde{\mathbf{x}}}_n = -\tilde{G}\tilde{\mathbf{x}}_n + \tilde{B}\mathbf{u}_m$$
$$\mathbf{i}_m = \tilde{L}^T \tilde{\mathbf{x}}_n$$

- Passivity preserved through congruent transformation

Hierarchical projection MOR: hiePrimor

- An illustrative example



Two subcircuits (I, II) are connected through the top circuit only.

Subcircuit I

- Sub MNA

$$\begin{bmatrix} G_1 & -G_1 & -1 \\ -G_1 & G_1+G_2 & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_{u_1} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \dot{v}_1 \\ \dot{v}_2 \\ \dot{i}_{u_1} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} u_1 \\ i_2 \end{bmatrix}$$

- Modified B matrix (add one current source)

$$B_1' = \begin{bmatrix} 0 & 0 \\ 0 & 1 \\ 1 & 0 \end{bmatrix}$$

Partitioned MNA

$$
\left[\begin{array}{ccc|cc|cc}
G_1 & -G_1 & -1 & 0 & 0 & 0 & 0 \\
-G_1 & G_1+G_2 & 0 & 0 & 0 & -G_2 & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & 0 \\
\hline
0 & 0 & 0 & (G_3+G_4) & -G_4 & -G_3 & 0 \\
0 & 0 & 0 & -G_4 & G_4 & 0 & 0 \\
\hline
0 & -G_2 & 0 & -G_3 & 0 & (G_2+G_3) & -1 \\
0 & 0 & 0 & 0 & 0 & 1 & 0
\end{array}\right]
\left[\begin{array}{c}
v_1 \\ v_2 \\ i_{u_1} \\ \hline v_3 \\ v_4 \\ \hline v_5 \\ i_{u_2}
\end{array}\right] +
$$

$$
\left[\begin{array}{ccc|cc|cc}
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & C_1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\hline
0 & 0 & 0 & C_3 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & C_4 & 0 & 0 \\
\hline
0 & 0 & 0 & 0 & 0 & C_2 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0
\end{array}\right]
\left[\begin{array}{c}
\dot{v}_1 \\ \dot{v}_2 \\ \dot{i}_{u1} \\ \hline \dot{v}_3 \\ \dot{v}_4 \\ \hline \dot{v}_5 \\ \dot{i}_{u2}
\end{array}\right] =
\left[\begin{array}{c|c}
0 & 0 \\
0 & 0 \\
1 & 0 \\
\hline
0 & 0 \\
0 & 0 \\
\hline
0 & 0 \\
0 & 1
\end{array}\right]
\left[\begin{array}{c}
u_1 \\ \hline u_2
\end{array}\right]
$$

$$
\left[\begin{array}{c}
i_{u_1} \\ \hline i_{u_2}
\end{array}\right] =
\left[\begin{array}{ccc|cc|cc}
0 & 0 & 1 & 0 & 0 & 0 & 0 \\
\hline
0 & 0 & 0 & 0 & 0 & 0 & 1
\end{array}\right] x_n
$$

$$
x_n^T = \left[v_1 \; v_2 \; i_{u_1} \; v_3 \; v_4 \; v_5 \; i_{u_2}\right]
$$

In general case

- An n-way partitioned RLC circuit

$$\begin{bmatrix} G_1 & 0 & \dots & G_{1t}^T \\ 0 & G_2 & \dots & G_{2t}^T \\ \vdots & \vdots & \dots & \vdots \\ G_{1t} & G_{2t} & \dots & G_{tt} \end{bmatrix} \begin{bmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \\ \vdots \\ \mathbf{x}_t \end{bmatrix} + \begin{bmatrix} C_1 & 0 & \dots & 0 \\ 0 & C_2 & \dots & 0 \\ \vdots & \vdots & \dots & \vdots \\ 0 & 0 & \dots & C_{tt} \end{bmatrix} \begin{bmatrix} \dot{\mathbf{x}}_1 \\ \dot{\mathbf{x}}_2 \\ \vdots \\ \dot{\mathbf{x}}_t \end{bmatrix}$$

$$= \begin{bmatrix} B_1 & 0 & \dots & 0 \\ 0 & B_2 & \dots & 0 \\ \vdots & \vdots & \dots & \vdots \\ 0 & 0 & \dots & B_{tt} \end{bmatrix} \begin{bmatrix} \mathbf{u}_1 \\ \mathbf{u}_2 \\ \vdots \\ \mathbf{u}_t \end{bmatrix}$$

- Sub-level reduction

$$\begin{bmatrix} \tilde{G}_1 & 0 & \ldots & \tilde{G}_{1t}^T \\ 0 & \tilde{G}_2 & \ldots & \tilde{G}_{2t}^T \\ \vdots & \vdots & \ldots & \vdots \\ \tilde{G}_{1t} & \tilde{G}_{2t} & \ldots & G_{tt} \end{bmatrix} \begin{bmatrix} \mathbf{z}_1 \\ \mathbf{z}_2 \\ \vdots \\ \mathbf{x}_t \end{bmatrix} + \begin{bmatrix} \tilde{C}_1 & 0 & \ldots & 0 \\ 0 & \tilde{C}_2 & \ldots & 0 \\ \vdots & \vdots & \ldots & \vdots \\ 0 & 0 & \ldots & C_{tt} \end{bmatrix} \begin{bmatrix} \dot{\mathbf{z}}_1 \\ \dot{\mathbf{z}}_2 \\ \vdots \\ \dot{\mathbf{x}}_t \end{bmatrix}$$

$$= \begin{bmatrix} \tilde{B}_1 & 0 & \ldots & 0 \\ 0 & \tilde{B}_2 & \ldots & 0 \\ \vdots & \vdots & \ldots & \vdots \\ 0 & 0 & \ldots & B_{tt} \end{bmatrix} \begin{bmatrix} \mathbf{u}_1 \\ \mathbf{u}_2 \\ \vdots \\ \mathbf{u}_t \end{bmatrix}$$

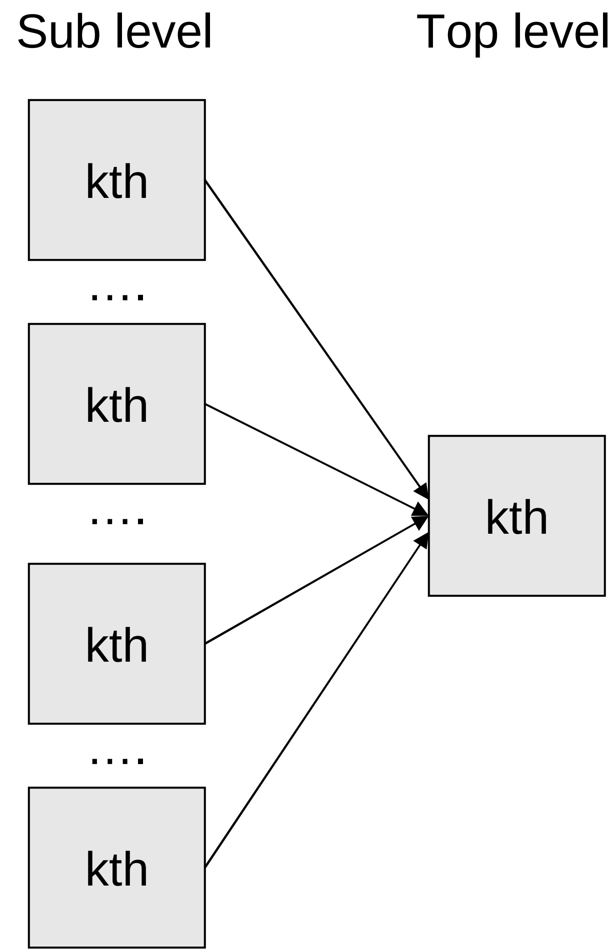
$$G_r \tilde{\mathbf{x}}_r + C_r \dot{\tilde{\mathbf{x}}}_r = B_r \mathbf{u}_r$$

- Top-level reduction

$$\tilde{G}\tilde{\mathbf{x}} + \tilde{C}\dot{\tilde{\mathbf{x}}} = \tilde{B}\mathbf{u}$$

Moment matching connection

- Final reduced model preserves the first k block moment.
- hiePrimor will have the same accuracy as the flat projection based method, if using the same reduced order.



Passivity preservation

- Transfer function: positive real, iff

$$
\begin{aligned}
&(1) \quad H(s) \text{ is analytic, for } Re(s) > 0 \\
&(2) \quad H^*(s) = H(s^*) \text{ , for } Re(s) > 0 \\
&(3) \quad H(s) + H(s^*)^T \geq 0 \text{ , for } Re(s) > 0
\end{aligned}
$$

- (1) and (2) are always satisfied for RLC circuits (no unstable poles and real response).
- Proof of (3) in detail can be found in our paper.

Circuit partitioning

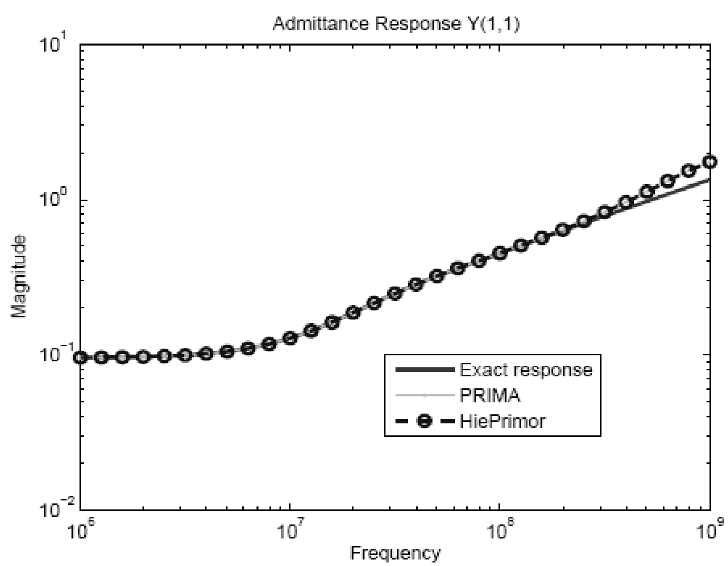
- Use hMETIS partition tool suite.
- Minimize the capacitive cut to make sure a DC path if there are current sources.
- Reduce terminal counts of subcircuits as much as possible.
- Very suitable for very large RLC networks like bus, coupled transmission lines and clock nets with loosely coupled circuits.
- Also be applied to densely coupled circuits

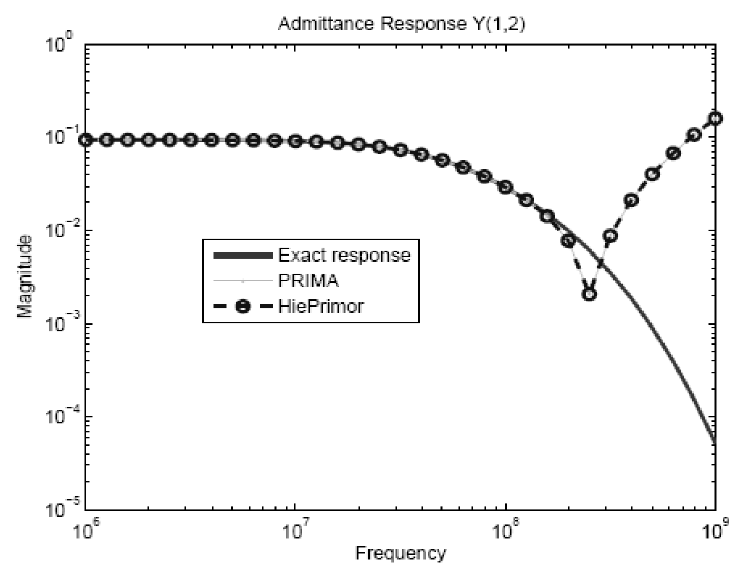
Experimental Environment

- Use Matlab 7.0 for matrix/vector operations.
- Use Python as parser for I/O operations.
- Intel Xeon 3.0GHz dual CPU workstation with 2GB memory.
- Sparse matrix structure in Matlab.
- Test circuits are in SPICE format.
- Benchmarks: capacitively-coupled bus lines with different length.

Results (1)

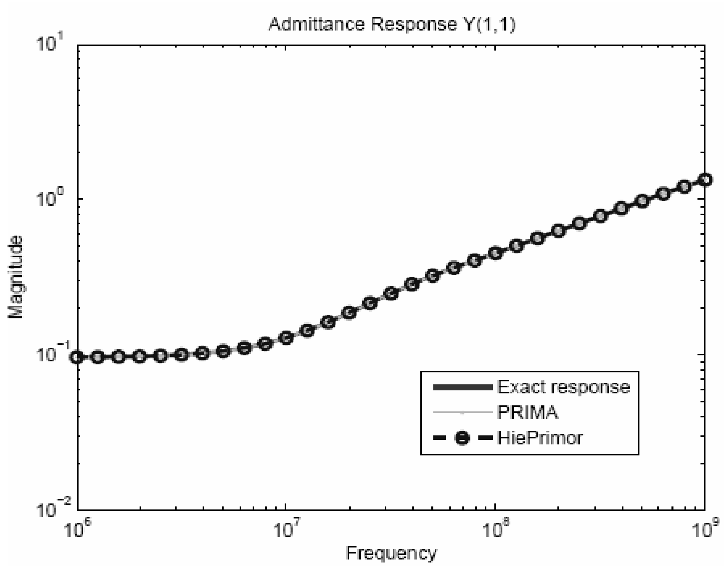
- Accuracy comparison of PRIMA and hiePrimor in Ckt1 when k = 4, q = n × k.

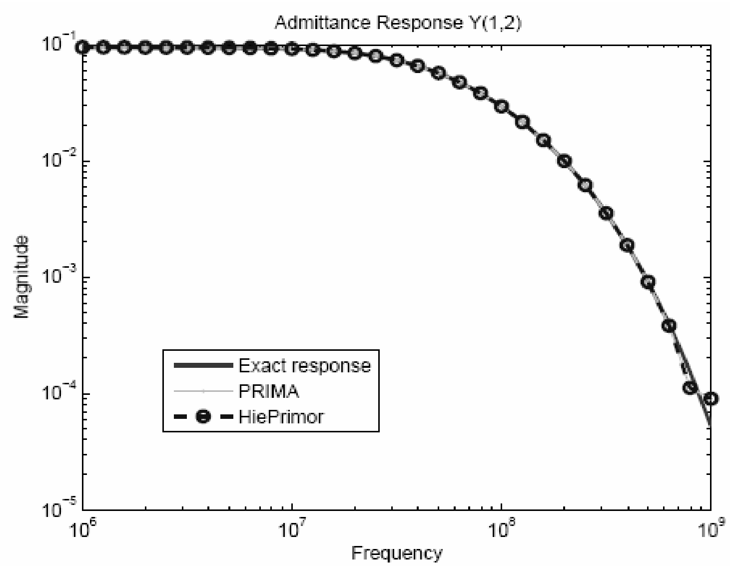




Results (2)

- Accuracy comparison of PRIMA and hiePrimor in Ckt1 when k = 8, q = n × k.





Results (3)

- Reduction time comparison of PRIMA and hiePrimor for all test circuits.
- hiePrimor up to 5x faster.

Test Ckts	#Nodes	#Sub	#Ports	PRIMA (s)	hiePrimor (s)	Speedup
Ckt1	$25k$	2	8	5	4	1.25
Ckt2	$50k$	4	16	16	9	1.78
Ckt3	$100k$	8	16	32	13	2.46
Ckt4	$200k$	8	16	69	27	2.56
Ckt5	$500k$	16	24	248	60	4.13
Ckt6	$800k$	16	24	401	99	4.05
Ckt7	$1M$	16	32	863	154	5.60
Ckt8	$1.5M$	16	20	–	176	–

Results (4)

- For different numbers of partitions

Test Ckts	#Parts = 2	#Parts = 4	#Parts = 8	#Parts = 16
Ckt5	116	100	71	60
Ckt6	374	251	128	99
Ckt7	383	298	204	154
Ckt8	675	394	257	176

- For different numbers of ports (Ckt7)

#Ports	PRIMA	hiePrimor	Speedup
8	189	56	3.38
16	339	96	3.53
32	863	154	5.60

Results (5)

- Comparison in artificial parallel computing setting.

Test Ckts	Max Sub (s)	Top (s)	Sum (s)	Speedup
Ckt1	2	0	2	2.50
Ckt2	3	1	4	4.00
Ckt3	3	1	4	8.00
Ckt4	5	1	6	11.50
Ckt5	6	1	7	35.43
Ckt6	10	1	11	36.46
Ckt7	17	3	20	43.15
Ckt8	14	1	15	–

Conclusion

- Hierarchical projection based MOR: hiePrimor.
- Divide-and-conquer strategy to reduce the reduction complexity and speed up the reduction process.
- Same accuracy as flat MOR given the same reduced order.
- Preserving passivity.
- Parallel computing techniques.

Thank you!