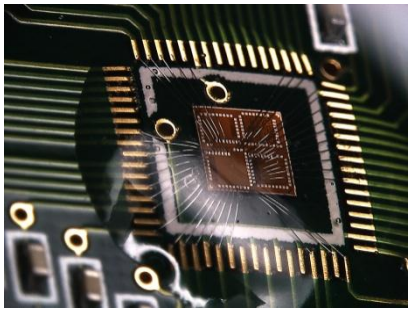


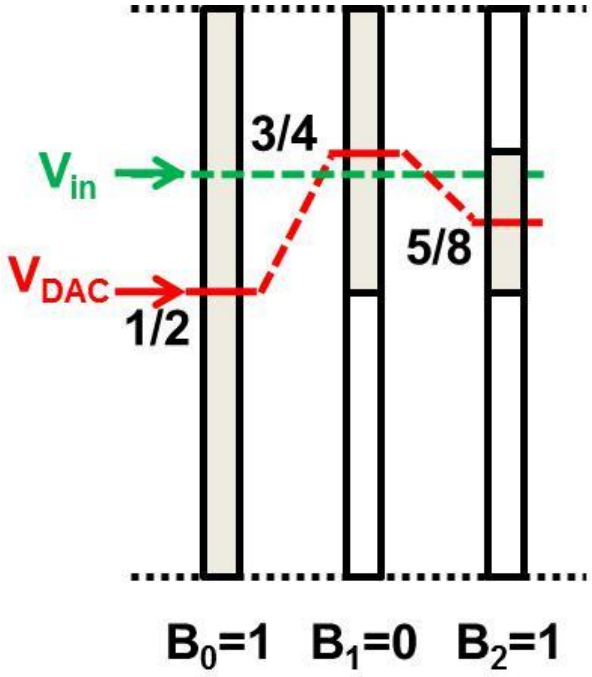
A 0.35-0.8V 8b 0.5-35MS/s 2bit/step Extremely-Low Power SAR ADC

Kentaro Yoshioka, Akira Shikata,
Ryota Sekimoto, Tadahiro Kuroda and Hiroki Ishikuro

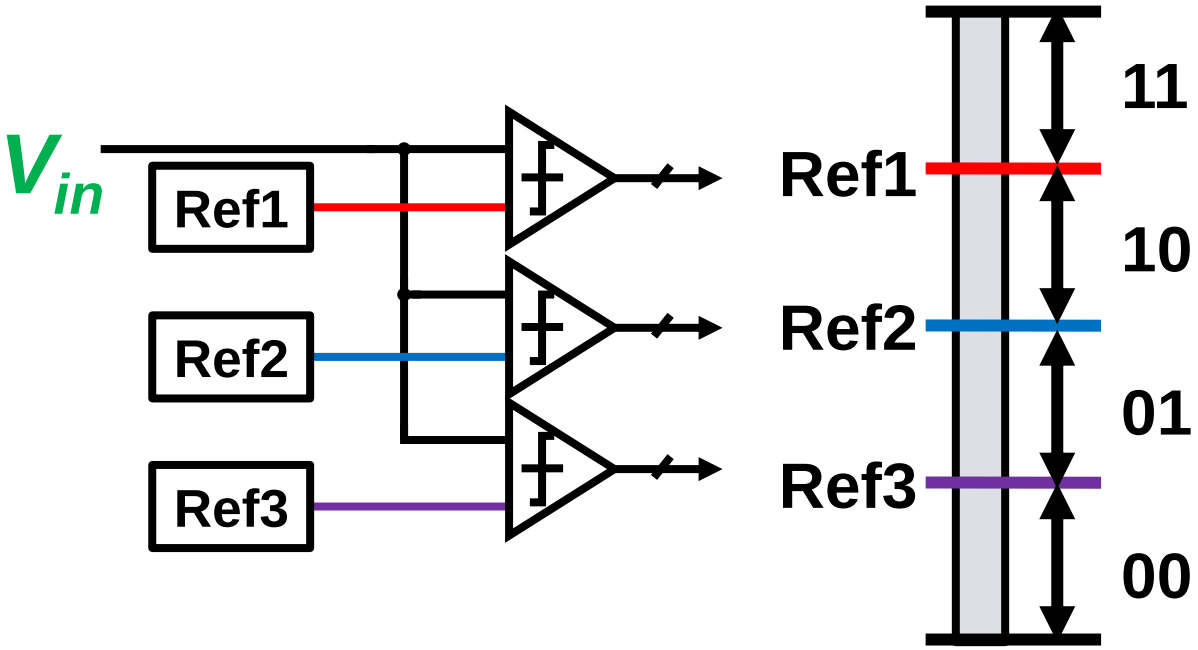
Keio University

1bit/step & 2bit/step SAR ADC

1bit/step(Conv. SAR)



2bit/step(High speed SAR)

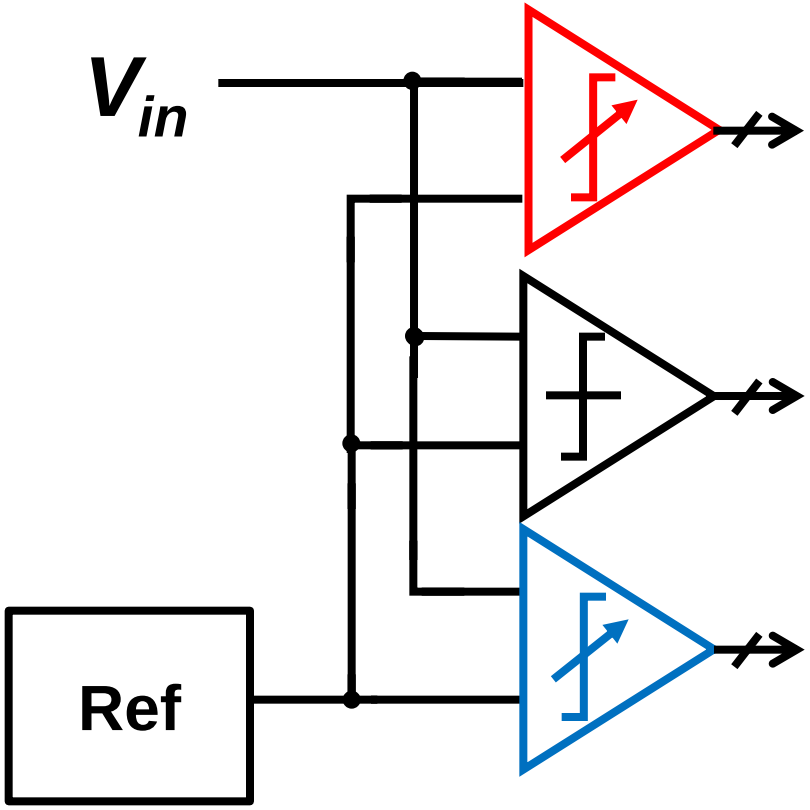


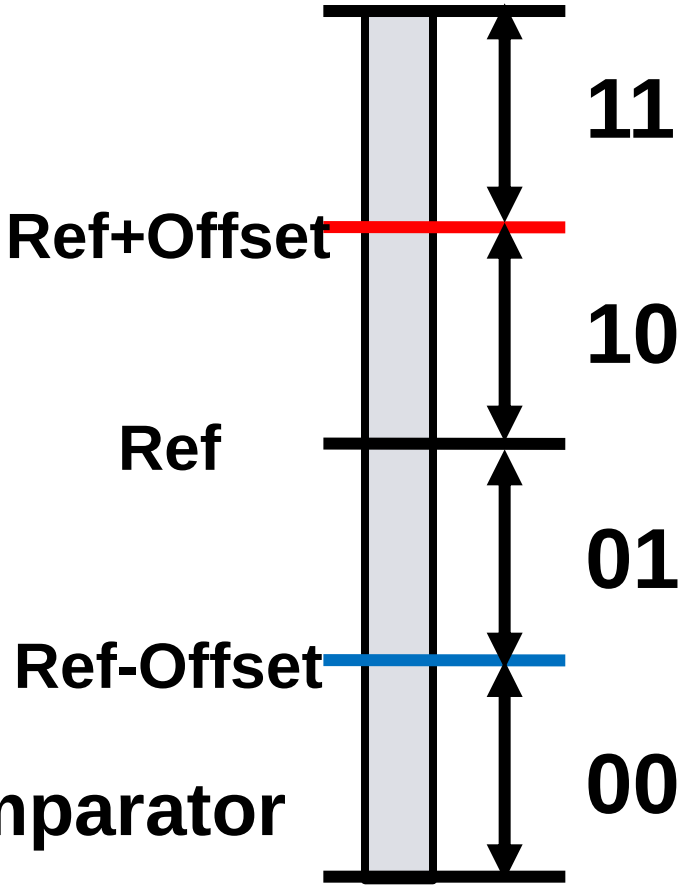
[ref] Z. Cao, JSSC 2009

- 2x speed improvement
  - *n* bit conversion with *n*/2 cycles
- Three-fold of analog elements required
  - 1.5x power, 3x area

SAR: Successive Approximation Register

Proposed 2bit/step Method

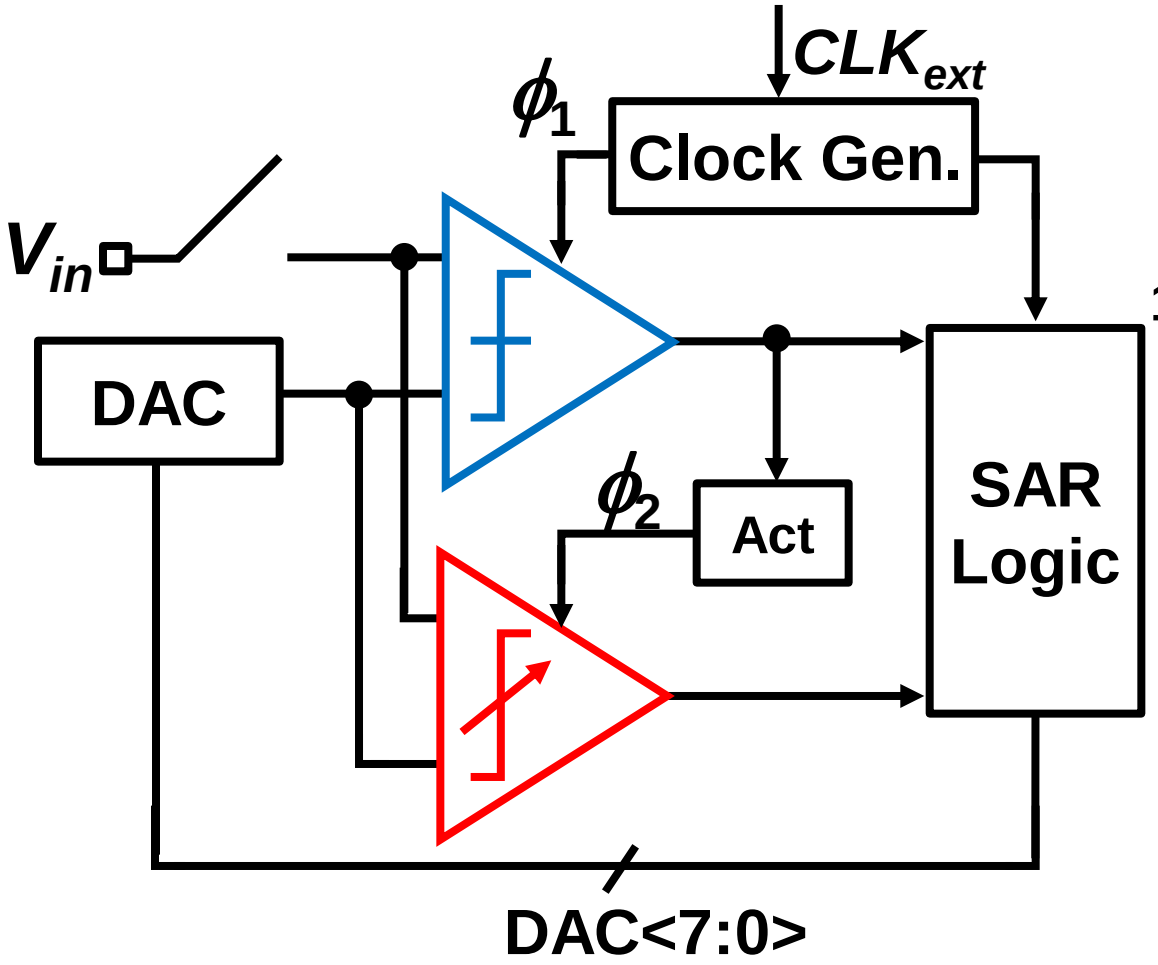


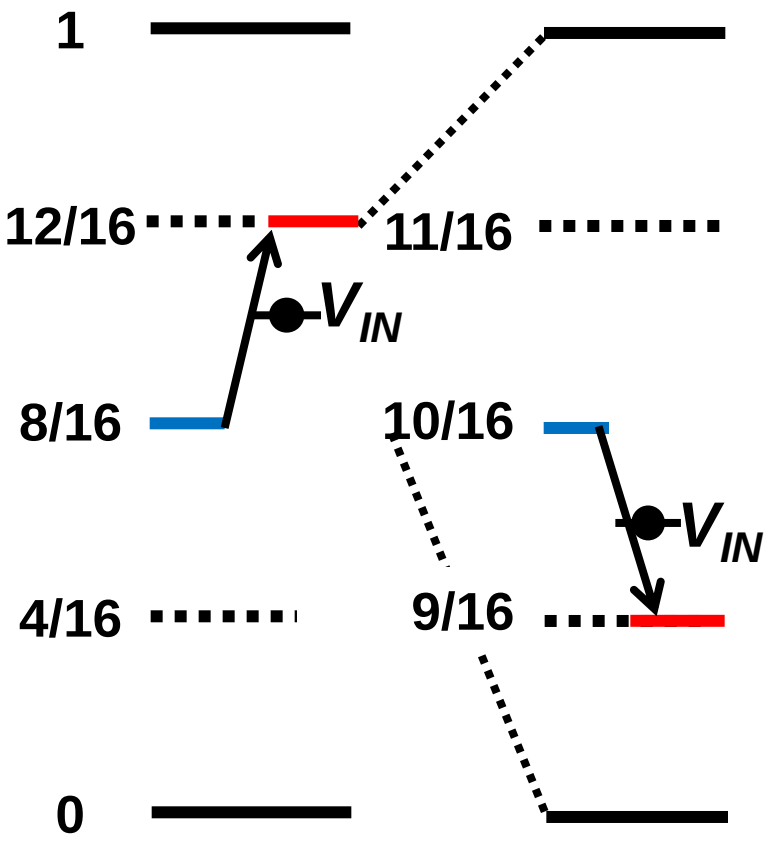


- Threshold configuring comparator
  - An offset added by intent
  - Only 1 reference generator required
- Low Power and high speed

Block Diagram

■ Comparators are activated successively



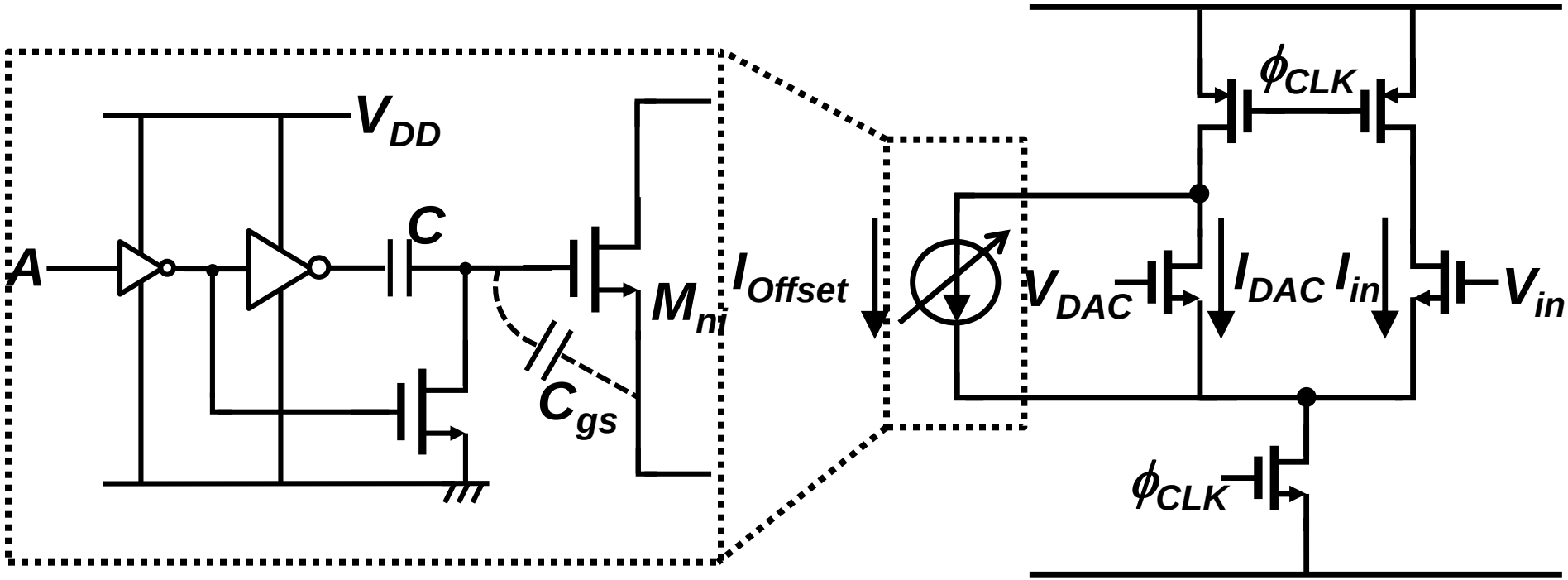


Cycle 1

Output: 10xx 1001

Wide Range Threshold Configuring

- $V_{DD}/2$ biased current source
  - Input signal common mode is $V_{DD}/2$
  - Comparator holds supply voltage noise immunity



Simplified Comparator Schematic

Comparison with state-of-the-art works