A Hybrid Low-Cost PLL Test Scheme based on BIST Methodology

Zhikuang Cai[1, a], Shixuan Que[2, b], Tingting Liu[2, b] and Haobo Xu[2, b]

[1]College of Electronic Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing, 210046, China

[2]National ASIC Systems Engineering Technology Research Center, Southeast University, Nanjing, 210096, China

[a]email: whczk@njupt.edu.cn, [b]email: {quesx/liutt/haobo_xu}@seu.edu.cn

Keywords: PLL; BIST; jitter; fault model; production test; parametric test

Abstract. In this paper, a hybrid built-in self-test (BIST) scheme is firstly proposed for phase-locked loop (PLL) production test and performance characterization. The scheme combines the structure test and function test in production test operation. The former is to detect hard faults and the latter is used to improve the soft fault coverage. Jitter measurement is selected as a typical parameter test in performance characterization mode, which includes vernier delay line (VDL) to measure timing jitter and undersampling technology to measure cycle-cycle jitter. The goal of the scheme is to enable complete production quality test and exact performance characterization.

Introduction

Phase-locked loop (PLL) is a mixed-signal building block used in a large number of applications. It is essential for systems like microprocessors, wireless transceivers and fiber optic receivers. With increasing complexity of mixed signal IC, the demand of preparing the low cost testing circuitry also gets increased. Sometimes PLL is the only analog block on the mixed-signal chips, and its test requirements directly translate into inflated product cost [1]. However, it is difficult to apply a test scheme for PLL, which need to solve the problem of testing environment, time consumption and the resources utilized at the same time. Measuring PLL off-chip is too expensive and impractical. A promising approach to the success of products with these properties is built-in self-test (BIST). Unfortunately, PLL remains a huge obstacle to utilize a BIST scheme owing to its tight feedback.

Previous Works

The tests required for PLL are typically Frequency Lock Test (FLT), locking time, jitter in different PLL operating modes and frequencies. Apart from the commonly used FLT, the literature [2] allows the estimation of forward path gain and measures the effects of leakage and mismatch. The paper [3] describes a PLL BIST scheme that is capable of testing all timing parameters of PLLs in production ICs such as jitter, duty cycle, phase delay, frequency ratio, and locking time. However, the PLL circuit is hard to describe, and it is difficult to evaluate the performance of the parameters extracted from the signals directly. Traditional function test is only for some specific test points on the circuit for functional verification and may cause the test to be redundant or inadequate.

Compared to the function test, defected-oriented structure test is more attractive. The structure test methods provide a long-term solution, especially if these methods are sufficient to prove associated with standard function tests. Defect-oriented test (DOT) not only can accurately detect physical defects of the PLL system, but also can diagnose with the fault model analysis. This technology usually makes use of the existing voltage controlled oscillator (VCO) and the divide-by-N block to measure the output as the signature of the system [4]. The paper [5] offers a structure test based on the function and implements high fault coverage with the minimal area consumption. In [6], a BIST solution testing catastrophe faults according to the Hamming distance is proposed. The literature [7] puts forward the technology of detecting both hard faults and soft faults with processing huge information. In conclusion, the fault model is still not mature. Moreover,

© 2015. The authors - Published by Atlantis Press

these above papers mention that it is needed to develop an innovative BIST technique to measure the PLL jitter in future works.

The PLL jitter is always measured in communication systems, high speed computation systems and so on. These systems pay close attention to the data loss and computation errors caused by jitter. Common BIST jitter measurement methods are based on vernier delay line (VDL), undersampling and others. The paper [2] comprehensively analyzes the PLL BIST circuit, and first gives the well-known jitter measurement based on delay chain. Sunter proposes a novel on-chip jitter measurement method in [8]. This undersampling method is used in a commercial EDA tool of Mentor Graphics. Nonetheless, almost of these methods are not separately in a production test environment. Additionally, the previous works are short of analyzing of different types of jitter according to application scenarios and researching each composition of jitter.

Proposed PLL BIST Scheme

In almost all published techniques, it is easy to find that these solutions ignore the unity of the structure test and the function test and just discuss unilaterally. Additionally, engineers' concerns are not the same for different testing goals. In the production test, designers pay attention to fault coverage, cost, and time; and precision and accuracy are concerned when characterizing performance. The paper [9] contains two BIST schemes which achieve internal node access and jitter measurement, respectively. The independence of the two schemes reduces resource sharing. The paper [10] takes production test and characterization as well as their common parts into account, but it can't be analyzed the relationship between parameters in detail, and the solution costs long test time.

As a result, a systematic and complete PLL test solution is proposed, as shown in Figure 1. This solution is a low cost and high quality scheme utilizing divide-and-conquer strategy. In production environment, this solution takes advantage of structure test technology to detect hard faults and supplements coverage with the function test technique. In performance characterization operation, the proposed scheme concentrates on jitter measurement.

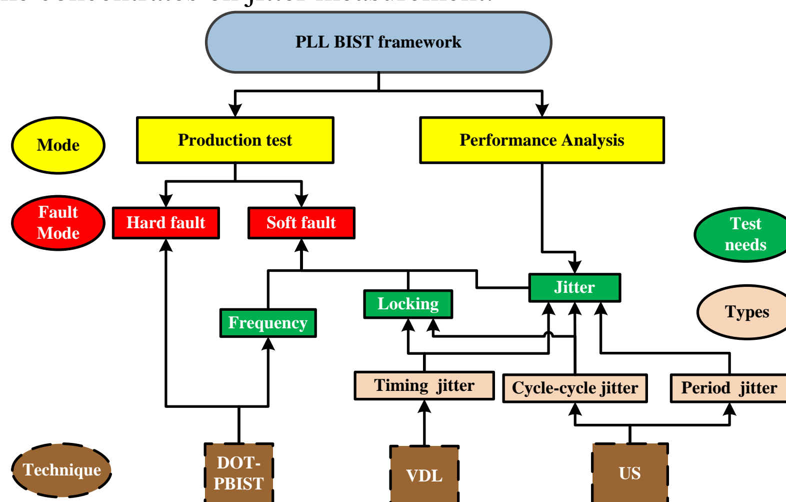


Figure 1. The proposed PLL BIST framework

1) Production test

The production test is often focused towards fault coverage and test cost. DOT is an efficient method for PLL production test. PLL fault model is extracted from the actual process defect. Nevertheless nowadays, PLL test methods haven't covered all defects due to immaturity of fault models. The structure test with BIST for PLL has a good coverage of hard faults.

This paper adopts the stuck-at fault model in digital components, which is the most widely accepted fault model for digital circuits. For the analog part, the hard fault model is used herein, including: gate-to-source short (GSS); gate-to-drain short (GDS); drain-to-source short (DSS); resistor-short (RS); capacitance-short (CS); gate-open (GO); drain-open (DO); source-open (SO); resistor-open (RO). The DOT-PBIST technique is adopted based on the fault models above in the

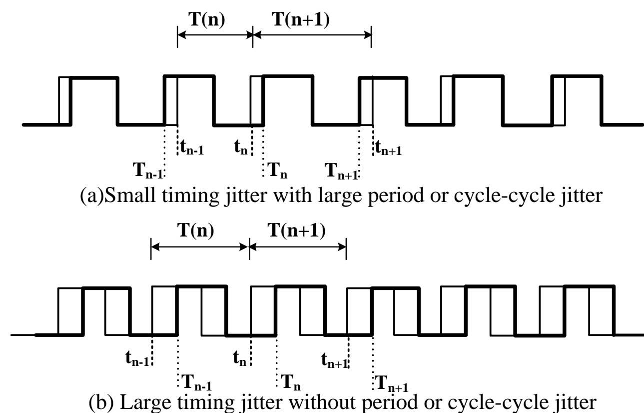
PLL BIST scheme.

However there is still no clear, unified soft fault model for PLL. Without using the soft fault model, the PLL fault coverage is actually going down. Due to many problems in soft fault model, this scheme still uses function test following the structure test to reflect the characteristics of faults, but its cost reduces compared to the traditional function test. Key parameters, such as the jitter and the locking, reflect the PLL performance. The proposed scheme uses function test, or rather, jitter measurement to supplement the soft fault coverage. In a word, this method can effectively improve overall fault coverage.

2) Performance characterization

The frequency of the VCO output signal is determined by the input voltage of the VCO. Because the frequency of the VCO output signal is the reciprocal of its period, the jitter has a close relationship with the actual frequency of the VCO output signal. Typically, PLL locking state can be represented by the frequency locking and the cycle-cycle jitter value. Because of the relevance between the timing jitter and the frequency locking, PLL locking state can be judged by jitter measurements.

As indicated above, there are different kinds of jitter, which are concerned in different applications. Sometimes only one of them is measured, which can’t accurately reflect the sufficient jitter information as shown in Figure 2. If the scheme only measures timing jitter, the PLL under test may meet the timing jitter requirement but fail to meet the period or cycle-cycle jitter requirement.



(a)Small timing jitter with large period or cycle-cycle jitter

(b) Large timing jitter without period or cycle-cycle jitter

Figure 2. Several cases of different types of jitter

Typically, the output signal of the VCO is used for jitter measurement. The most common methods include VDL technique and undersampling technique, the former measures timing jitter and the latter tests cycle-cycle jitter. However, VDL methodology requires a high frequency reference clock, resulting in the larger test cost. It can be proved that the timing jitter of the divider output signal is equal to that of the VCO output signal. But due to the frequency divider, N cycles of the VCO output signal can only generate one edge in the divider output signal. Additionally, the period jitter of the divider output signal is actually an accumulated jitter, which is equal to the sum value of the period jitter during N cycles of the VCO output signal. So does the cycle-cycle jitter. As a result, the divider output signal is used for VDL timing jitter measurement, and the undersampling technique selects the VCO output signal to measure cycle-cycle jitter.

All in all, this framework makes full use of VDL and undersampling schemes to measure jitter pointing at the different PLL needs. Measuring timing jitter in the divider output decreases the requirement of the reference clock and consequently reduces test cost.

Discussion

Traditional function test leads to time consuming and a huge cost. Now many scholars are interested in the structure test. DOT is an efficient method for PLL production test. PLL fault model is extracted from the actual process defects. However, in the actual case, the parameter fault model is not mature, therefore, if the hard fault is considered solely, then the fault coverage is inaccurate.

Additionally, in production test phase, structure test and function test were thought separately in previous works. Therefore, in this paper, we combine them together. Through analysis above, the characteristic of faults can be reflected by the PLL performance parameters. So in the production test, we use a DOT-PBIST circuit to detect hard faults, and the jitter measurement is regarded as a supplement. This ensures test coverage and significantly reduces test time and cost at the same time.

Measurement requirements of the different applications were overlooked in the past research on jitter measurement. Meanwhile, the methods were vague about the ingredients for the jitter. The timing jitter of the divider output signal and that of the VCO output signal are equal. Therefore, the proposed scheme uses the VDL circuit to test the divider output signal.

Finally, there are some intrinsic links between different measurement circuits, which reducing the hardware overhead. In production test mode, the jitter measurement is coarse resolution without a precise reference clock. Nonetheless, in performance characterization, it is completely different. The former is a low cost solution and the latter is of high quality. The goal of this scheme is to enable complete production quality test and exact performance characterization.

Conclusion

This systematic solution is a low cost and high quality BIST scheme. It uses divide-and-conquer strategy that considers production test and performance characterization, but shares the common test circuits to reduce cost. It is an introductory overview for PLL test engineers and designers. In conclusion, this scheme is a comprehensive and complete solution.

References

[1] Kim S, Soma M, “An all-digital built-in self-test for high-speed phase-locked loops”, in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 48(2), 141-150, 2001.

[2] Burbidge M J, Poullet F, Tijou J, et al, “Investigations for Minimum Invasion Digital Only Built-In “Ramp” Based Test Techniques for Charge Pump PLL's”, in Journal of Electronic Testing, 19(4), 481-490, 2003.

[3] Kinger R, Narasimhawsamy S, Sunter S, “Experiences with parametric BIST for production testing PLLs with picosecond precision”, IEEE International Test Conference, 1-9, 2010.

[4] S. Kim, M. Soma and D. Risbud, “An effective defect-oriented BIST architecture for high-speed phase-locked loops”, IEEE VLSI Test Symposium, 231 -236, 2000.

[5] Hsu C L, Lai Y, Wang S W, “Built-in self-test for phase-locked loops”, in IEEE Transactions on Instrumentation and Measurement, 54(3), 996-1002, 2005.

[6] Youbean KIM, Kicheol KIM, Incheol KIM, “A New Built-in Self Test Scheme for Phase-Locked Loops Using Internal Digital Signals”, in IEICE transactions on electronics, 91(10), 1713-1716, 2008.

[7] Guo Yu, Peng Li, “A Methodology for Systematic Built-in Self-Test of Phase-locked Loops Targeting at Parametric Failures”, IEEE International Test Conference , 1-10, 2007.

[8] Sunter S, Roy A, “Circuit and method for measuring jitter of high speed signals”, U.S. Patent 7,158,899, 2007.

[9] Dasnurkar S, “Methods for high volume mixed signal circuit testing in the presence of resource constraints”, University of Texas, 2012.

[10] Burbidge M J, Lechner A, Bell G, et al, “Motivations towards BIST and DfT for embedded charge-pump phase-locked loop frequency synthesisers”, IEE Proceedings Circuits, Devices and Systems, 151(4), 337-348, 2004.