Thermo-Mechanical Analysis and Fatigue Life Prediction for an Electronic Surface-Mount Device (SMD)

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Abstract: This paper is aimed to investigate on thermal and thermo-mechanical behavior of an electronic Surface-Mount Device (SMD). The main target of the present investigation is to apply a numerical procedure to assess the fatigue life for the solder layer that represent, in general, one of the weakest part of the electronic devices. FE-based models were built-up by considering different conditions in model implementation in order to simulate, from one hand the worst thermal condition for the device, and from another one different failure models related to thermal cycling and power cycling conditions. Simulations were carried-out both in steady and transient conditions allowing to estimate the device thermal maps, the device thermal resistance and impedance, the stress-strain distributions, the plastic deformations and finally to assess the number of cycles to failure of the constitutive solder layer.

Keywords: Surface-Mount Device (SMD), FE, Thermal cycle, Power cycle, Coffin-Manson.

1. Introduction

Electronic devices produce a very high rate of specific heat compared to their dimensions. Overheating and thermo-mechanical stresses are the main causes of failure for electronic equipment. In fact, exceeding in maximum safe operating temperature means a strong reduction of semiconductors efficiency, reliability and lifetime [1]. For those reasons, thermal design represents an unavoidable step in pre-production phase [2], in order to ensure reliability and performance of the electronic devices. In service, electronic components are subjected to temperature fluctuations due to heat dissipation of silicon-based chips (power transients) in the surrounding environment. Combined with the thermal expansion mismatch between the different materials of the assembly, cyclic thermal loading results in stress reversals and potential accumulation of inelastic strain in the solder joint. This inelastic strain accumulates with repeated cycling and ultimately causes solder joint cracking and interconnect failure [3]. In literature, the fatigue life of power devices is usually evaluated by applying thermal and power cycles. This cycle is repeated within a range from a high temperature to a low temperature. Otherwise, in an actual operating environment, a power device works in a power cycle, during which device is switched ON/OFF [4]. During thermal cycling, the solder layer reaches an uniform temperature. In case of the power cycle becomes short, this state is different from the real active state of the power device, in fact the real temperature distribution on the solder layer is not uniform. Therefore, there is a difference between a fatigue life evaluation that uses power cycling and one that uses temperature cycling [5]. At low frequency and high temperature, it was predominantly time-dependent, while cycle becomes determinant at high frequency and low temperature [6]. From a modelling point of view, there are different approaches in order to study the different regimes of the fatigue phenomena: low-cycle fatigue (LCF) and high-cycle fatigue (HCF).. Because of the demand for high power density electronic devices, coupled thermo-mechanical analyses oriented to the solder joint fatigue life prediction are becoming a topic of very high interest [7]. In this framework, a numerical analysis on thermo-mechanical behavior and fatigue life prediction for an electronic Surface-Mount Device (SMD) is proposed.

2. Methods

Models were implemented and solved using COMSOL Multiphysics. In our study, we numerically analysed thermal state, thermal-induced stress-strain and we carried-out a LCF life prediction for a Surface-Mount Device (SMD). In following, geometry and model

implementation are firstly presented, then some of the obtained results are shown.

2.1 Geometry of the numerical model

The geometry of the studied device is shown in Fig. 1. The device is mainly made by a copper frame, a lead-free solder layer (also called solder die) and a silicon die equipped with a front metal, which is connected to device pins by several ribbons.

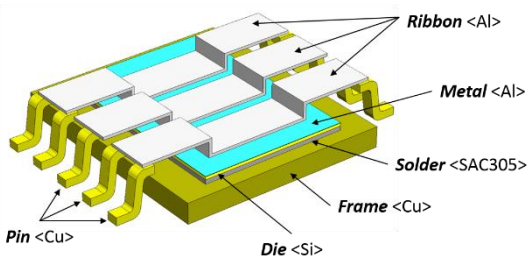


Figure 1. Geometry of the numerical model.

Physical properties of materials considered in our study are reported in Tab. 1.

Table 1. Physical properties of materials.

	ρ	k	C_p
Material	[kg/m^3]	[W/(m·K)]	[J/(kg·K)]
Copper	8700	400	385
Solder	7370	75	220
Silicon	2329	130	700
Aluminium	2700	238	900

	α	E	ν	σ_Y
	[K^{-1}]	[MPa]	[-]	[MPa]
Copper	1.7E-5	1.1E5	0.35	48
Solder	2.2E-5	5.0E4	0.36	34
Silicon	2.6E-6	1.7E5	0.27	40
Aluminium	2.3E-5	7.0E4	0.33	11

2.2 Thermal model

In the first step of our investigation, labelled from now (Case A), a thermal simulation was carried-out for the device, both in steady and transient conditions. The governing equation reads as follows:

$$\rho C_p \frac{\partial T}{\partial t} = \nabla \cdot (k \nabla T) + Q \qquad (1)$$

Eq. (1) represents the energy equation, where T is the temperature, ρ is the density, C_p is the specific heat at constant pressure and Q is the volumetric heat generation. This analysis was performed considering the worst working conditions in order to compute the maximum temperature, the device thermal resistance and impedance during the module functioning. To this goal, the bottom surface of the frame was held at constant temperature (T_{ref}) and a volumetric heat source was applied to the device. Values of thermal heat source correspond to the maximum power supplied to the device during its functioning. On all other boundaries, an insulation condition was applied.

2.3 Thermo-mechanical model

In a second step of our investigation, a thermo-mechanical simulation was carried-out. The governing equation reads as follows:

$$\sigma - \sigma_0 = C : (\varepsilon - \varepsilon_0 - \alpha\theta) \qquad (2)$$

Eq. (2) is the Hooke's law relating the stress-strain of material, where σ is the stress tensor, σ_0 and ε_0 are initial stress and strain, C is the fourth order elasticity tensor, α is the coefficient of volumetric thermal expansion and ε represents the total strain tensor, defined as:

$$\varepsilon = \frac{1}{2}(\nabla s + (\nabla s)^T) \qquad (3)$$

Eq. (2) and (3) were solved in order to detect the stress-strain thermally induced on the constitutive materials. The term θ appearing in Eq. (2) denotes the difference between local temperature (T) and the strain reference one (T_{ref}), that corresponds to the frame temperature. This analysis was performed considering the worst working conditions in order to compute the related stress-strain distribution during the device functioning. From the mechanical point of view, a fixed constraint was chosen for the bottom surfaces of frame and pins, maintaining free all other boundaries of the model. The structural load was related to the thermal computed state only.

2.4 Fatigue model

In the final step of our investigation, labelled from now on (Case B) a thermal fatigue life

prediction was carried-out. The target of this analysis was to assess the fatigue life of solder die subjected to thermal cycles and power cycles. The model proposed for predicting the fatigue life of solder layer is *plastic-strain* based. As usually done when applying a *plastic-strain* approach, time-independent plastic strain conditions are applied and the resulting stresses within a component are analysed. Thermal fatigue-induced strains from CTE mismatch fall under this category.

2.4.1 Thermal cycle test

A computational model was built considering a thermal cycle between two environmental fixed temperatures. To this goal, we solved the energy equation in "passive" conditions. That means we applied different external conditions as thermal load to the device. In particular, no internal heat source was considered, while we applied two different thermal states (T_c = -40 [°C] and T_h = 125 [°C]) to the entire device external boundaries. This procedure simulates the device standing inside a climatic test room, held at two different constant control temperatures (cold temperature, T_c, and hot temperature, T_h). By means of this approach, the plastic strain amplitude ($\Delta\varepsilon_p$) was evaluated by using the achieved thermal states. The ε_p is defined as the effective plastic strain, computed as a component of the total strain [8].

Then, in analogy to the Basquin equation, we applied the Coffin-Manson equation [9] to compute the number of cycles to failure, reading as follows:

$$\frac{\Delta\varepsilon_p}{2} = \varepsilon'_f \left(2N_f\right)^c \qquad (4)$$

where ε'_f is the fatigue ductility coefficient, c is the fatigue ductility exponent of the solder material and N_f is the number of cycles to failure.

2.4.2 Power cycle test

Then, a computational model was built considering the square wave power cycle, shown in Fig. 2, as thermal load for the thermo-mechanical simulation. The device is cyclically switched ON/OFF between two power states: (a) the device is switched OFF and the dissipated power was considered naught (P = 0 [W]); (b) the device is switched ON and the dissipated power was considered at the maximum value (P = P_{max}). Several tests were performed changing the value of P_{max}, in order to study different power dissipation conditions.

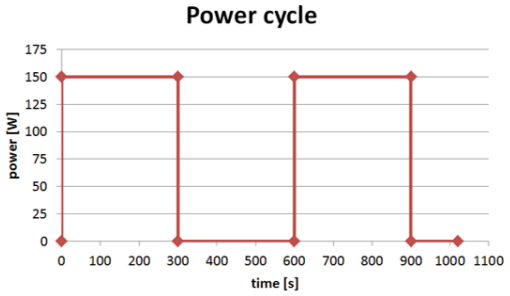


Figure 2. Square wave power cycle (P_{max} = 150 [W]).

The plastic strain amplitude $\Delta\varepsilon_p$ was evaluated and then it was used in (4) in order to determine the number of cycles to failure N_f for solder layer.

2.5 Numerical solution

Continuous equations were spatially discretized by a Finite Element approach based on the Galerkin method on non-uniform and non-structured computational grids made of tetrahedral Lagrange elements of order 2. Influence of spatial discretization was preliminary studied in order to assure mesh-independent results. Finally, a computational grid made of about 45,250 elements was retained for computations, giving 137,399 degrees of freedom. A snapshot of the used mesh is presented in Fig. 3.

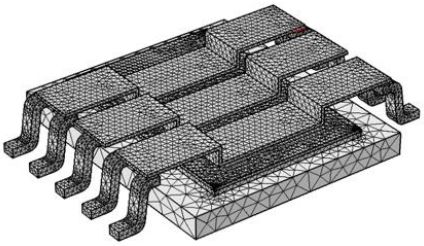


Figure 3. Mesh of the numerical model.

Steady solutions of discretized equations were carried-out by applying an iterative dumped Newton-Raphson scheme [10], classically based on the discretized PDE linearization by a first-order Taylor expansion. Algebraic systems of equations coming from differential operators

discretization were solved by an PARDISO package, a direct solver particularly efficient in order to solve unsymmetrical sparse matrixes by a LU decomposition method.

For time-marching simulations we adopted an Implicit Differential-Algebraic (IDA) solver based on a variable-order and variable-step-size Backward Differentiation Formulas (BDF) [11].

3. Results

Results were carried-out for different geometrical and constitutive configurations of the power device. In particular, different layers thickness were investigated and different physical properties were considered in solving the governing equations. In the following paragraphs, we present an extract of those results.

3.1 Thermal analysis results

The thermal distribution obtained for a steady simulation of the device, when it is switched ON and the maximum power is supplied to, is shown in Fig. 4. In the enlargement of the picture, we report the maximum junction temperature value (T_{jc} (MAX) = 44.4 [°C]) which was detected by simulation on the front metal of chip. By means of time-dependent simulations, we obtained the thermal impedance curves computed for the most critical thermal state. Those results were exploited for assessing the thermal resistance for the studied device. The computed value of the junction-to-case thermal resistance is $R_{th\text{-}jc}$ = 0.13 [°C/W]. Fig. 5 reports the thermal impedance curve computed for (Case A) conditions.

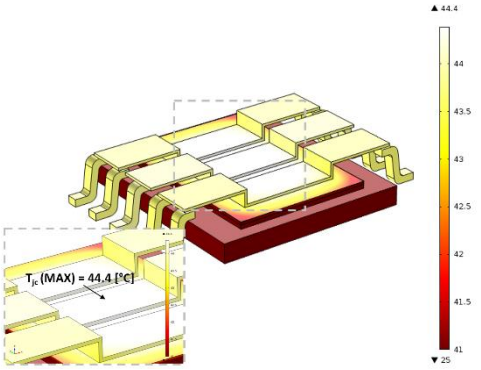


Figure 4. Thermal map [°C] on the device (Case A).

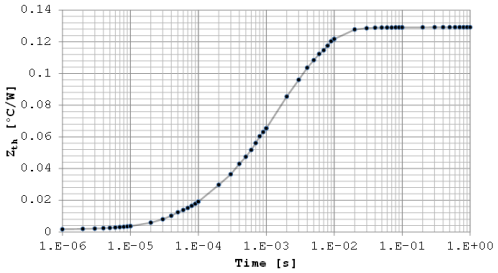
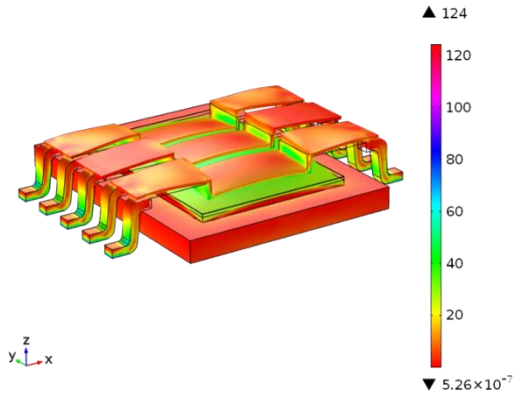


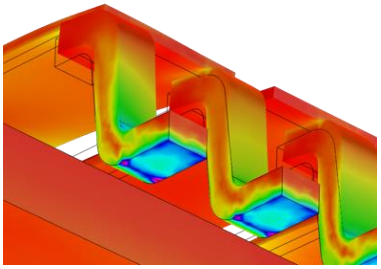
Figure 5. Thermal impedance curve computed during a transient analysis in (Case A) configuration.

3.2 Thermo-mechanical analysis results

The von Mises stress distribution, caused by the thermal load in (Case A) configuration, is shown in Fig.6a-b. In Tab. 2 the maximum value of von Mises stress computed for each device layer is compared to the ultimate strength of the constitutive materials. From comparison, tensile resistance results widely verified in spite of the worst thermal case considered.



(a)



(b)

Figure 6. Von Mises stress distribution [MPa] in deformed configuration (50X) (Case A).

Table 2. Thermal resistance check in worst thermal conditions.

Material	Layer	von Mises stress	Ultimate strength
		[MPa]	[MPa]
Copper	Frame	20.4	210
Copper	Pin	123.8	210
SAC305	Solder	34.9	276
Silicon	Die	55.0	172
Aluminum	Metal	66.5	150
Aluminum	Ribbon	83.2	150

3.3 Thermal cycle test analysis results

Thermal states computed in (Case B) configuration were exploited for estimating the effective plastic strain distribution. The maximum value of $\Delta\varepsilon_p$ was detected on the solder layer, joining the frame and the silicon die. In particular, the most critical value of the effective plastic strain was detected in correspondence of the solder layer corners. This is maybe due to the geometrical singularity.

Fig. 7 shows the effective plastic strain distribution in proximity of solder layer corner, where the highest value of ε_p was found in both environmental thermal conditions (T_c and T_h). This result well agrees with experimental evidences in literature obtained by SAM (Scanning Acoustic Microscope) observations developed on SMD devices [8, 12-14].

As previously mentioned, from plastic strain evaluation it is possible to numerically assess the potential number of cycles to failure. In consequence, we were able to estimate the expected number of cycles to failure for the solder layer, that are well-known the weakest part of the module from this point of view. From our investigation, the solder die fatigue life prediction is approximately 10,802 cycles. Successively a comparison of the fatigue life of SAC305 to SnPb solder was performed. From results, the fatigue life prediction for SnPb solder die is approximately 208,658 cycles. This result well agrees with evidences in literature showing that the fatigue life of SAC305 is considerably lower that SnPb solder [15].

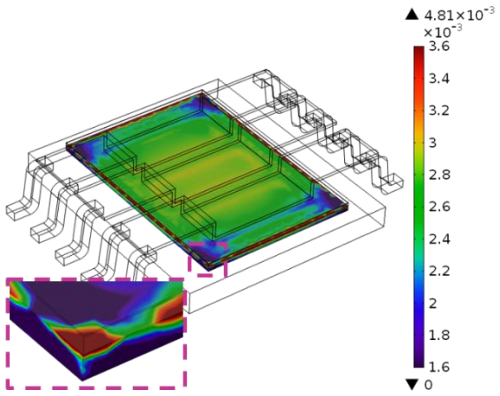


Figure 7. Effective plastic strain distribution for SAC305 solder die (T_h = 125 [°C]).

3.4 Power cycle test analysis results

The number of cycles to failure for solder layer obtained for power cycle analysis is shown in Fig.8. The crack propagation is nearly concentric, originating almost directly under the silicon chip that is the hottest point [12]. From results, the fatigue life prediction for SAC305 solder die is approximately $2.83 \cdot 10^7$ cycles and for SnPb solder is approximately $1.83 \cdot 10^8$ cycles.

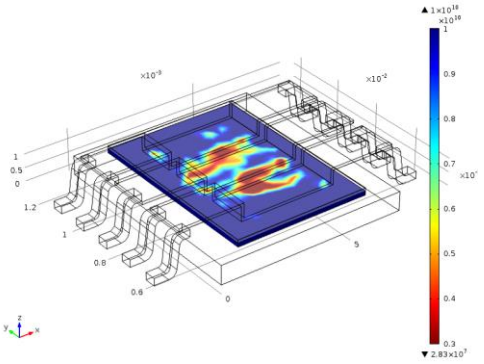


Figure 8. Number of cycles to failure for SAC305 solder die.

4. Conclusions

A numerical investigation was carried-out in order to assess thermal state, thermo-mechanical behavior and fatigue life of a Surface-Mount Device (SMD). Firstly, a thermal characterization was made considering the device switched ON and supplying a heat source corresponding to the maximum working power. From steady and transient simulations carried-out in this

configuration, the maximum temperature, the thermal resistance and the thermal impedance were computed. The obtained thermal state was then exploited to solve a thermo-structural analysis oriented to evaluate the stress-strain distribution on the device in the most critical conditions. Secondly, thermal analysis was performed considering the device switched OFF and applying two different external thermal loads. This configuration was implemented to assess the thermal fatigue behavior during a thermal cycle inside a climatic test room, held at two different constant control temperatures. The obtained thermal states were then exploited to determinate, by a Coffin-Manson approach, the effective plastic strain, from which the number of cycles to failure was estimated for solder layer. Similarly, a fatigue life prediction was performed during a power cycle test (ON/OFF) in order to evaluate the number of cycle to failure for solder layer. From results, it appears that thermal levels are lower than potential critical values for constitutive materials, even in the worst working conditions. Similarly, the maximum von Mises stress computed by the thermo-mechanical analysis is lower than the ultimate tensile strength of materials. The fatigue life prediction coming from our investigation results in good agreement with literature evidences and experimental findings, both qualitatively (device portion subjected by the high plastic strain) and quantitatively (number of cycles to failure).

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7. Nomenclature

Symbol	Quantity	SI Unit
C	Fourth order elasticity tensor	Pa
C_p	Specific heat at constant pressure	J/(kg·K)
c	Fatigue ductility exponent	-
E	Young's modulus	Pa
k	Thermal conductivity	W/(m·K)
N_f	Number of cycles to failure	-
Q	Volumetric heat generation	W/m^3
$R_{th\text{-}jc}$	Junction-to-case thermal resistance	°C/W
s	Displacement	m
T	Temperature	K
T_c	Cold temperature	K
T_h	Hot temperature	K
T_{jc}(MAX)	Maximum junction temperature	K
T_{ref}	Reference temperature	K
$Z_{th\text{-}jc}$	Junction-to-case thermal impedance	°C/W
α	Coefficient of volumetric thermal expansion	K^{-1}
ε	Total strain tensor	-
ε_0	Initial strain	-
ε'_f	Fatigue ductility coefficient	-
ε_p	Effective plastic strain	-
θ	$T\text{-}T_{ref}$	K
ν	Poisson's ratio	-
ρ	Density	kg/m^3
σ	Stress tensor	Pa
σ_0	Initial stress	Pa
σ_Y	Yield strength	Pa