Cost and Benefit Models for Logic and Memory BIST

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Abstract

We present cost and benefit models and analyze the economics effects of built-in self-test (BIST) for logic and memory cores. In our cost and benefit models for BIST, we take into consideration the design verification time and test development time associated with testability. Experimental results for logic BIST and memory BIST examples show that a threshold volume exists when BIST is profitable for the logic core under consideration—it is not recommended for a higher volume. However, BIST is a good choice for memory cores in general.

1. Introduction

Built-in self-test (BIST) is receiving growing attention with the advent of core-based system-on-chip (SOC) design, which is a natural sequel of deep-submicron VLSI technology. When cores from different vendors are integrated together on the system chip, the difficulty level of chip testing rapidly multiplies. Among the most apparent issues are core isolation, core access, system diagnosis, test reuse, test compaction, tester qualification, intellectual property (IP) protection, etc. For all these issues, BIST is a potentially good solution, if used properly. However, we do care about hardware overhead (area, pin, etc.), performance penalty, and extra design effort that may be associated with BIST. An economics (i.e., costs and benefits) analysis tool for weighing the costs and benefits of BIST (and other design-for-testability methodologies) is definitely helpful for the project managers and designers (see, e.g., [1, 2, 3, 4, 5, 6]).

We analyze the economics effects of BIST for logic and memory cores in this paper. BIST is a relatively mature DFT methodology, but techniques used in logic BIST (LBIST) may be quite different from those used in memory BIST (MBIST). LBIST is normally based on pseudo-random pattern generator and signature analyzer techniques with scan paths [7]. MBIST, on the other hand, is normally based on the march algorithms [8, 9].

In this paper we propose economics models for estimating both the costs and benefits associated with LBIST and MBIST. We have performed experiments on these models, and the results show that a threshold volume exists when LBIST is profitable for the case we studied, i.e., it is not recommended for a volume higher than the threshold. However, MBIST is shown to be a good choice in general, except when the volume is low.

2. Models for LBIST

We consider recurring and nonrecurring costs and benefits for LBIST. In our model, the cost associated with LBIST mainly comes from area overhead. In return, reduced tester time and development time (i.e., time-to-market) represent the recurring and nonrecurring benefits, respectively.

2.1. Benefit due to Early Market Entry

Conventionally, DFT has been considered to lengthen time-to-market, since extra design effort is required. However, we have observed that the product development cycle may actually be shortened if proper DFT methodology is adopted, saving verification and debugging time (mainly in the prototyping stage) [5, 6].

We divide the product development cycle into three stages: the design stage, test development stage, and verification stage. Our development time model (T_d) thus is

$$T_d = T_{dsgn} + T_{td} + T_{veri}, \tag{1}$$

where T_{dsgn} is the design time, T_{td} is the test development time, and T_{veri} is the verification (including prototyping) time. When LBIST is adopted in a design, the development time $T_{d_{LB}} = T_{dsgn_{LB}} + T_{td_{LB}} + T_{veri_{LB}}$.

Our design time model is

$$T_{dsgn} = \frac{g}{N_{d_{eng}} R_g}(1-\rho)(\frac{1}{1-\kappa}), \quad (2)$$

where g is the gate count, $N_{d_{eng}}$ is the average number of engineers, R_g is the designer skill level, ρ is the design reusability factor, and κ is its complexity. The two variables, ρ, and κ, are normalized between 0 and 1. The amount R_g is measured in number of gates designed per day. With LBIST, ρ is assumed to remain unchanged. Also, g is expected to increase when LBIST is adopted, i.e.,

$$g_{LB} = (1 + \alpha_{LB\_area})g, \quad (3)$$

where α_{LB_area} represents the area overhead of LBIST, which will be discussed later. The complexity parameter, κ, can be estimated from the complexity of the functionality and specification (e.g., timing and power specifications and silicon budget) of the target circuit. When adding LBIST to the design, the relation between κ and κ_{LB} is modeled as

$$\kappa_{LB} = \kappa + (1-\kappa) \times \alpha_{LB\_area}. \quad (4)$$

To calculate $T_{dsgn_{LB}}$, we use g_{LB} and κ_{LB} in Eq. (2). We adopt the test generation time model in [10], i.e., our test development time model is

$$T_{td} = \alpha_{td} \cdot e^{g}, \quad (5)$$

where α_{td} is a constant factor that relates the test generation time to the IC gate count g. When adding LBIST to the design, the test development time $T_{td_{LB}}$ is modeled as

$$T_{td_{LB}} = \frac{1}{590} \cdot \alpha_{td} \cdot e^{g_{LB}}, \quad (6)$$

where the factor "590" represents the test length reduction ratio due to LBIST, and will be explained later. Here we assume that the test development time is in proportion to the test length. The verification time includes the time for design verification, design debugging, and prototyping (including engineering runs). Our verification time model is

$$T_{veri} = T_{v1} + 590 \cdot T_{v2}, \quad (7)$$

where T_{v1} is the part of the verification time that is independent of circuit testability, while T_{v2} is testability dependent. Again, the number "590" represents the saving factor in verification time due to the improvement in circuit controllability and observability. Our model for $T_{veri_{LB}}$ is therefore

$$T_{veri_{LB}} = T_{v1} + T_{v2}. \quad (8)$$

After calculating $T_{dsgn_{LB}}$, $T_{td_{LB}}$, and $T_{veri_{LB}}$, $T_{d_{LB}}$ is obtained and the amount of time saved by LBIST is

$$T_{saving} = T_d - T_{d_{LB}}, \quad (9)$$

which is used in the market life cycle model for estimating the revenue gain. Figure 1 [5, 6] shows a market window with three periods: the growth period, maturity period, and decline period. Early to the market results in extra revenue as represented by the shaded region in the figure.

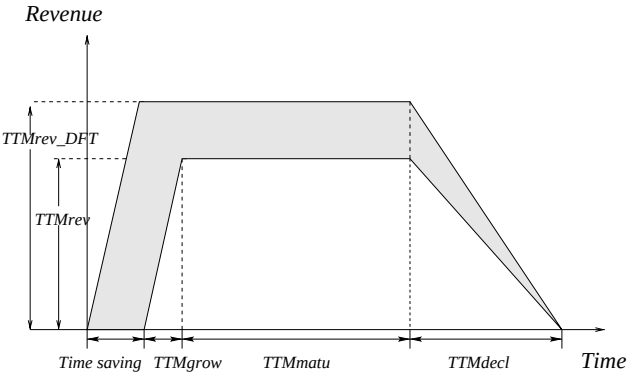

Figure 1. The Market Life Cycle Model.

The revenue of a product with a delay in time-to-market is

$$R = (TTM_{grow} + 2TTM_{matu} + TTM_{decl})TTM_{rev}/2. \quad (10)$$

The overall revenue from the product with an early time-to-market (due to LBIST) can be estimated as [6]

$$\begin{aligned} R_{LB} =& ((TTM_{grow} + 2TTM_{matu})TTM_{rev}/2) \\ & \times \left(\frac{T_{saving} + TTM_{grow} + TTM_{matu}}{TTM_{grow} + TTM_{matu}}\right)^2 \\ & + (TTM_{decl} \cdot TTM_{rev}/2) \\ & \times \frac{T_{saving} + TTM_{grow} + TTM_{matu}}{TTM_{grow} + TTM_{matu}}, \end{aligned} \quad (11)$$

where TTM_{grow} is the market growth period, TTM_{matu} is the market maturity period, TTM_{decl} is the market decline period, and TTM_{rev} is the maximal revenue per month at the maturity period without DFT. Therefore, the benefit can be estimated as

$$B_{TTM} = R_{LB} - R. \quad (12)$$

2.2. Man-Power Benefit due to Shortened Development Time

The benefit for product development man-power is

$$B_{Labor} = N_{d_{eng}} \cdot U_{d_{eng}} \cdot T_{saving}, \quad (13)$$

where $N_{d_{eng}}$ is the average number of engineers and $U_{d_{eng}}$ is the average cost of an engineer per day. Note however that T_{saving} is not necessarily positive.

2.3. Cost due to Area Overhead

The LBIST area overhead ranges from 4% to 15% in most cases [10]. Our model for the core area with LBIST is

$$A_{LB} = (1 + \alpha_{LB\_area})A, \tag{14}$$

where α_{LB_area} is the area overhead. As to the yield affected by the area overhead, we adopt the Poisson yield model [11]:

$$Y = e^{-\rho_d \cdot A}, \tag{15}$$

where ρ_d is the defect density. The cost per die due to the area overhead is modeled as [10]

$$C_{Area} = N_v \cdot \frac{U_{wafer}}{\pi R_{wafer}^2 \cdot \alpha_{util}} \left(\frac{A_{LB}}{Y_{LB}} - \frac{A}{Y} \right), \tag{16}$$

where N_v is the production volume, U_{wafer} is the cost per wafer, R_{wafer} is the radius of the wafer, and α_{util} is the utilization ratio of the wafer. A typical value for α_{util} is 90%.

2.4. Benefit due to Reduced Testing Cost

BIST reduces off-chip communication, so the external tester can be greatly simplified. The testing cost savings thus can be translated to the tester cost:

$$B_{Test} = N_v \cdot \frac{R_{dep}}{T_{sec\_year}} (U_{Leq} \cdot T_t - U_{Leq_{LB}} \cdot T_{t_{LB}}), \tag{17}$$

where U_{Leq} is the price of the external logic tester to access the chip without LBIST, $U_{Leq_{LB}}$ is the price of the tester to access LBIST, R_{dep} is the annual depreciation rate of the tester, T_{sec_year} is the number of seconds in one year (i.e., 31,536,000), T_t is the tester time for the core without LBIST, and $T_{t_{LB}}$ is the tester time for the core with LBIST.

With LBIST, the pin count seems to increase. However, using self test, the pin and frequency requirement of the tester actually is greatly reduced, i.e.,

$$U_{Leq_{LB}} = \alpha_{freq} \cdot \frac{P_{LB}}{P} \cdot U_{Leq}, \tag{18}$$

where α_{freq} is the tester frequency factor, P_{LB} is the number of pins for the simple inexpensive tester to access LBIST (typically ranging from three to five if the core is tested entirely by LBIST), and P is the pin count of the core without LBIST. Note that LBIST also can reduce test length in most cases, as compared with functional or even sequential ATPG patterns. According to our testability experiment which will be discussed later, adding LBIST causes a reduction of $\frac{1}{590}$ in test length, i.e.,

$$T_{t_{LB}} = \frac{T_t}{590}. \tag{19}$$

In summary, the total benefit for using LBIST is

$$B = B_{TTM} + B_{Test} + B_{Labor} - C_{Area}. \tag{20}$$

3. Models for MBIST

For MBIST, we will also consider costs due to extra design effort and area overhead, and benefit due to reduced testing cost.

3.1. Cost due to Extra Development Effort

Our model for the extra development cost in terms of man-power is

$$C_{Labor} = N_{d_{eng}} \cdot U_{d_{eng}} \cdot T_{MB}, \tag{21}$$

where $N_{d_{eng}}$ is the average number of extra engineers for MBIST, $U_{d_{eng}}$ is the average cost of engineer per day, and T_{MB} is the development time associated with MBIST.

3.2. Cost due to Area Overhead

Our model for the MBIST overhead is [9]

$$A_{MB} = A\left(1 + \frac{log_2(M\_SIZE)}{M\_SIZE} \times 1.33\right), \tag{22}$$

where M_SIZE is the memory capacity. We use the same yield model as shown in Eq. (15). The silicon cost due to area overhead is

$$C_{Area} = N_v \cdot \frac{U_{wafer}}{\pi R_{wafer}^2 \cdot \alpha_{util}} \left(\frac{A_{MB}}{Y_{MB}} - \frac{A}{Y} \right). \tag{23}$$

3.3. Benefit due to Reduced Testing Cost

MBIST reduces the time that memory testers have to be used [9]. Therefore, similar to Eq. (17), the benefit that we gain from this is

$$\begin{aligned} B_{Test} = & N_v \left[\frac{R_{dep}}{T_{sec\_year}} (U_{Meq} \cdot T_t - U_{Meq} \cdot T_{t1_{MB}}) \right. \\ & \left. - \frac{R_{dep}}{T_{sec\_year}} \times U_{Meq_{MB}} \times T_{t2_{MB}} \right], \end{aligned} \tag{24}$$

where $T_{t1_{MB}}$ and $T_{t2_{MB}}$ represent the amount of time the memory tester and logic tester are used for the chip with MBIST, respectively; U_{Meq} is the price of a memory tester; $U_{Meq_{MB}}$ is the price of a logic tester to access the MBIST circuit. Similarly to Eq. (18), the relation between $U_{Meq_{MB}}$ and U_{Meq} is

$$U_{Meq_{MB}} = \alpha_{freq} \cdot \frac{P_{MB}}{P} \cdot U_{Meq}, \tag{25}$$

where P_{MB} is the number of pins for the logic tester to access the memory core with MBIST (it normally ranges from 4 to 10, and the default is 8 [9]). Also, we assume $T_{t1_{MB}} = T_t/3$ and $T_{t2_{MB}} = 2T_t/3$.

In summary, the total benefit from MBIST is

$$B = B_{Test} - C_{Labor} - C_{Area}. \quad (26)$$

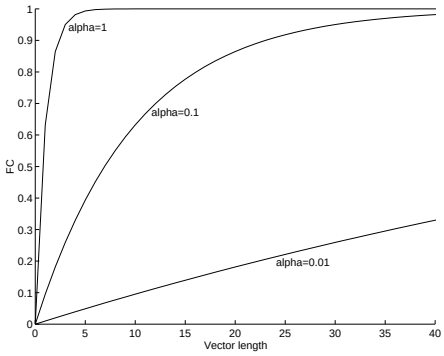

Figure 2. Fault coverage (FC) vs. test length for various α_{FC} values.

4. Testability Analysis

Figure 2 shows the relation between fault coverage (FC) and test length (number of vectors, V) [6, 12], which can be modeled by

$$FC = 1 - e^{-\alpha_{FC}V}, \quad (27)$$

where α_{FC} is the factor representing the growth rate of FC. We have experimented the model using ISCAS89 benchmark circuits [13], and the results are listed in Fig. 3.

The testability improvement ratio, λ_{LB}, varies from one to about one thousand. The weighted arithmetic mean of α_{LB_tb} is calculated as follows:

$$\alpha_{LB\_tb} = \frac{\sum_{circuits}(N \cdot \lambda_{LB})}{\sum_{circuits} N} = 590, \quad (28)$$

where N is the number of nets in a circuit, e.g., for s1488, $N = 1488$. According to the result, adding LBIST causes a reduction in test length and testing time by a factor of "590", as has been shown previously. Note that the value 590 was obtained empirically from the benchmark circuits. For practical applications, a better result can be obtained by looking at the specific class of circuits under consideration.

5. LBIST Case

We use the chip reported in [14] as a case for our LBIST model evaluation. The costs and benefits associated with

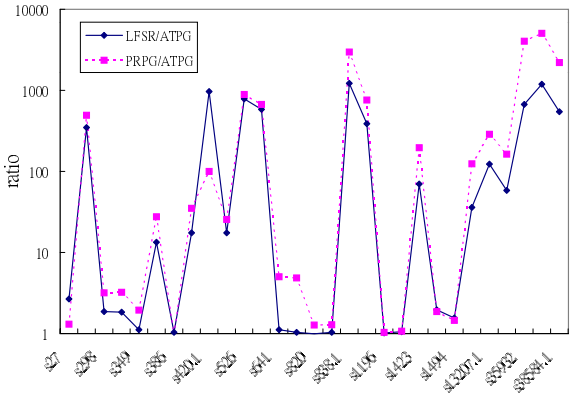

Figure 3. Testability improvement ratios.

LBIST are calculated using our models and are shown in Fig. 4.

When the production volume is low (less than 4M), the overall economics effect is dominated by nonrecurring terms, i.e., labor and time-to-market. For higher N_v values (above 4M), the effect of recurring costs dominates.

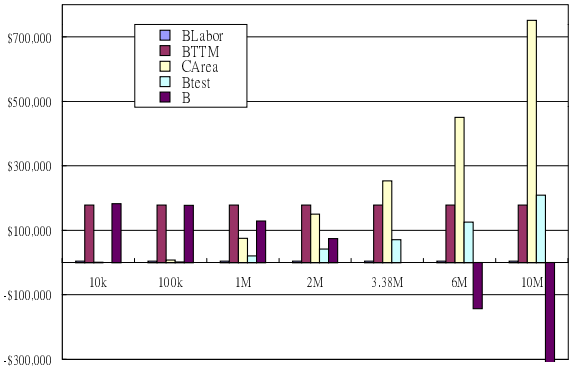

Figure 4. Analysis results of the LBIST case.

6. MBIST Case

We use the design reported in [9] as a case for our MBIST model evaluation. The testing benefit is high due to expensive memory testers and a significant reduction in memory tester time. As a result, MBIST is beneficial for medium- to high-volume products, as shown in Fig. 5.

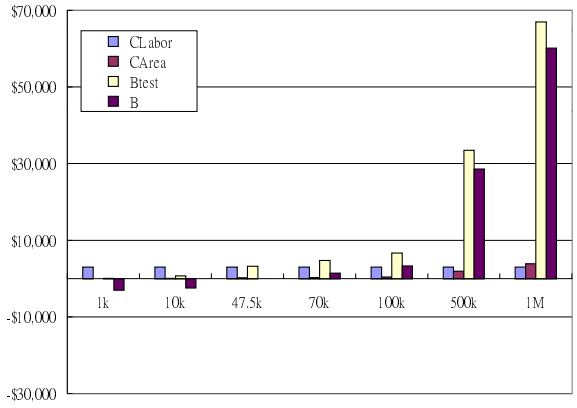

Figure 5. Analysis results of the MBIST case.

7. Conclusions

We have presented cost and benefit models associated with BIST for logic and memory cores, and a novel approach for testability estimation which is used in our models. Two cases have been presented, one for LBIST and the other for MBIST. Experimental results show that LBIST is preferred at lower production volume for the case we use, while MBIST is favorable at higher volume in general. Note that the results shown are for the specific cases we have experimented. Different projects (and manufacturers) may lead to different results and conclusions due to variation in the parameters.

We are currently modifying our Evaluation System for TEst Engineering Methodologies (ESTEEM) to incorporate the BIST related models proposed here. Our system allows user modification of the default models in addition to the parameters, so customization for a specific product line can easily be done.

The system is not meant to accurately predict the profit that a product may bring before it is actually manufactured (or even designed), because it is not possible. Rather, it is an aid for project leaders to allocate DFT budget as early as possible, to increase the possibility of product success. In some cases, however, the decision may not be economic, e.g., due to company policy or the lack of other solutions.

References

[1] P. Varma, A. Ambler, and K. Baker, "An analysis of the economics of self-test," in *Proc. Int. Test Conf. (ITC)*, pp. 20–30, 1984.

[2] B. Davis, *The Economics of Automatic Testing*. London: McGraw-Hill, second ed., 1994.

[3] C. Dislis, J. H. Dick, I. D. Dear, and A. P. Ambler, *Test Economics and Design for Testability for Electronic Circuits and Systems*. Hemel Hempstead: Ellis Horwood, 1995.

[4] J. M. Miranda, "A BIST and boundary-scan economics framework," *IEEE Design & Test of Computers*, vol. 14, pp. 17–23, July-Sept. 1997.

[5] C.-W. Wu and C.-C. Wei, "The economic models for a VLSI test strategy planning system," in *Proc. SEMICON Taiwan 97, Test Seminar*, (Taipei), pp. 87–92, Sept. 1997.

[6] J.-D. Lin, J.-M. Lu, and C.-W. Wu, "An improved VLSI test economics analysis system," in *Proc. 9th VLSI Design/CAD Symp.*, (Nantou), pp. 149–152, Aug. 1998.

[7] P. H. Bardell, W. H. McAnney, and J. Savir, *Built-In Test for VLSI*. New York: John Wiley & Sons, 1987.

[8] A. J. van de Goor, *Testing Semiconductor Memories: Theory and Practice*. Chichester, England: John Wiley & Sons, 1991.

[9] C.-T. Huang, J.-R. Huang, C.-F. Wu, C.-W. Wu, and T.-Y. Chang, "A programmable BIST core for embedded DRAM," *IEEE Design & Test of Computers*, vol. 16, pp. 59–70, Jan.-Mar. 1999.

[10] S. Wei, P. K. Nag, R. D. Blanton, A. Gattiker, and W. Maly, "To DFT or not to DFT?," in *Proc. Int. Test Conf. (ITC)*, 1997.

[11] V. K. Kim, M. Tegethoff, and T. Chen, "ASIC yield estimation at early design cycle," in *Proc. Int. Test Conf. (ITC)*, pp. 590–594, 1996.

[12] J.-D. Lin, "An improved VLSI test economics analysis system," master thesis, Department of Electrical Engineerig, National Tsing Hua University, Hsinchu, Taiwan, June 1998.

[13] F. Brglez, D. Bryan, and K. Koźmiński, "Combinational profiles of sequential benchmark circuits," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, pp. 1929–1934, 1989.

[14] C.-H. Tsai, "IEEE Std 1149.5 MTM-Bus Slave module chip design and its application to hierarchical system test," master thesis, Department of Electrical Engineerig, National Tsing Hua University, Hsinchu, Taiwan, June 1996.