

Gate-All-Around Si Nanowire Transistors (SNWTs) for Extreme Scaling: Fabrication, Characterization and Analysis

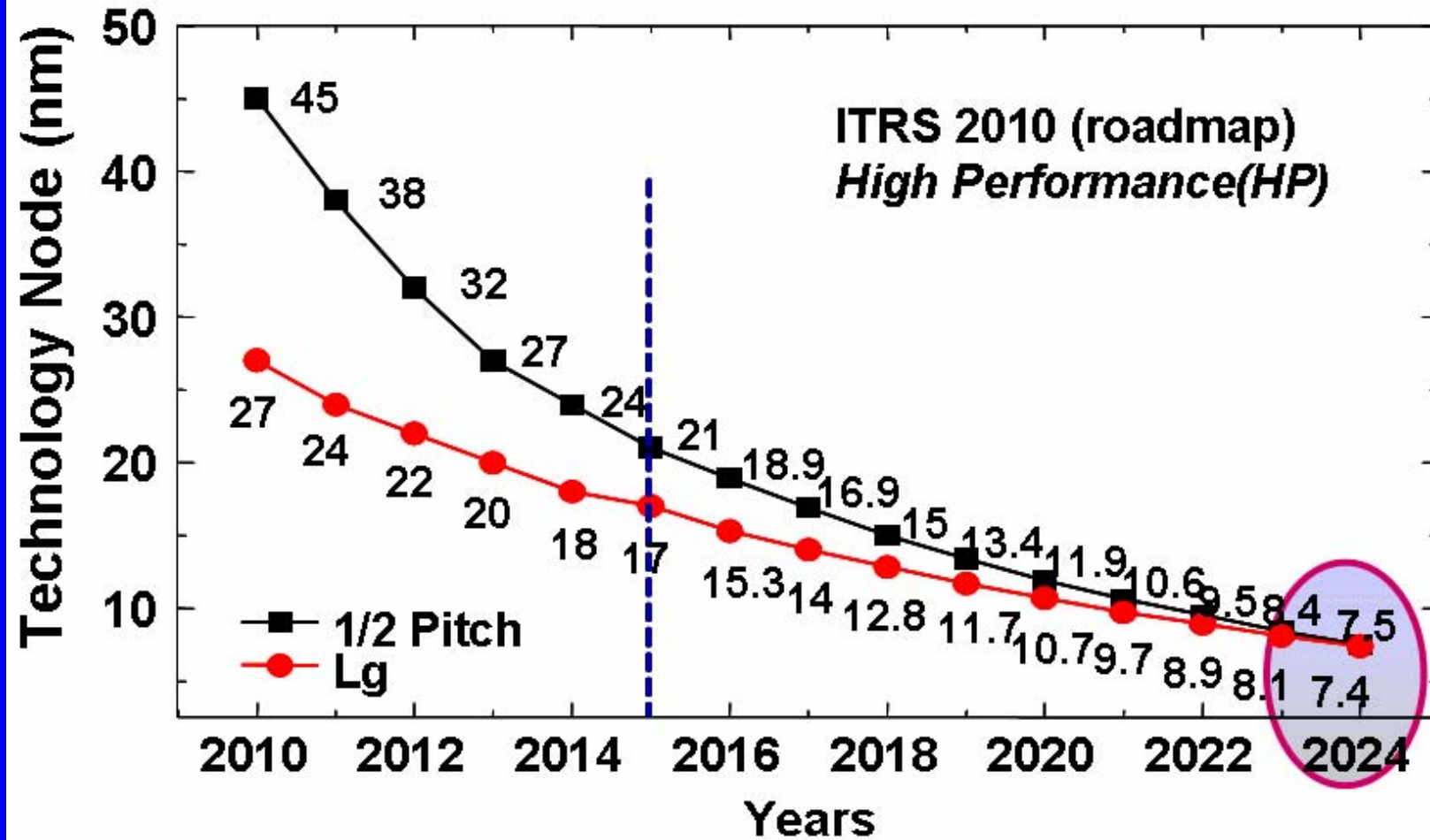
Ru Huang
Peking University (PKU)
Beijing 100871, China



Outline

- **Introduction**
- **Fabrication and integration**
- **Recent advances in understanding SNWTs**
 - **Parasitic effects**
 - **Self-heating effects**
 - **Variability**
- **Recent nanowire circuit demonstrations**
- **Summary**

Introduction - 1/5

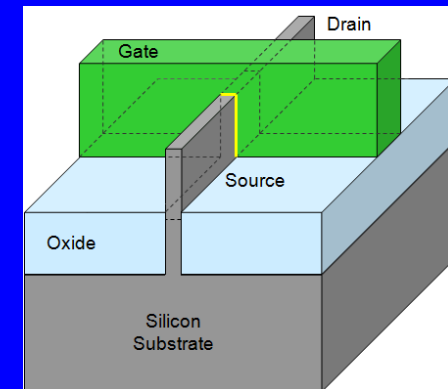
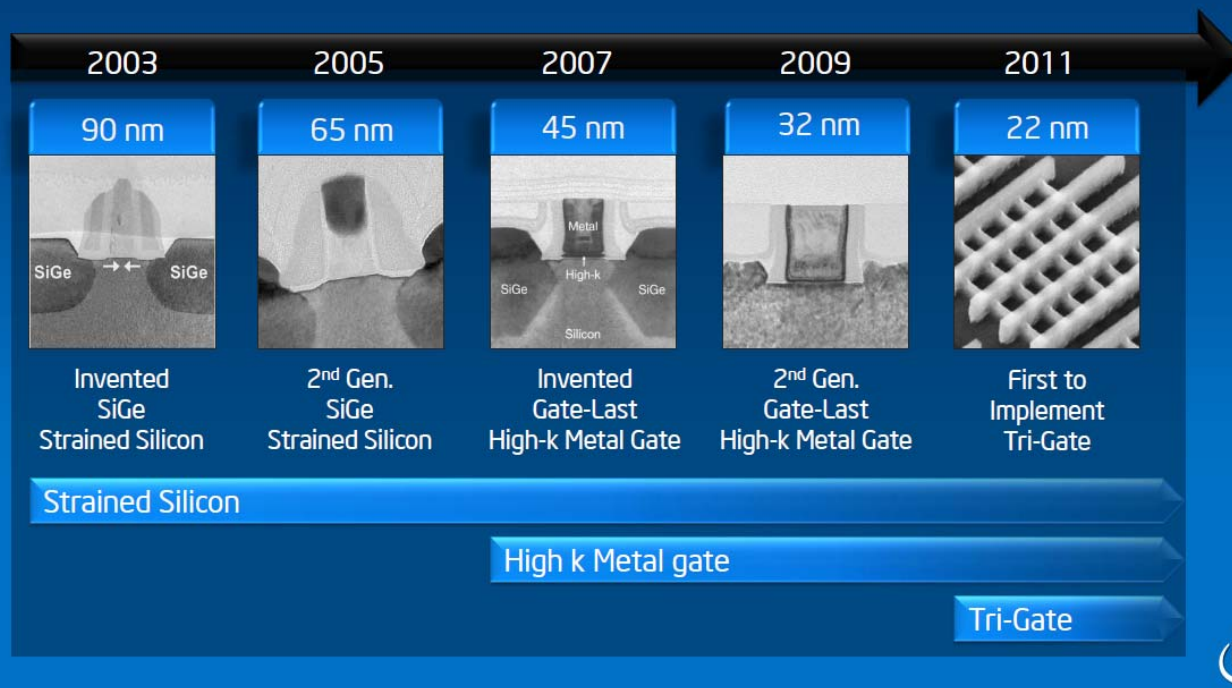


Introduction - 2/5

We are entering the multi-gate era!

- Intel's 22nm is Tri-gate transistor

Transistor Innovations Enable Technology Cadence

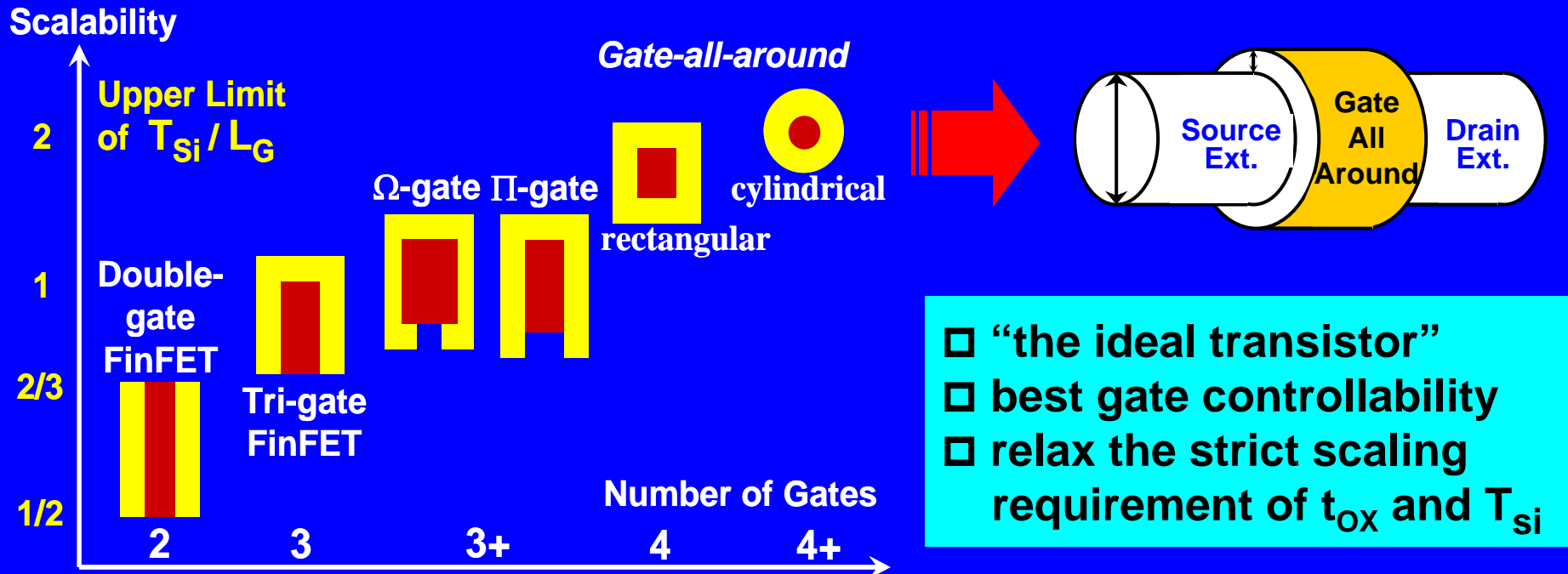


- ***What's next?***

Source: M. Bohr and K. Mistry, <http://www.intel.com>

Introduction - 3/5

Next: *Gate-all-around Nanowire Transistor*



FinFET/Tri-gate
Fin
Channels

Extreme
Scaling

Gate-all-around
Nanowire
Channels

Introduction - 4/5

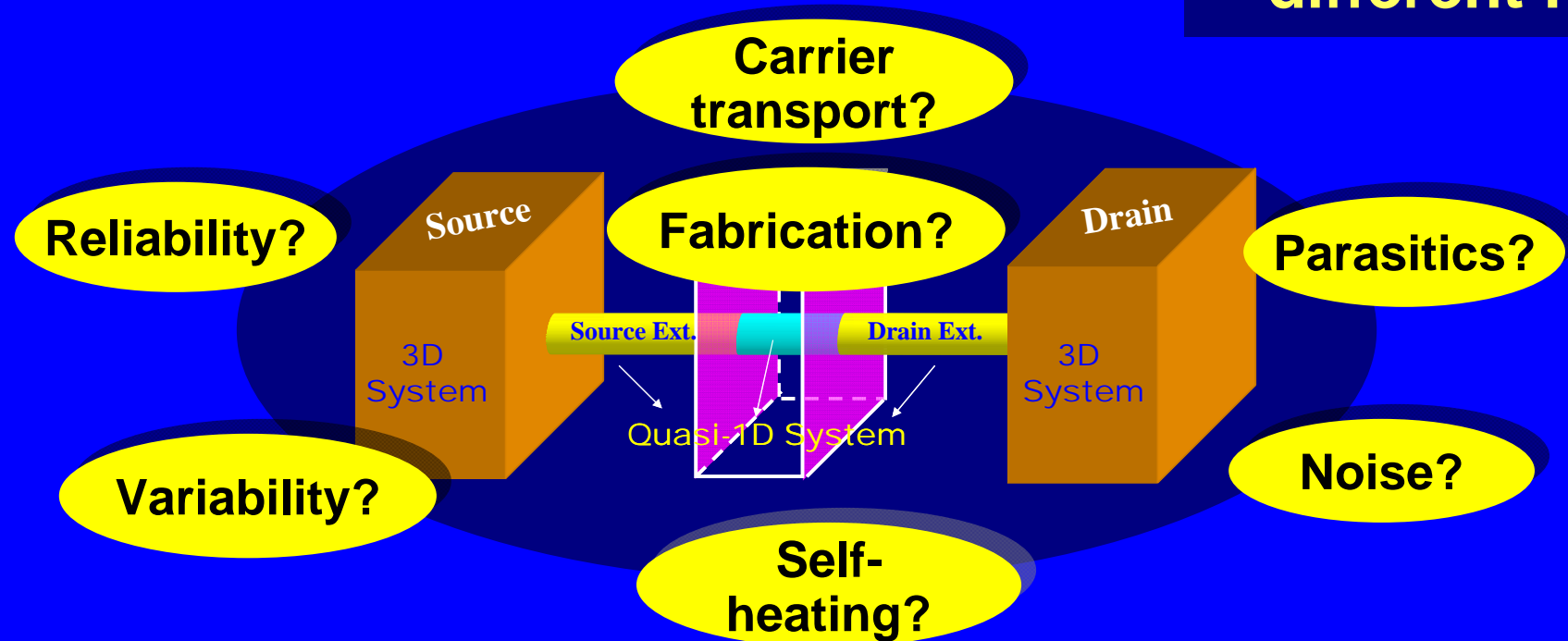
How to fabricate this device?

Did we know all about this kind of device?

- We already have the scaling theory for Tri-gate and GAA
- But, one cannot simply scale GAA properties to get correct understanding of Si nanowire transistor

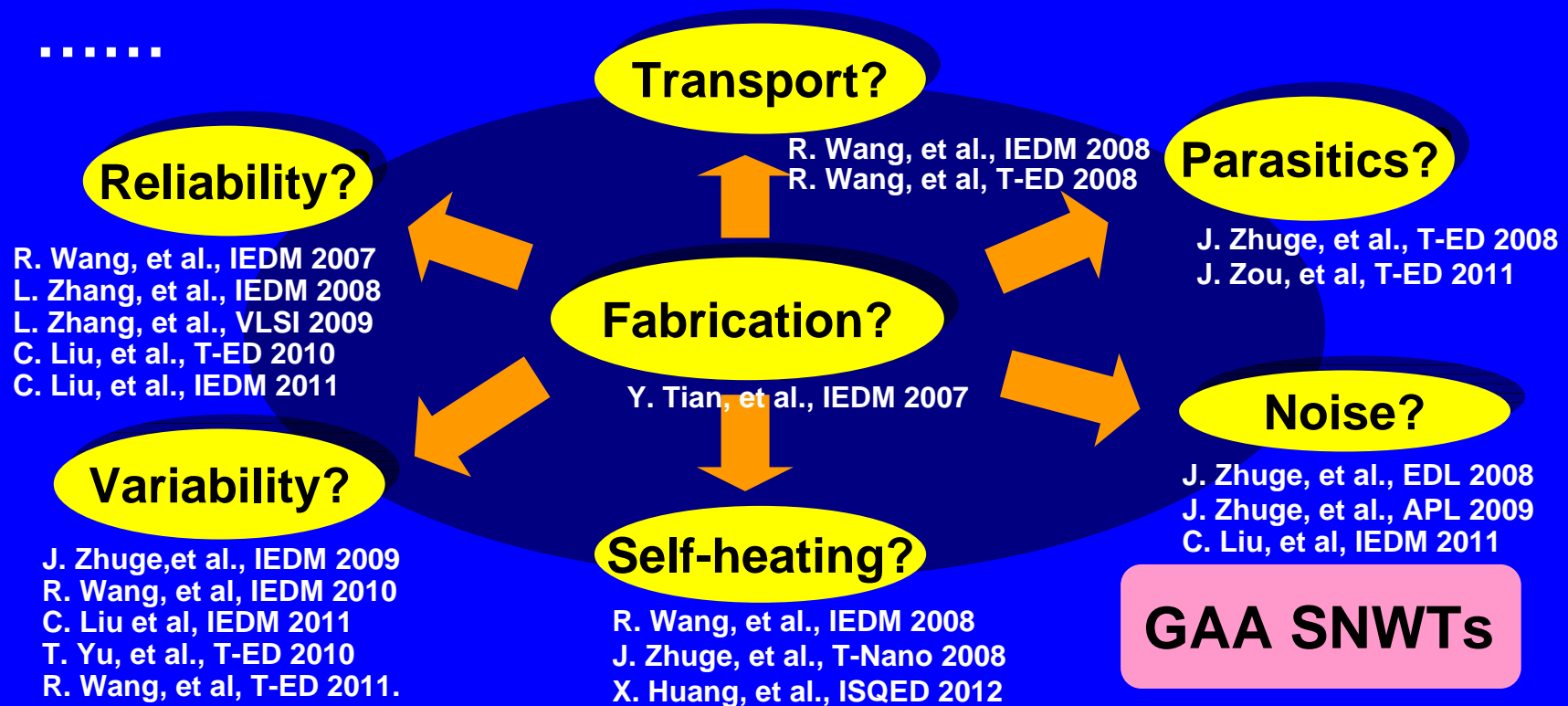
Strongly-confined quasi-1D structure

fundamentally different !



Introduction - 5/5

- ✓ Fabricate this device from top-down approach
- ✓ Evaluate the key device characteristics for circuit applications with confined quasi-1D structure
- clarify the related physics
- find the challenges for optimization
- new characterizing techniques
-

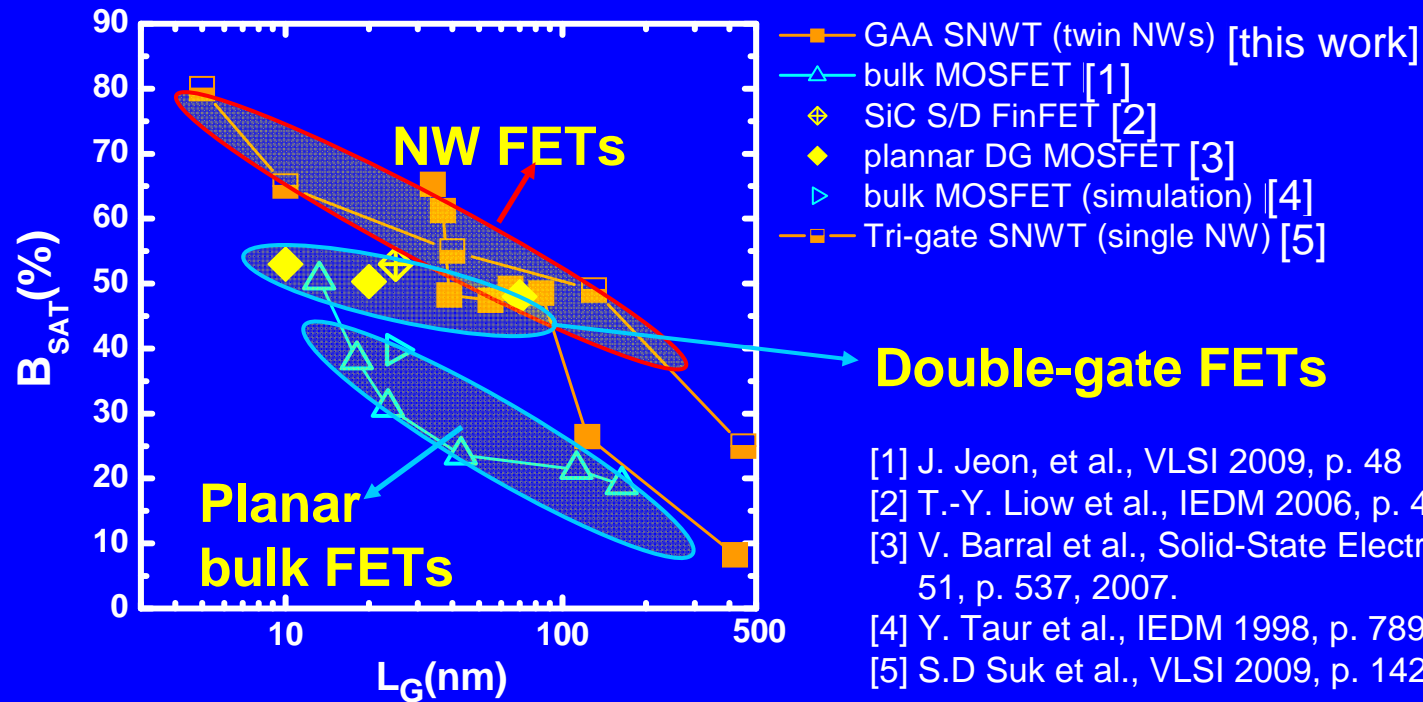


Key Messages: *Preview*

- Fabrication and integration: *almost Manufacturable*
- Recent advances in understanding SNWTs
 - Intrinsic carrier transport: *near-ballistic transport*

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- Better B_{SAT} than planar and double-gate devices

Key Messages: *Preview*

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- Recent advances in understanding SNWTs
 - Intrinsic carrier transport: *near-ballistic transport*
 - Low-frequency noise: *slightly degraded and fluctuated*
 - Parasitic effects (R and C): *should be optimized*
 - Self-heating effects: *observable when $d_{NW} < 14\text{nm}$*
 - Variability: *holds the record low (static) variations*
 - Reliability: *HCI is OK, but NBTI needs more studies*
- Recent nanowire circuit demonstrations: *On the way*
 - *SRAM, ring oscillator, current mirror...*
- *Other benefits for 3D integration, MtM applications...*
- Summary: ***We are facing a great opportunity!***

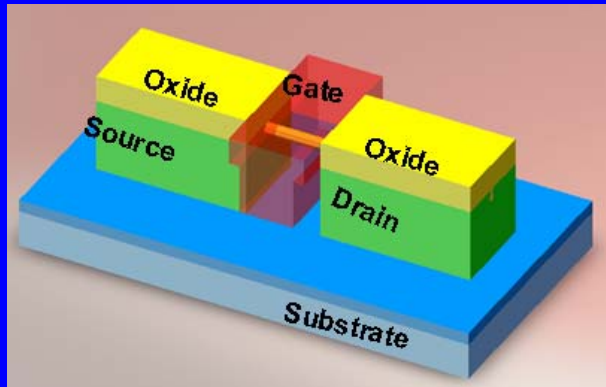
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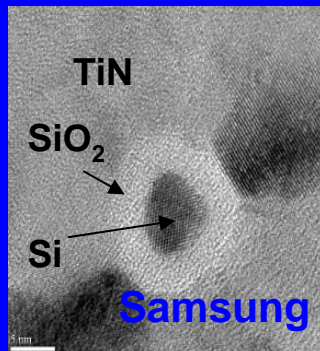
Outline

- Introduction
- **Fabrication and integration**
 - based on bulk (our focus)
 - based on SOI
 - with stacked NW channel
- Recent advances in understanding SNWTs
 - Parasitic effects
 - Self-heating effects
 - Variability
- Recent nanowire circuit demonstrations
- Summary

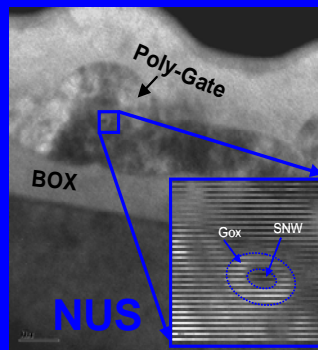
Top-down process for SNWTs



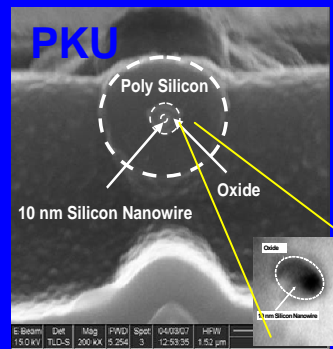
- Key points
 - NW formation
 - NW releasing or suspending



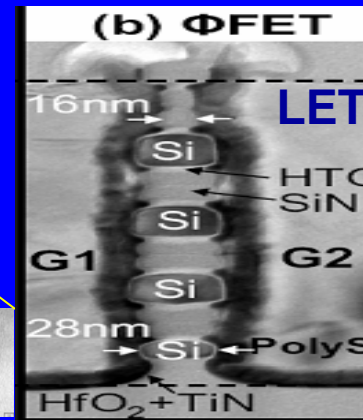
IEDM, 2005
Samsung



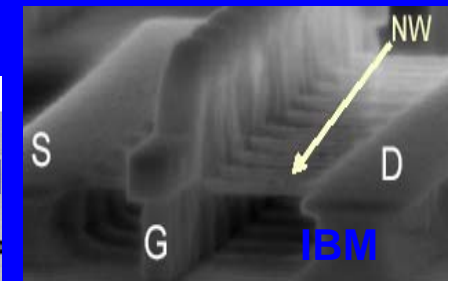
IEDM, 2006
NUS



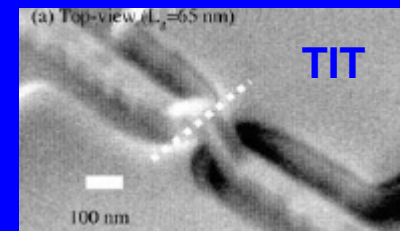
IEDM, 2007
PKU



C. Dupré et al.,
IEDM, 2008
LETI

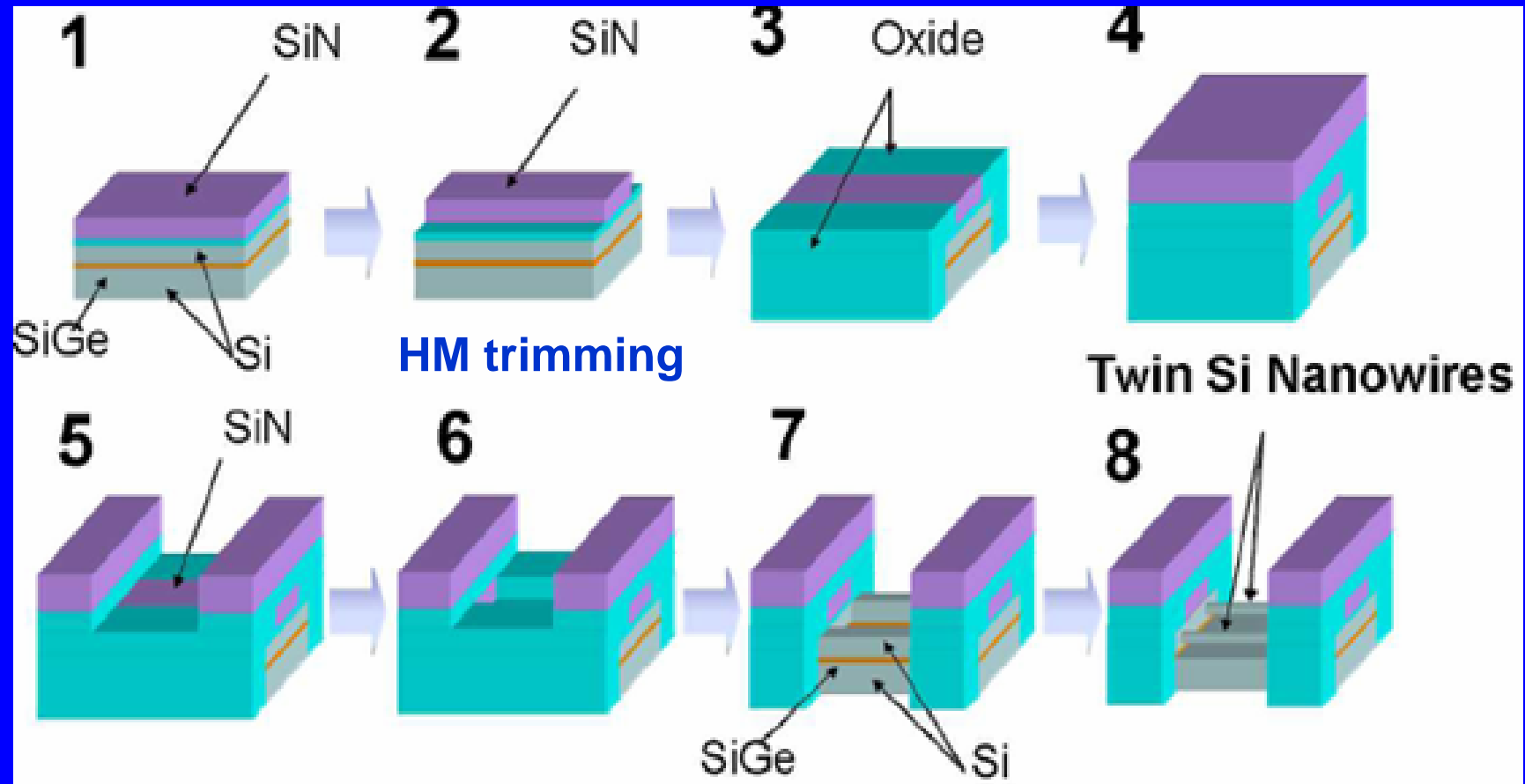


S. Bangsaruntip
et al., IEDM, 2009
IBM



Sato S, et al., SSE,
2010, TIT

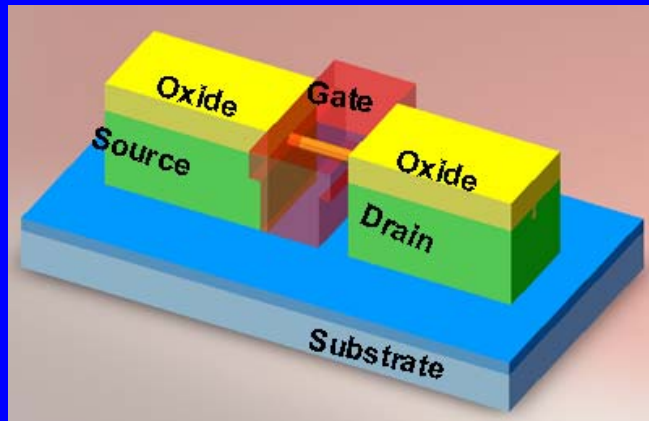
Bulk SNWTs - Samsung method



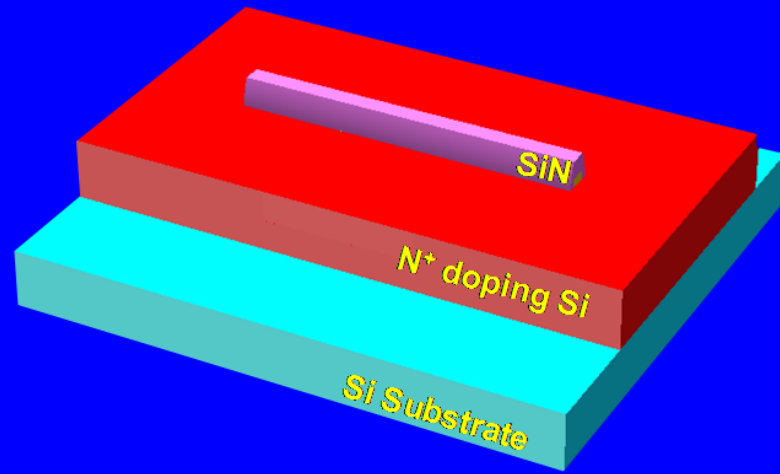
- ✓ HM Trimming for NW definition
- ✓ SiGe/Si stack epi for releasing

diameter = 10nm
 $t_{ox}=3.5nm$
TiN metal-gate

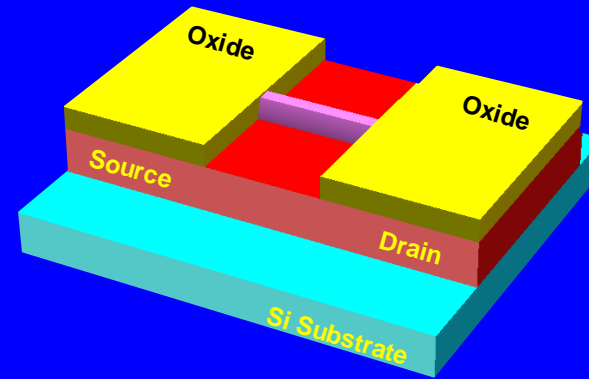
Self-aligned bulk SNWTs by epi-free compatible process



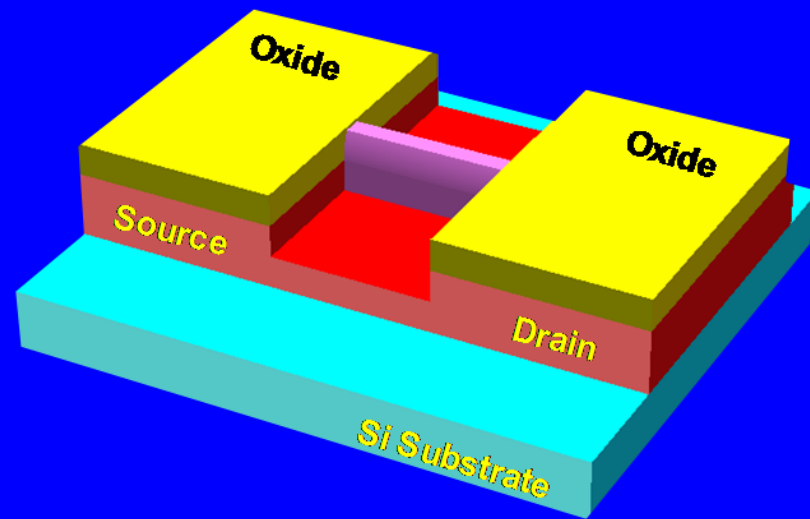
- ✓ based on bulk substrate
- ✓ NW originally defined by e-beam, thinning and cylinder channel shaping by self-limiting oxidation and annealing
- ✓ NW released by isotropic etch with HM



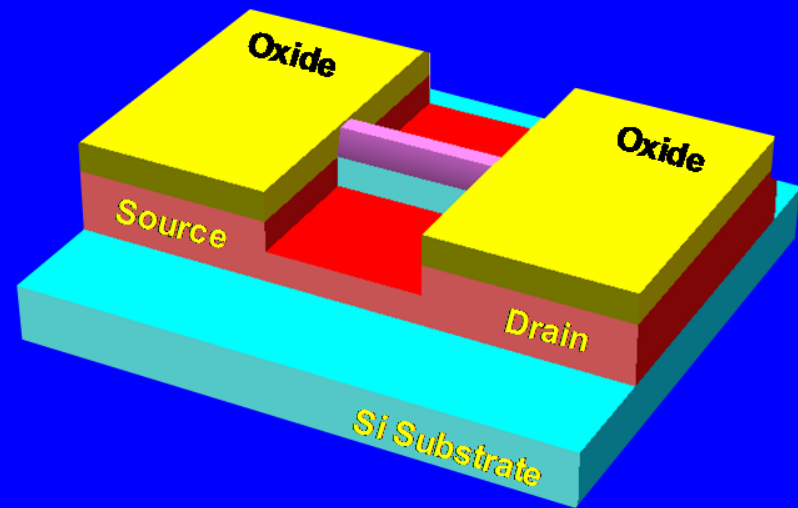
Nitride fin patterning & S/D implantation



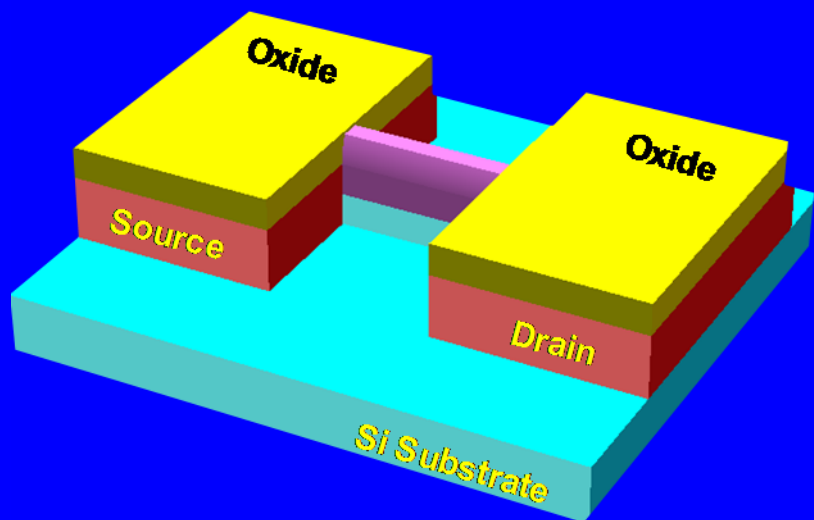
Gate trench etching after oxide deposition



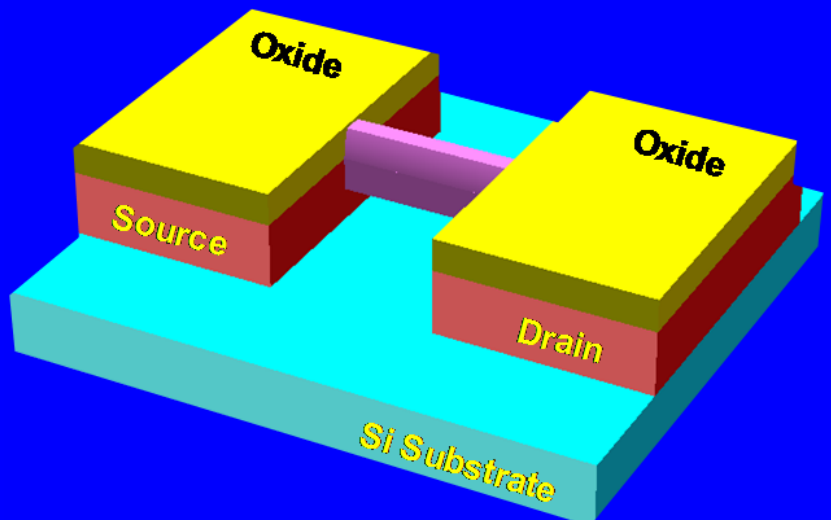
Nitride spacer formation



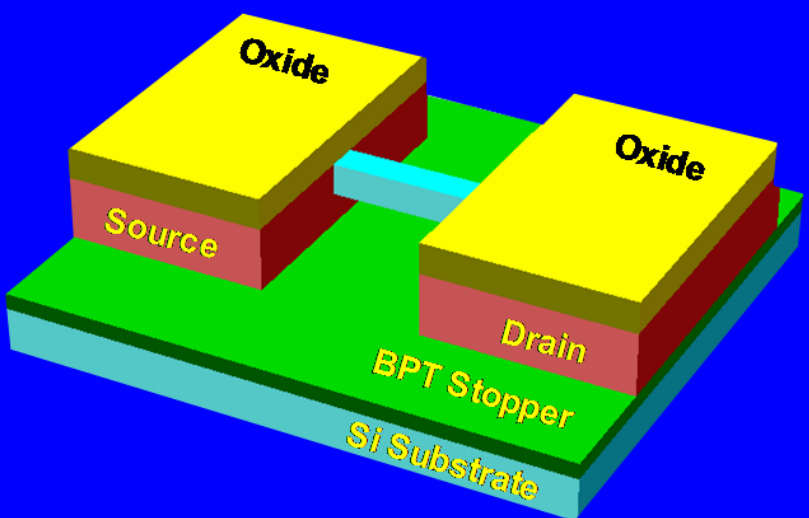
Silicon fin etching



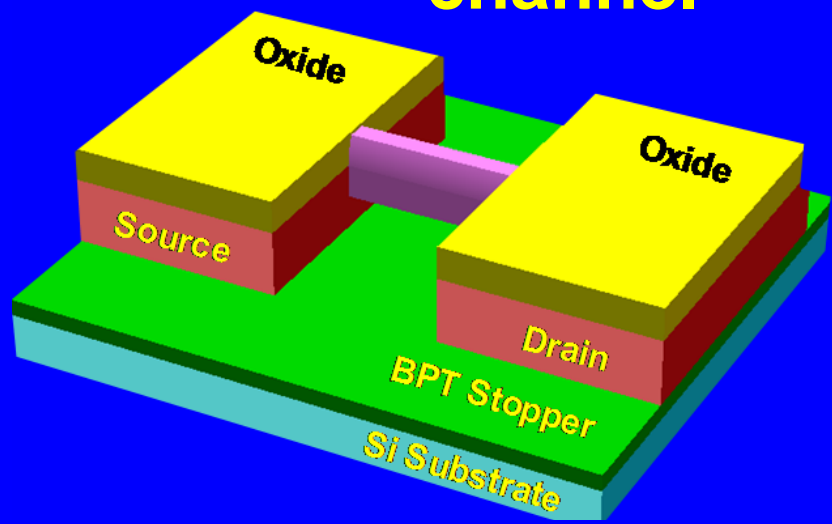
Silicon etching surrounding fin channel



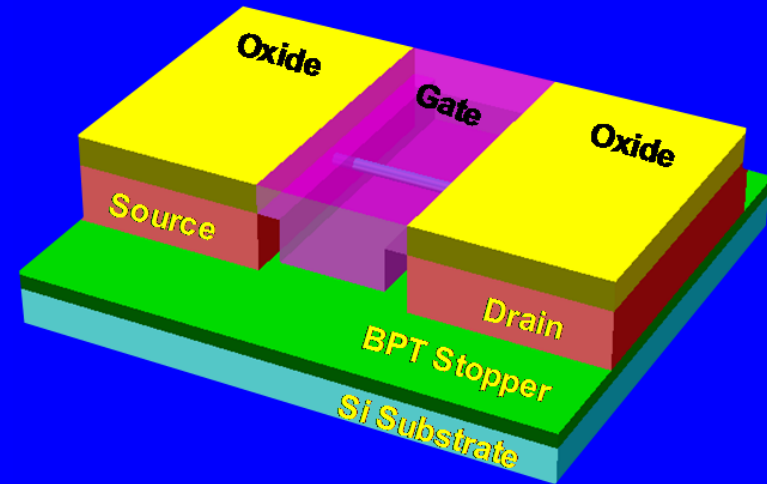
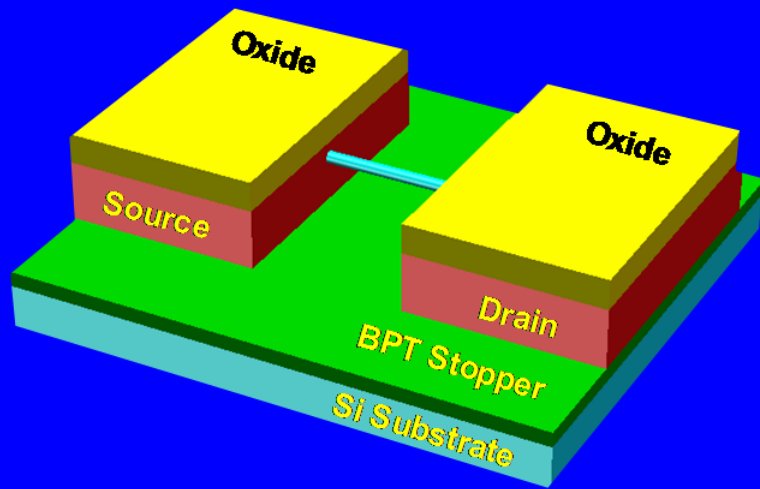
Si etching under channel



Hard mask removal



BPT (bottom parasitic transistor) Stopper layer



Cylindrical shaping

Gate oxidation & Poly-Si gate formation

- diameter = 10nm
- $t_{ox}=5nm$
- Poly gate

NW formation

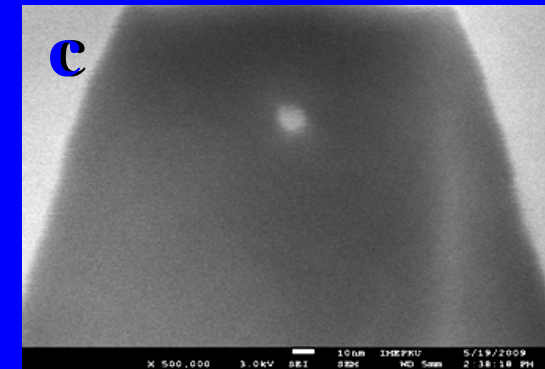
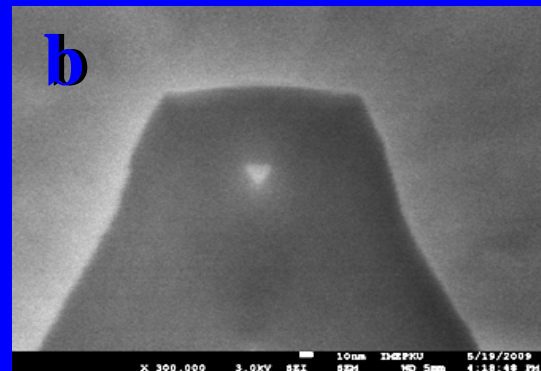
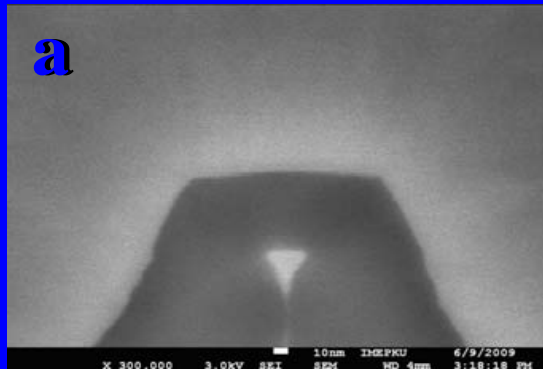
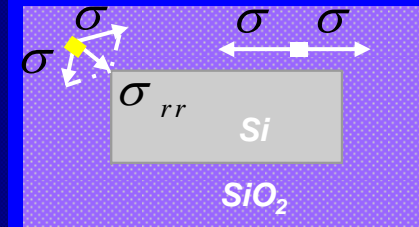
NW shaping and diameter controlling

Patterning for original channel



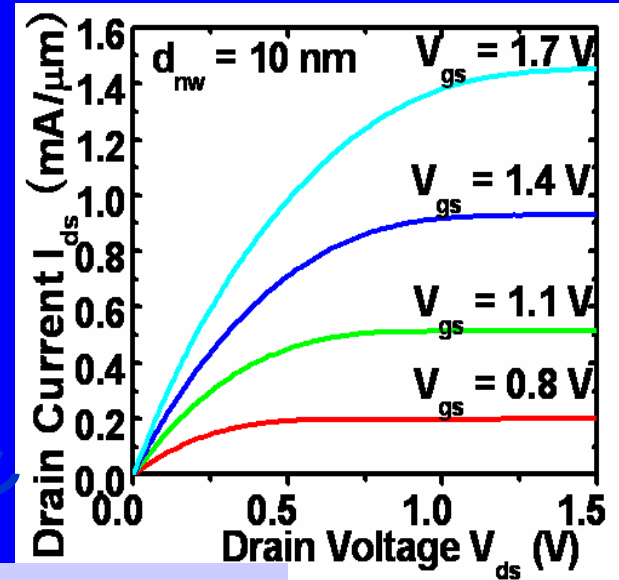
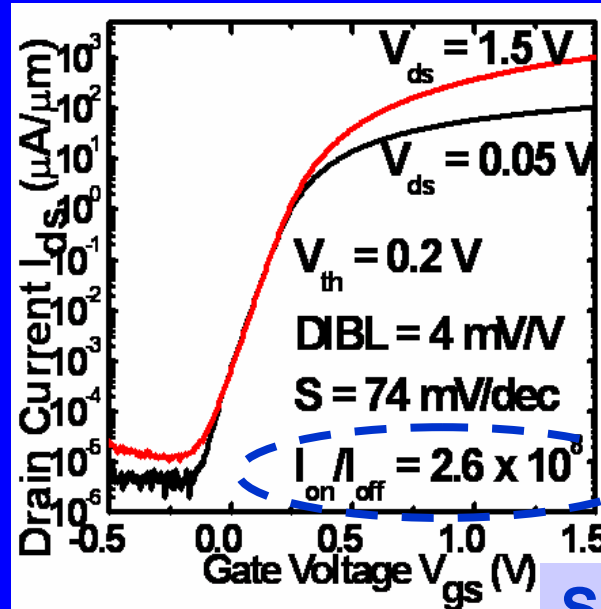
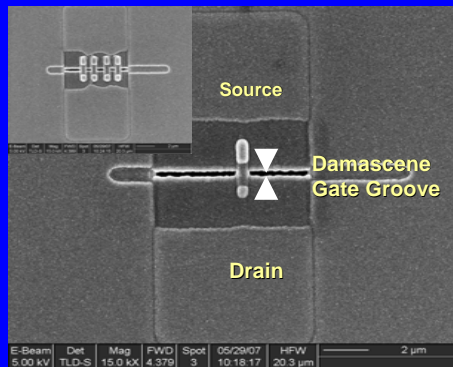
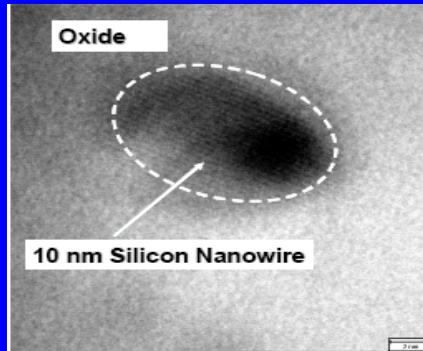
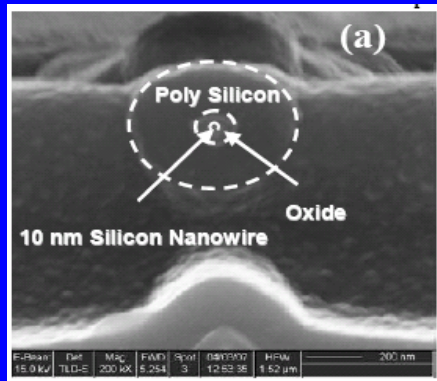
Oxidation (Temperature & time)

Traded with Oxidation retardation effect

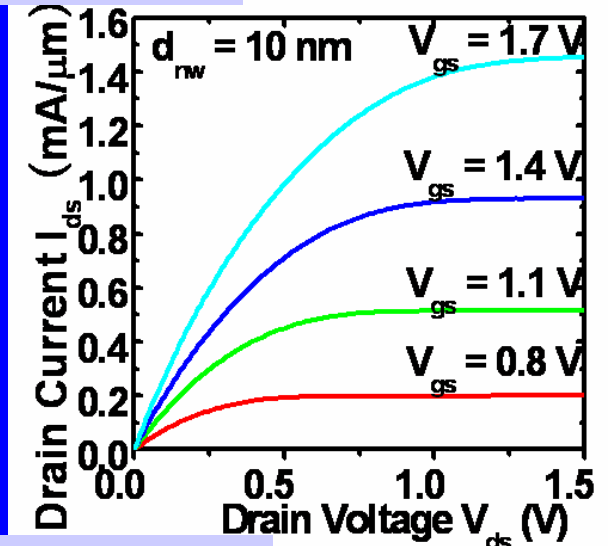
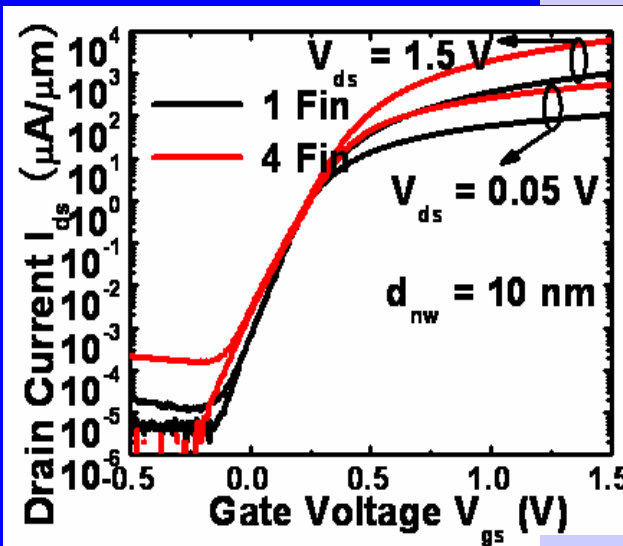


Increasing oxidation time: from triangle to circle

Experimental results of NWFETs



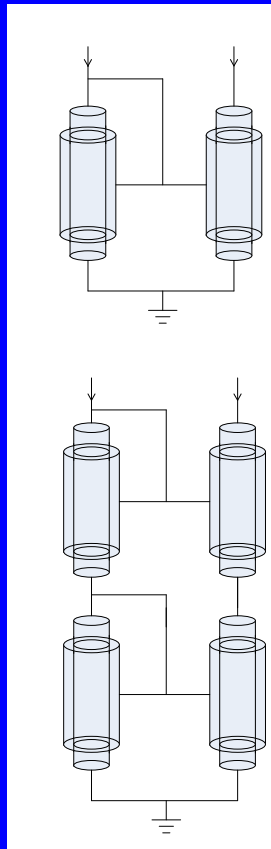
Single wire



Multiple wire

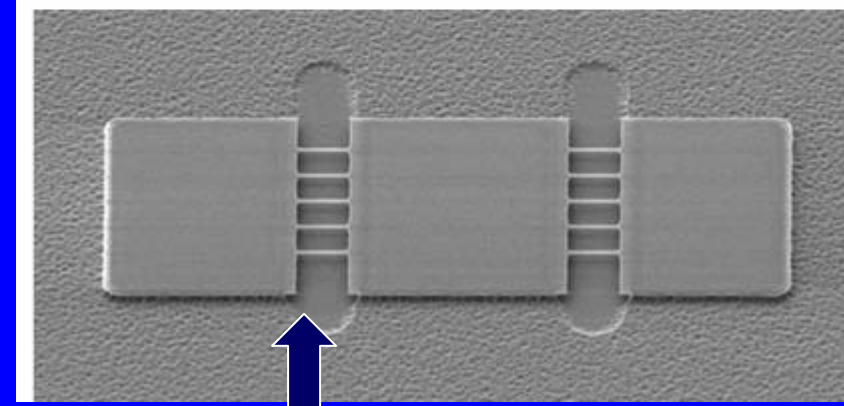
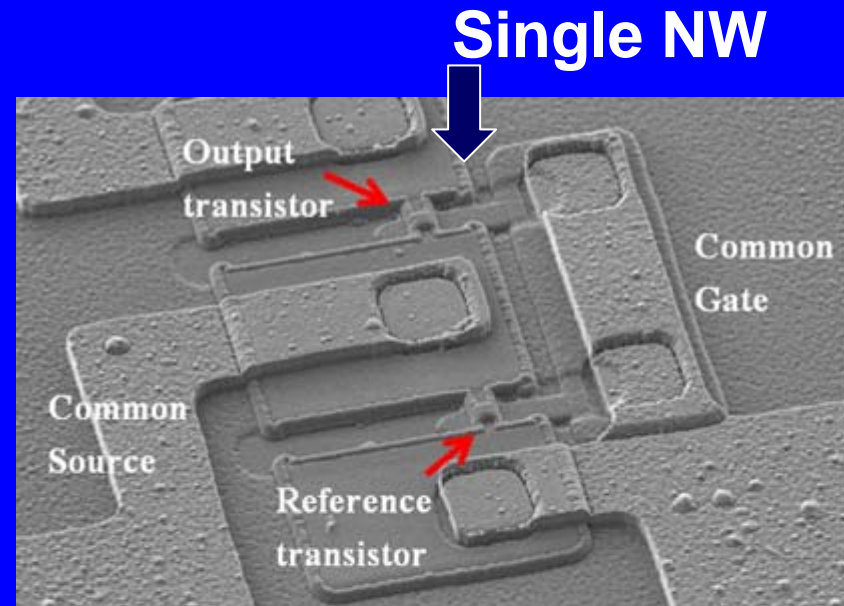
Y. Tian *et al.*, IEDM, 2007, PKU

Current mirror (CM) based on SNWTs



2T CM

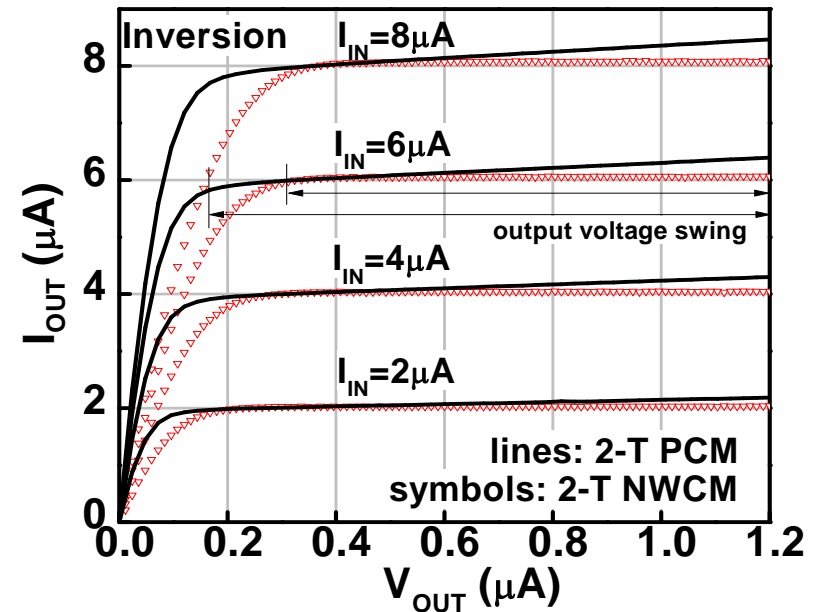
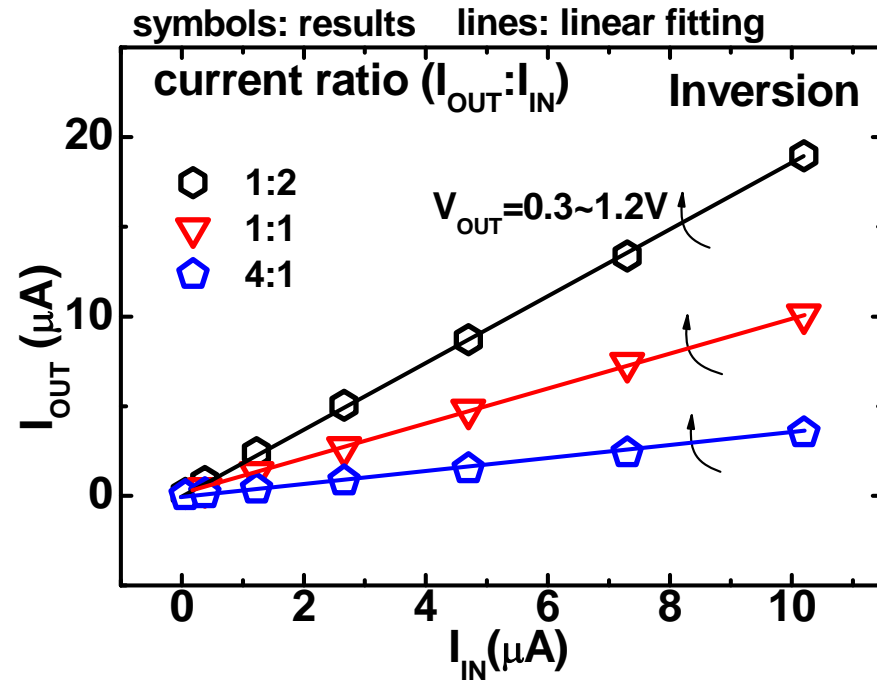
cascade CM



Multi NW
adjust current ratio
with NW number

R.Huang et al., T-ED, 2011, PI

Testing results

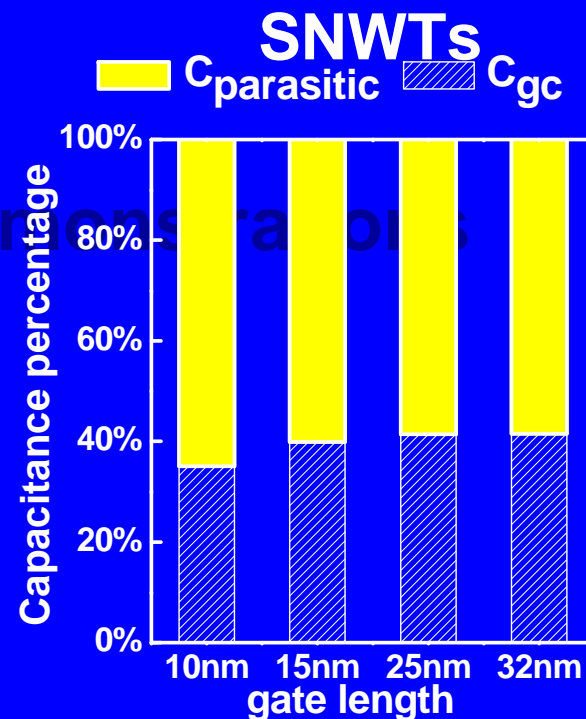


$$OVC(\%)=100(\Delta I_{OUT}/I_{OUT})/\Delta V_{OUT}$$

OVC	NW CM	Planar CM
2T	~ 0.2%	~5.7%
cascade	~0.05%	~1%

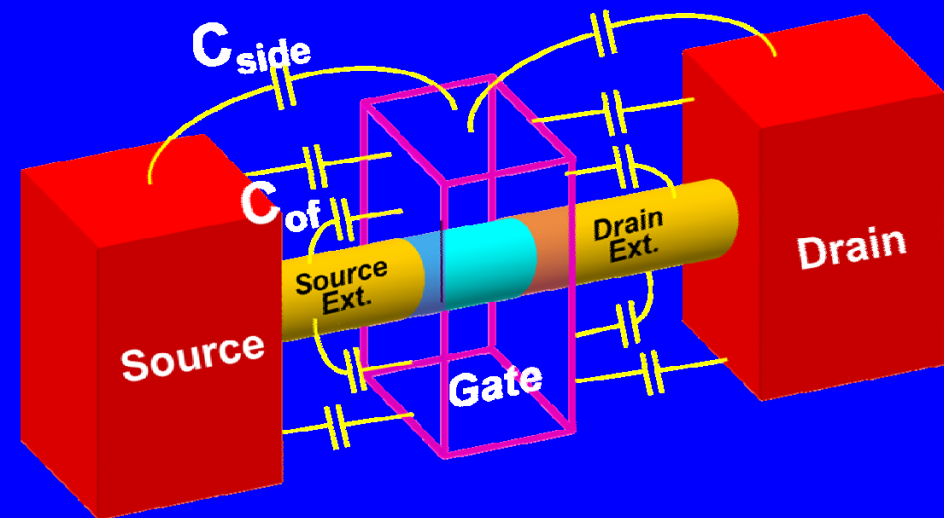
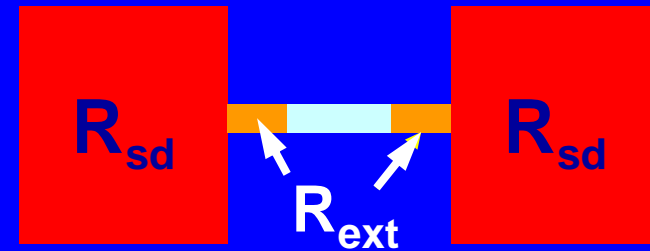
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 - Parasitic effects (R_{par} and C_{par})
 - dominant factors in R_{par} and C_{par}
 - Self-heating effects
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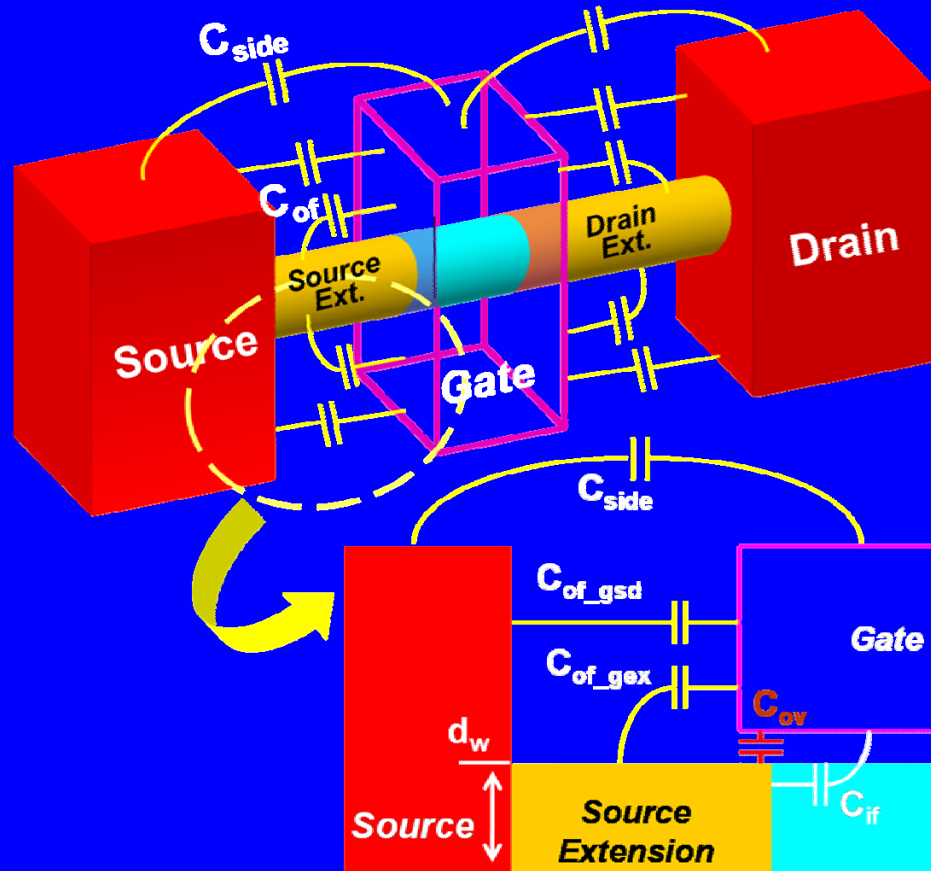


Parasitic R and C in GAA SNWTs

- SNWT is worse than planar devices and FinFETs
 - larger and dominant **SDE series resistances**
 - larger **outer fringing capacitances**



Parasitic capacitances in SNWTs



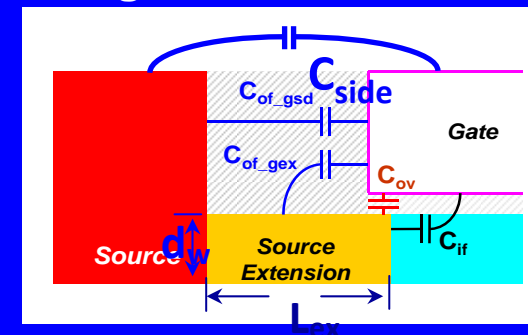
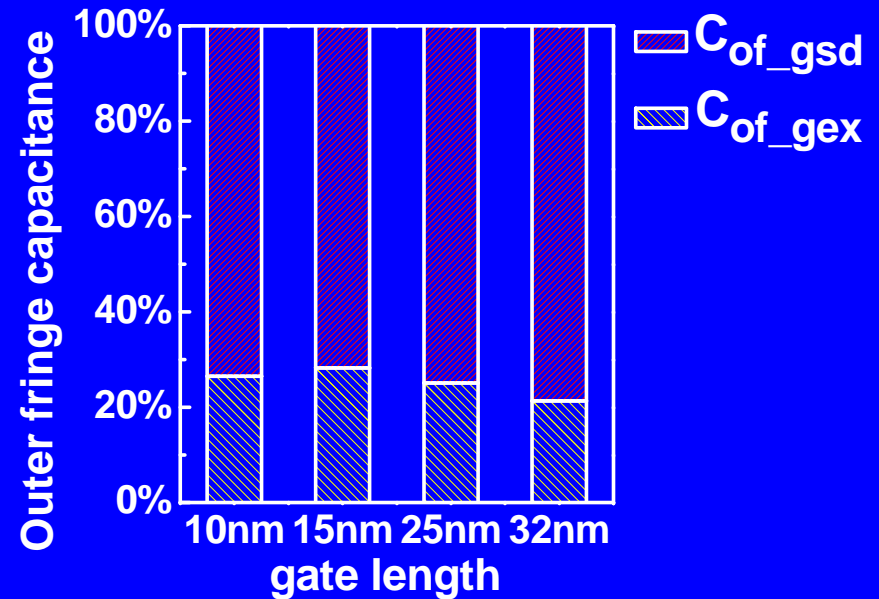
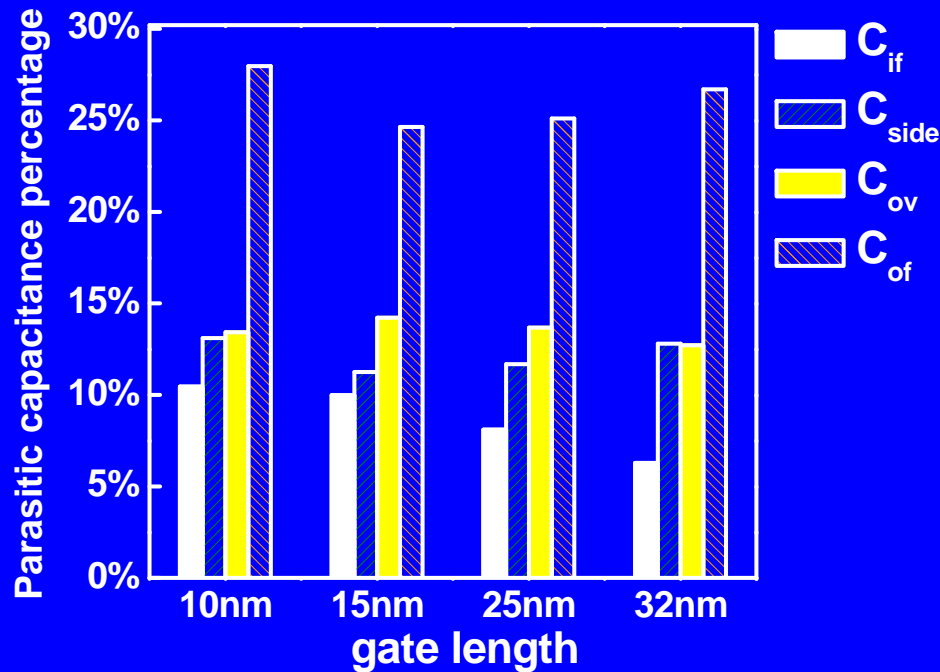
$$C_{parasitic} = C_{of} + C_{if} + C_{ov} + C_{side}$$

$$C_{of} = C_{of_gsd} + C_{of_gex}$$

- A predictive model for parasitic C in SNWTs has been developed*

Impacts of parasitic C -1/2

- Outer fringe capacitance C_{of} is dominant
 - C_{of_gsd} is the main contributor

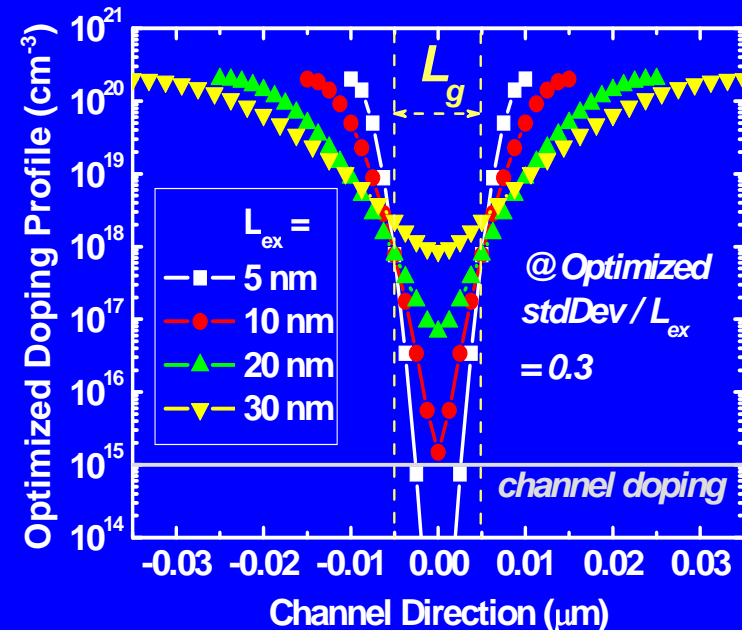


J. Zhuge et al., T-ED 2008, p. 2142; PKU

Jibin Zou et al., IEEE T-ED, vol. 58, no. 10, Oct. 2011. PKU

Key messages for design optimization of parasitics in SNWTs

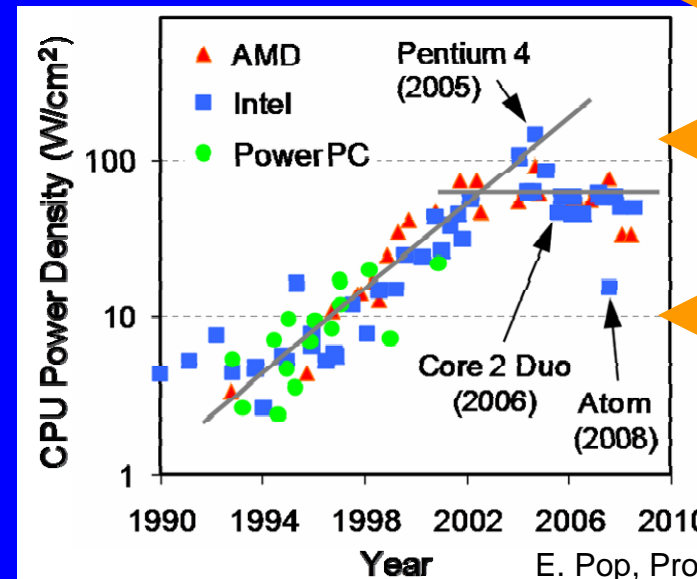
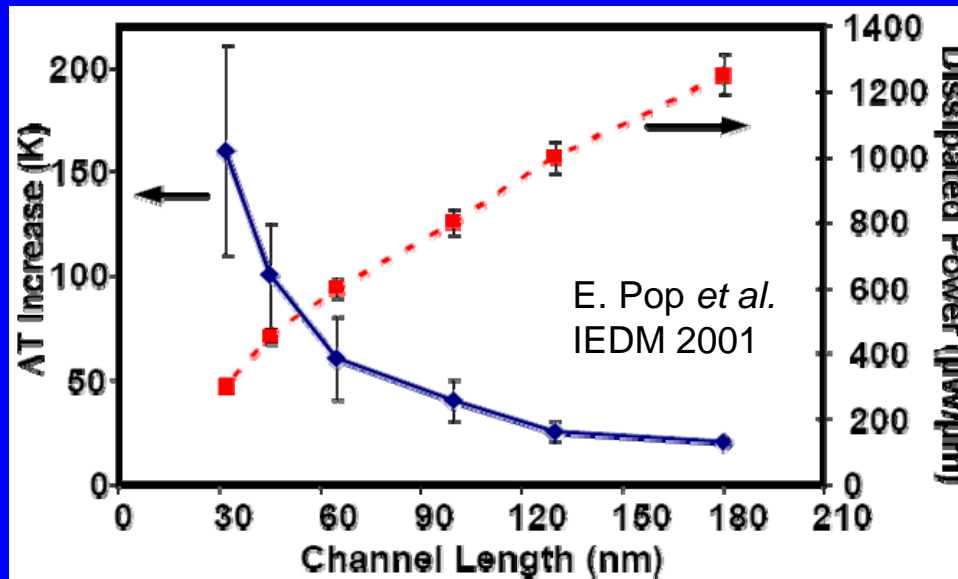
- multi-wire structure is needed
 - with merged SDE structure
- gate height need to be reduced
- Optimizations in SDE regions
 - different from DG FinFETs
 - FinFETs: underlap is better
 - SNWTs: overlap is better
 - ✓ due to better gate control capability in SNWTs
 - ✓ can effectively reduce R_{ext} but with smaller impact on $C_{parasitic}$



Outline

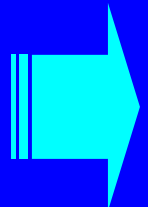
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 - **Self-heating effects (SHE)**
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Transistor thermal challenges at nanoscale -1/2



Rocket Nozzle
Nuclear Reactor
Hot Plate

Increasing self-heating with size shrinking

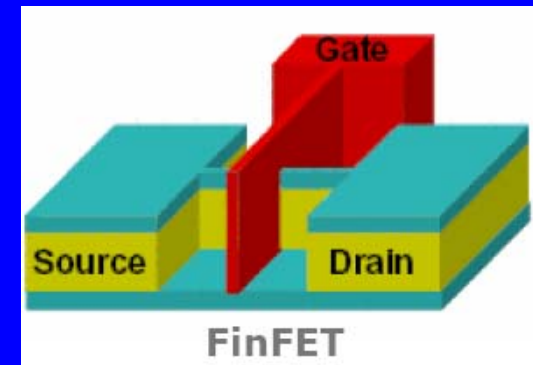
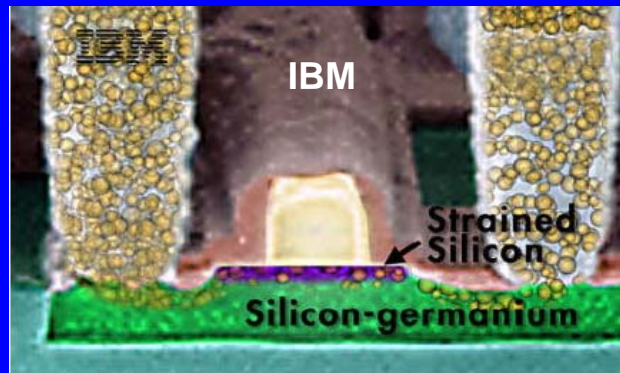


- Headache for analog circuits
- mismatch issue due to thermal distribution
- Reliability: NBTI ...
- Thermal noise
-

Transistor thermal challenges at nanoscale -2/2

Worse SHE for scaled technology: Confined geometries (thin Si films in UTB, DG...) and novel materials (SiGe, Ge, silicide...) with poor thermal conductivity

Material	k_{th} (W/mK)
Si	148
Ge	60
Silicides	40
Si (10 nm)	13
SiO ₂	1.4

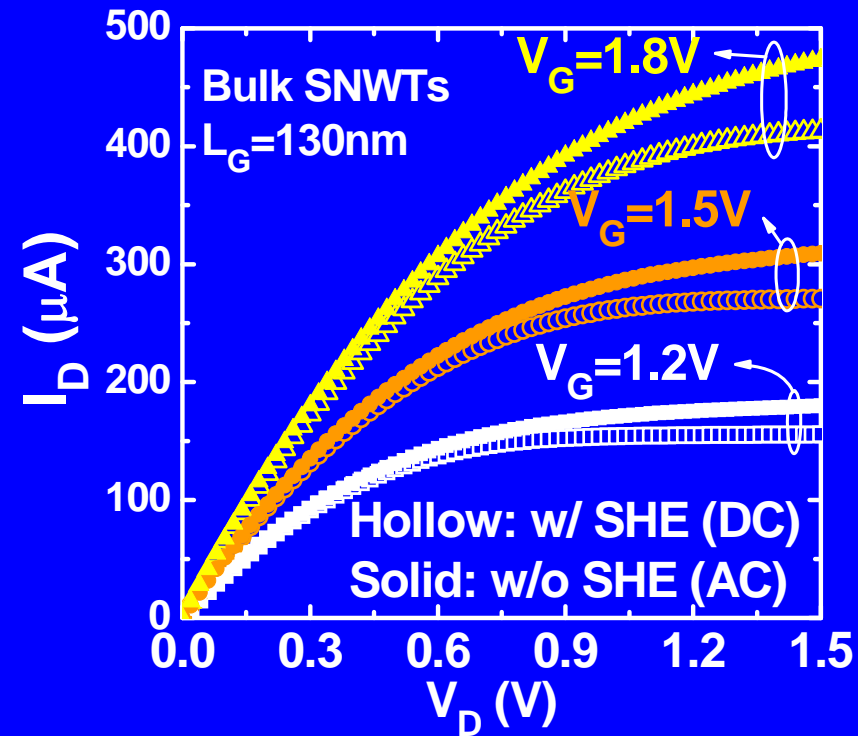


E. Pop, *Proc. IEEE* 2006

- **SNWTs: more confined structure**
So, how about the self-heating?

SHE Characterization of SNWTs

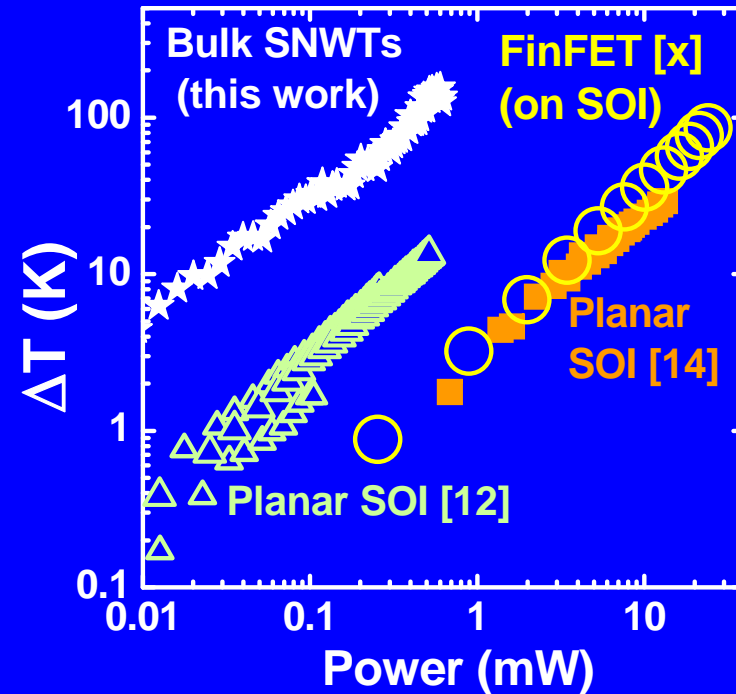
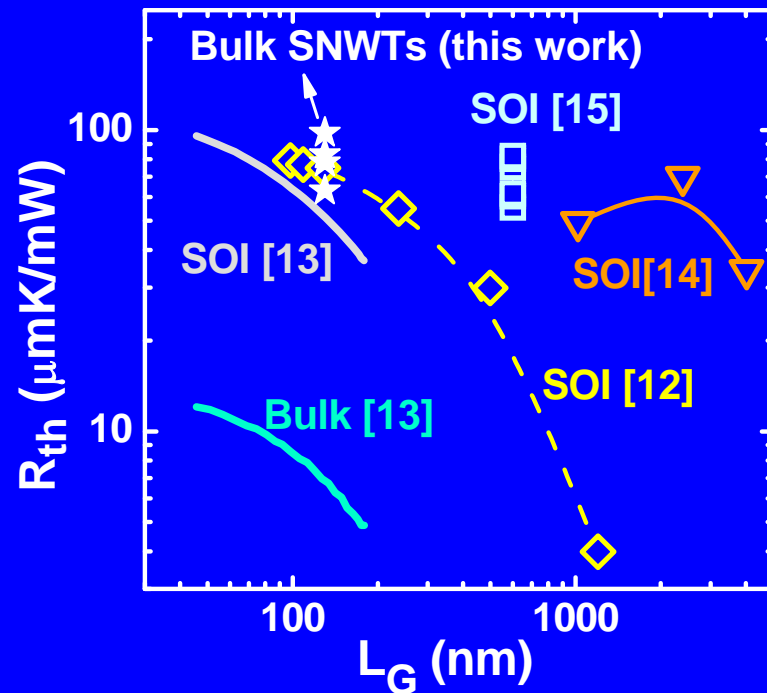
- AC conductance method



**SNWTs on fully bulk substrate
(w/o e-SiGe S/D or SOI)**

R. Wang, et al., IEDM 2008, PKU

Comparisons

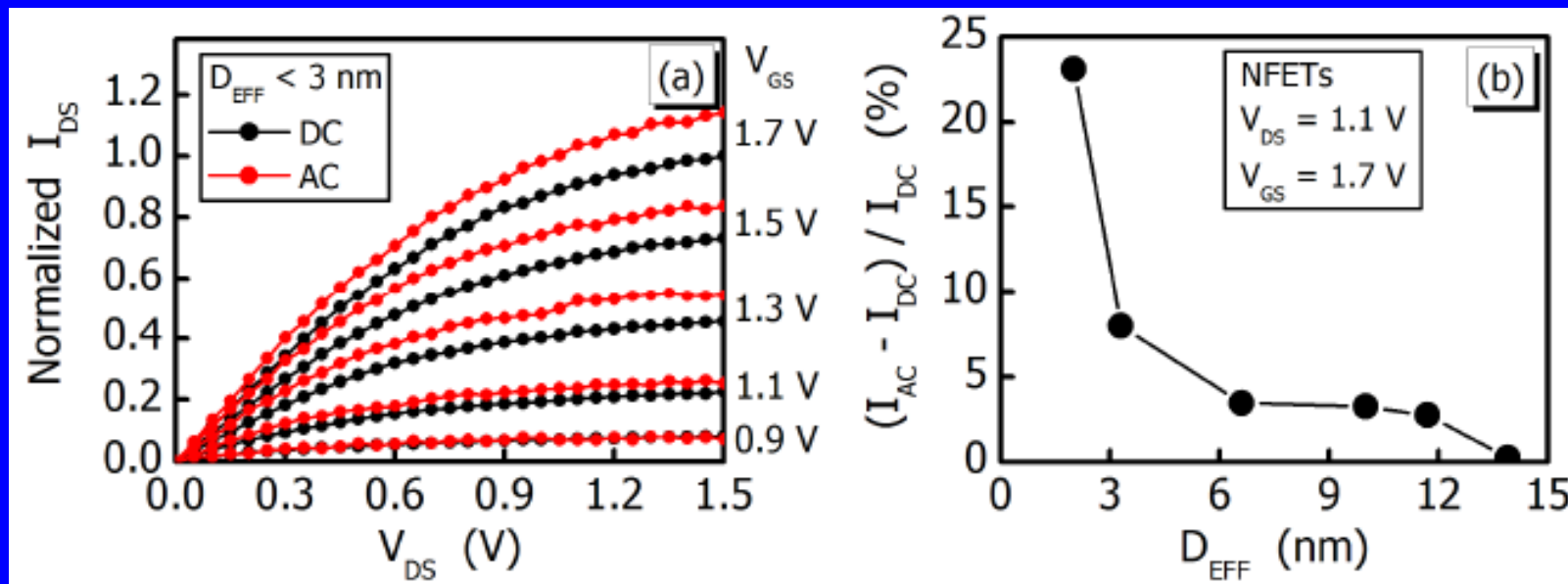


- SHE in SNWTs **even on bulk-Si substrate** is a little bit worse than SOI devices

[12] G. Guegan et al., *Mater. Res. Soc. Symp. Proc.*, 2006; [13] K. Etesam-Yazdani et al., *ITHERM*, 2006; [14] B. M. Tenbroek et al., *IEEE TED*, 1996; [15] W. Jin et al., *IEDM*, 1999; [x] A.J. Scholten et al., *IEDM* 2009.

Improvement by increasing heat dissipation through the gate stack?

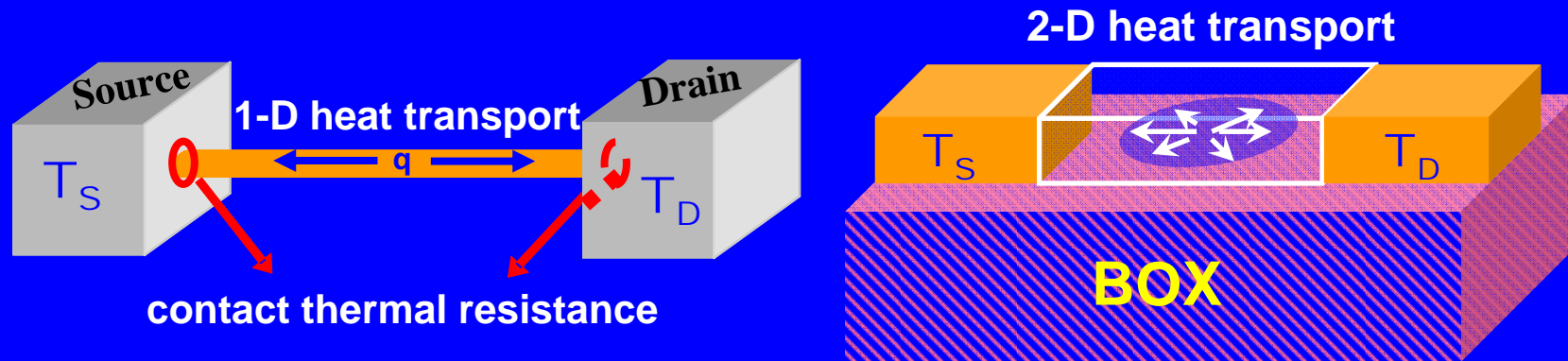
- High-k gate dielectric has better thermal conductivity than SiO₂ or SiON gate material
- but still have non-negligible SHE when $d_{NW} < 14\text{nm}$



HfO_x / TaN gate, $L_G = 21\text{ nm}$

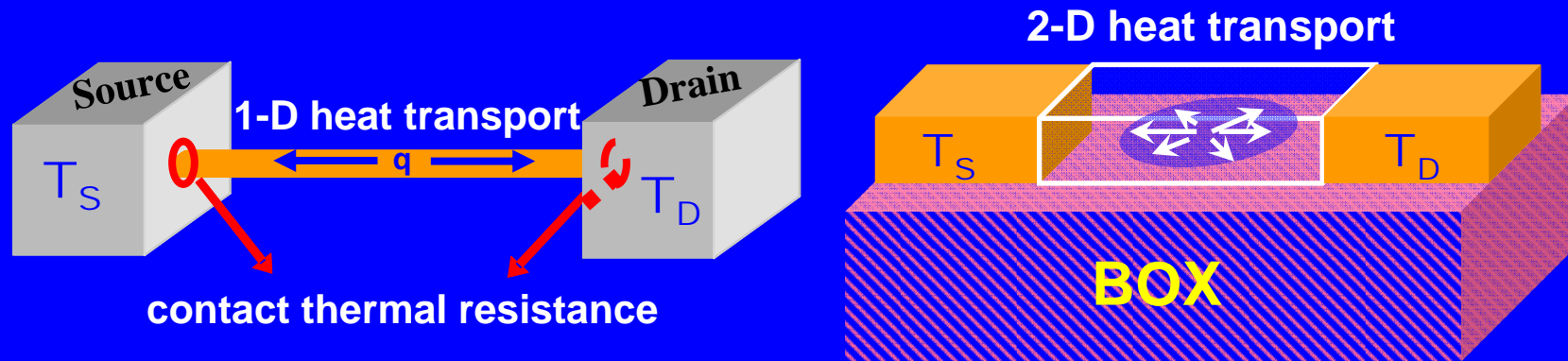
Why degraded SHE in SNWTs?

- 1D heat transport for strongly-confined NW structure – limited modes for heat dissipation



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 - limited modes for heat dissipation

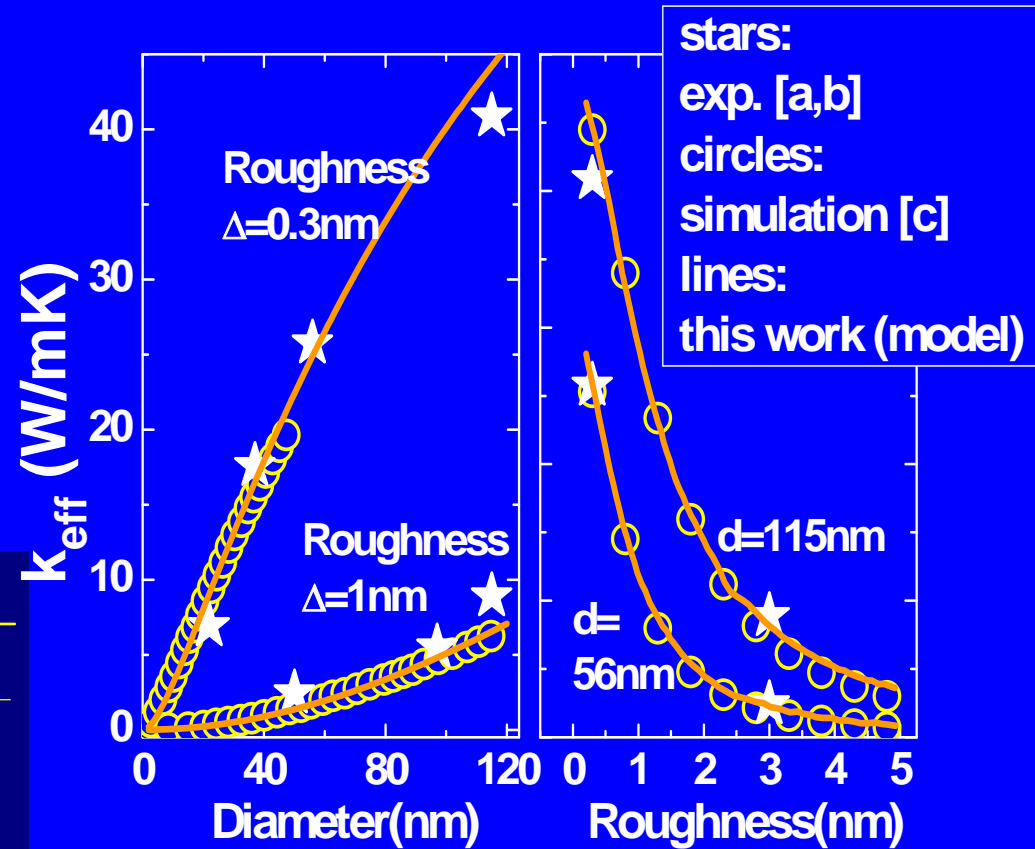


- Additional contact thermal resistance
 - abrupt interface between 1D-NW and 3D-S/D region
 - does not exist in planar devices
- GAA: increased surface/volume ratio, strong phonon-boundary scattering and thus increased boundary R_{th}
 - worse than UTB SOI, DG/TG structures

Thermal conductivity model for Si NWs

The model includes diameter dependence, surface roughness and gate length dependence.

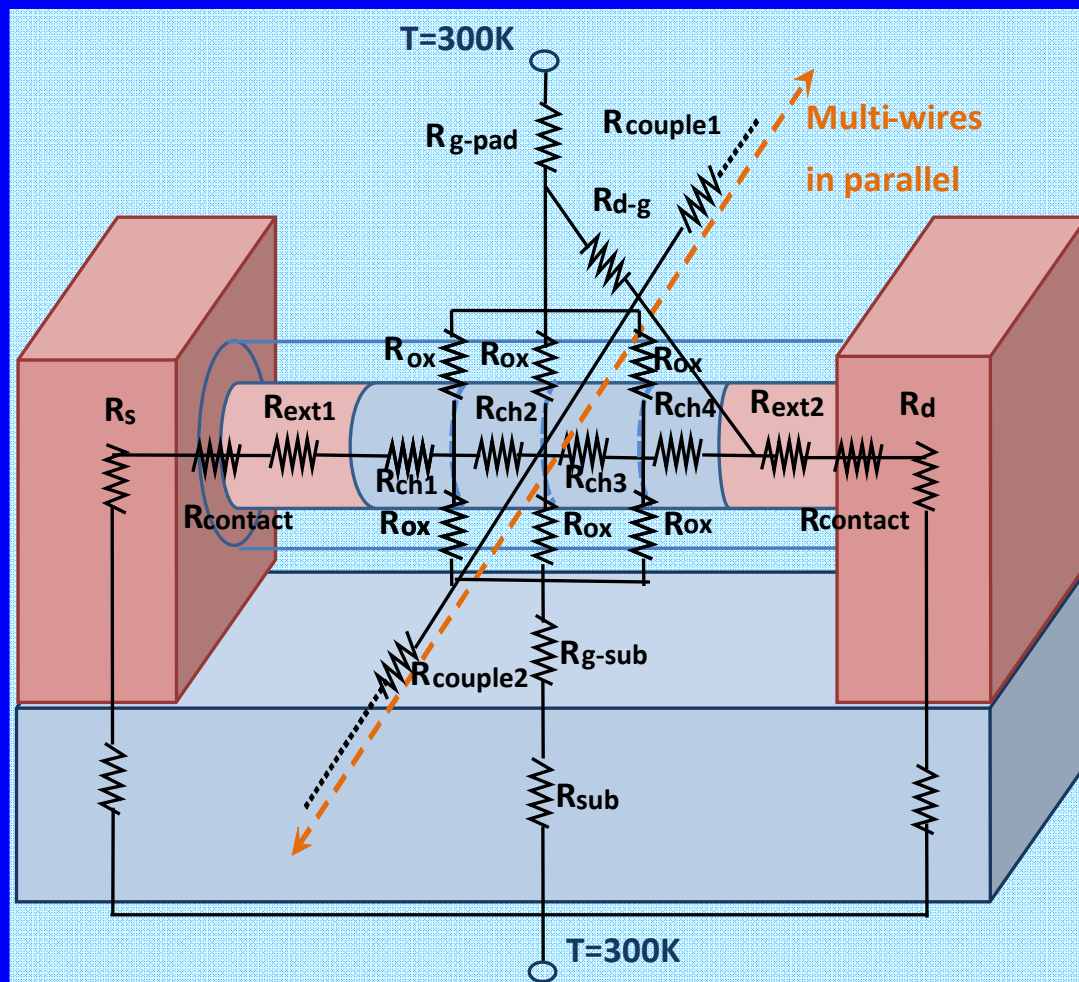
$$k_{eff} = \frac{k_b}{1 + \frac{A}{\frac{d}{\lambda_b} - \frac{d^2}{4\lambda_b^2}} + \frac{B\Delta^2}{d^2} + \frac{C \cdot \lambda_b}{L}}$$



- [a] A. I. Hochbaum et al., Nature, vol. 451, p.163, 2008.
 [b] D. Li et al., APL, vol. 83, p. 2934, 2003.
 [c] P. Martin et al., PRL, vol. 102, p. 125503, 2009.

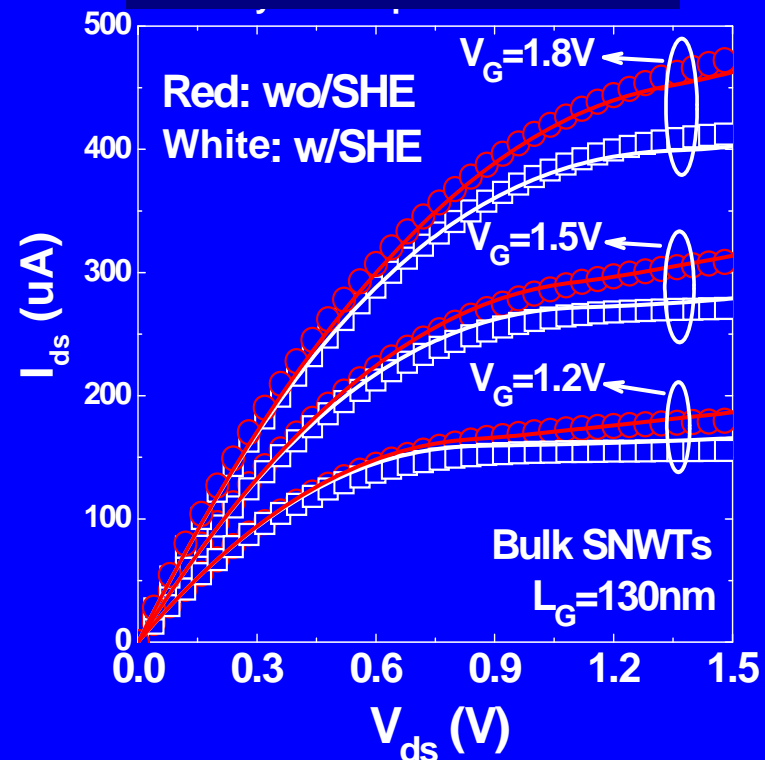
X. Huang, et al., to be published.

Equivalent Thermal Network for SNWTs



Heat dissipation: to big S/D
to gate

Symbol: Experiment
Line: model



X. Huang, et al., to be published.

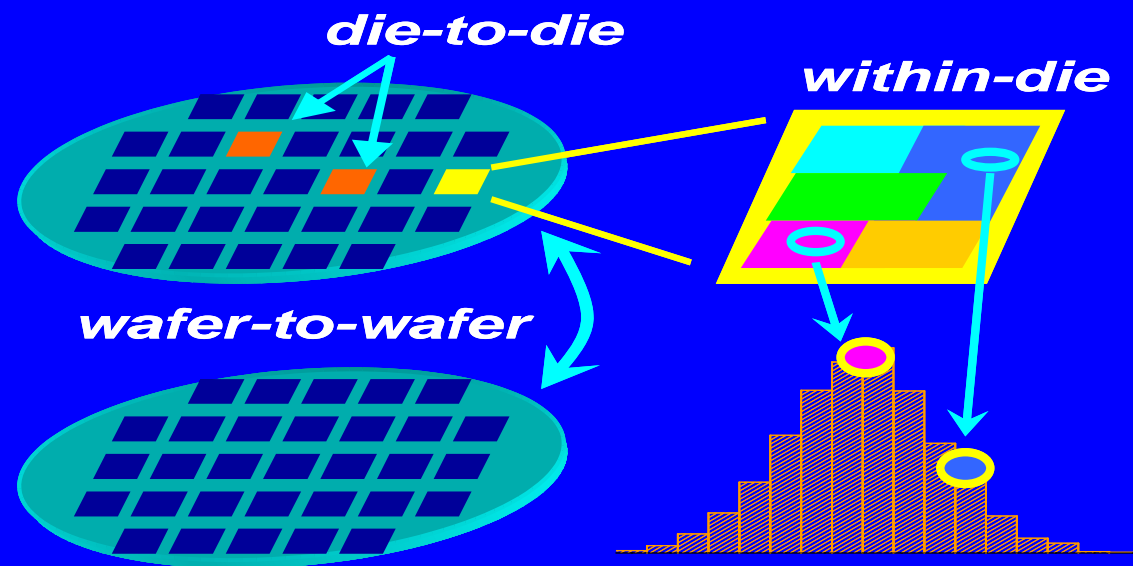
Outline

- Fabrication and integration (a quick review)
- **Recent advances in understanding SNWTs**
 - Intrinsic carrier transport
 - Parasitic effects (R and C)
 - Low-frequency noise
 - Self-heating effects
 - **Variability**
- Recent nanowire circuit demonstrations
- Summary

“There’s plenty of room at the bottom” -- Richard P. Feynman

**“There’s also plenty of noise
and *variation* at the bottom...”**

- Variability challenges in nano-CMOS
 - new process technologies
 - new materials
 - much smaller devices

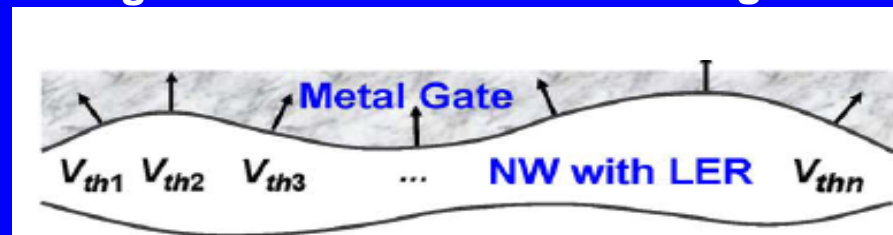
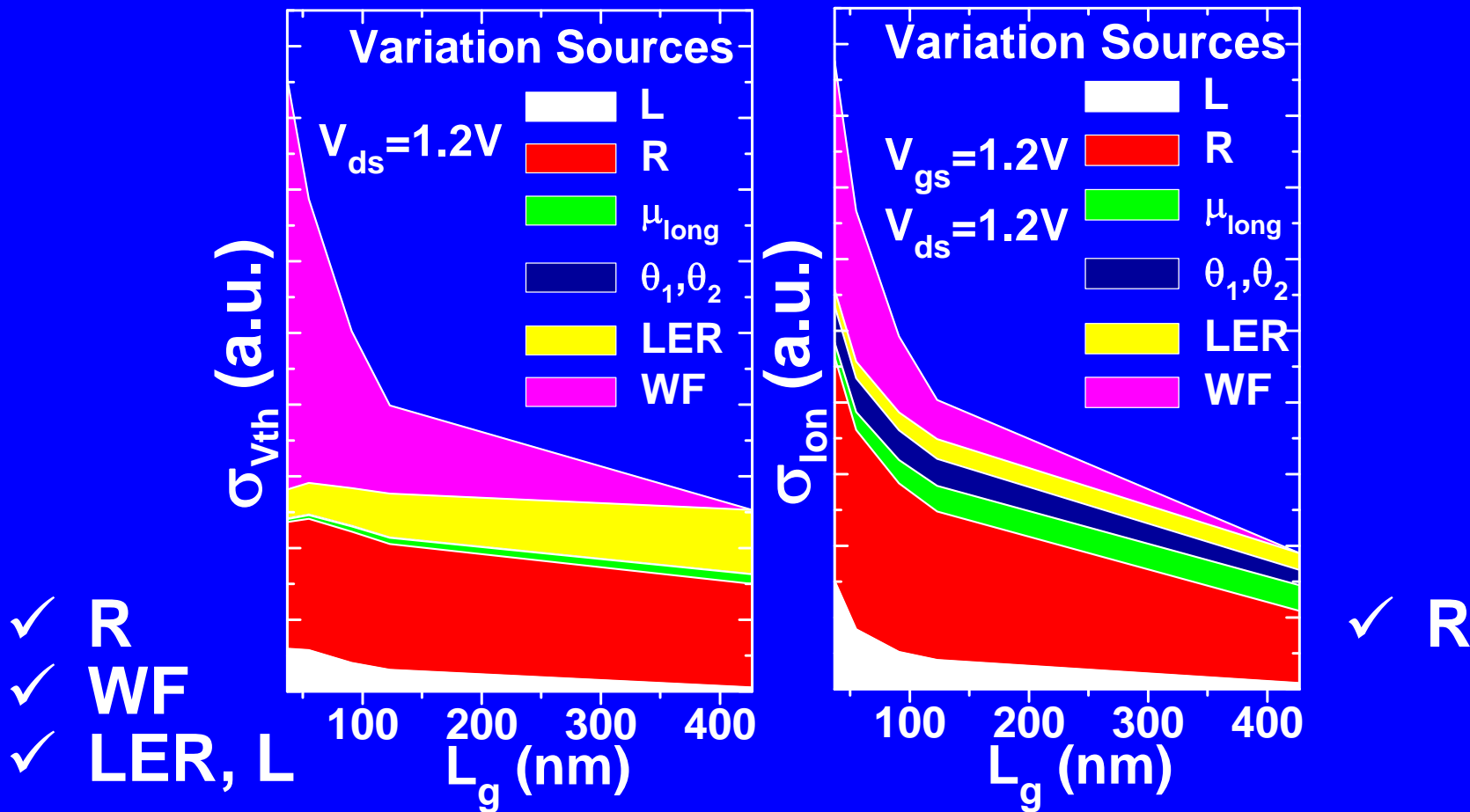


Variation in nano-scale devices

Systematic	OPC, Layout Dependent Strain...
Random	Random Dopants, Line Edge Roughness, High-k Morphology, Metal Gate Granularity...

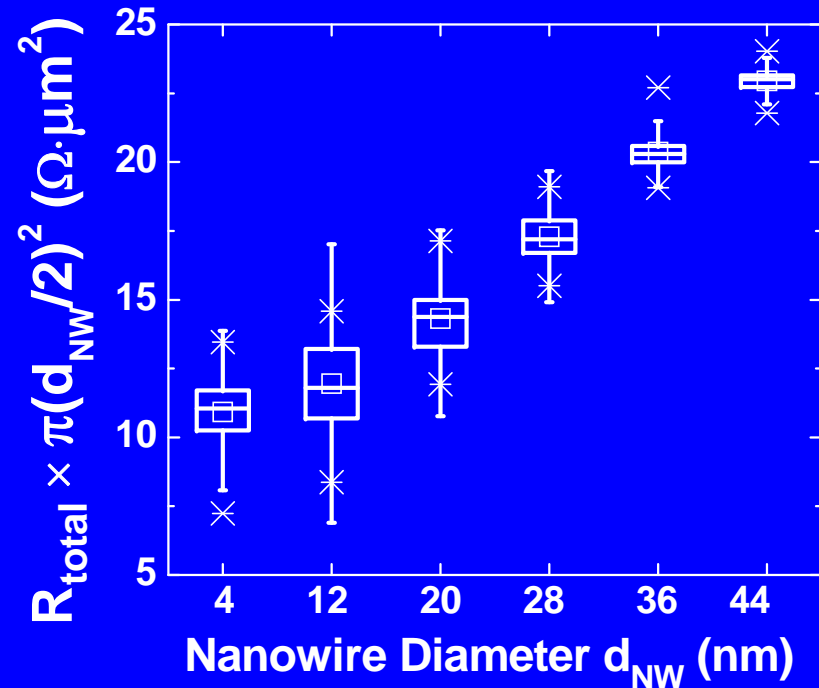
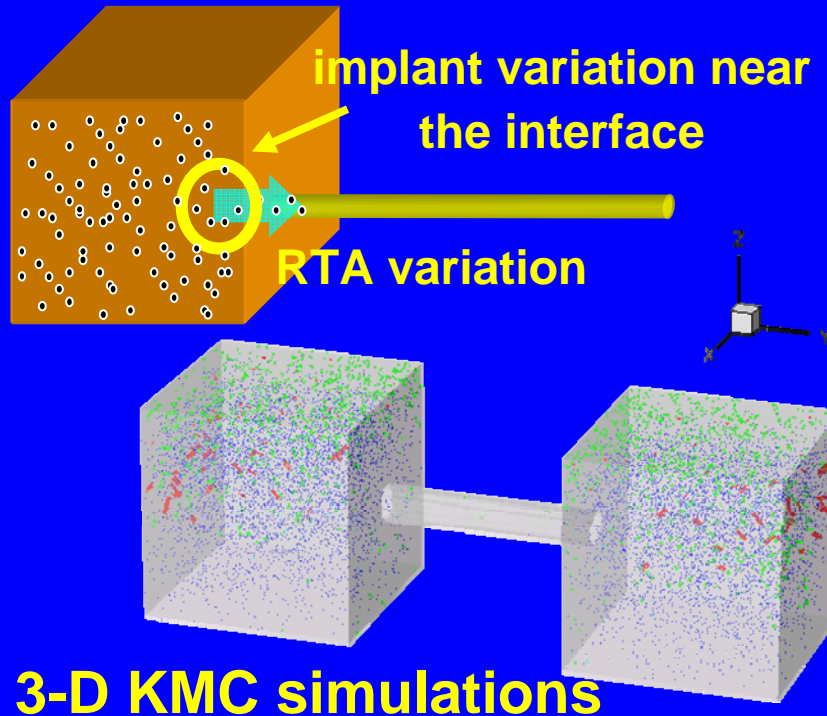
- Random variations near atomic dimensions
 - impacts circuit functionality and stability
- New architecture NWFET with ultra-scaled dimension and surrounding gate structure
 - *What about its variability?*

Impacts of Variation Sources in SNWTs (Experimental Extraction Results)



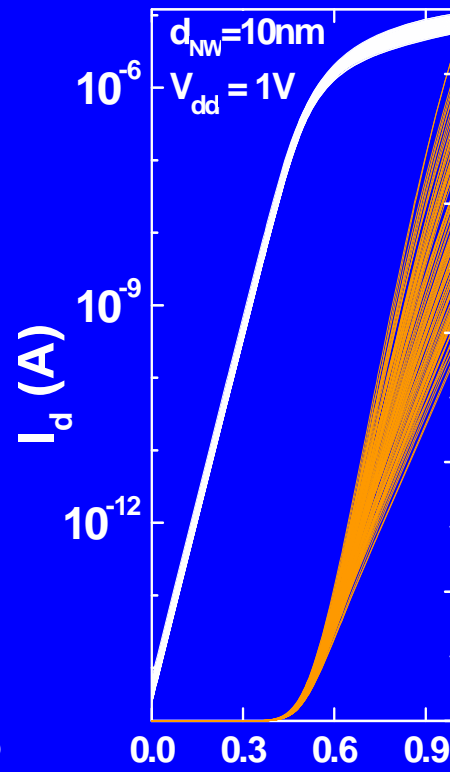
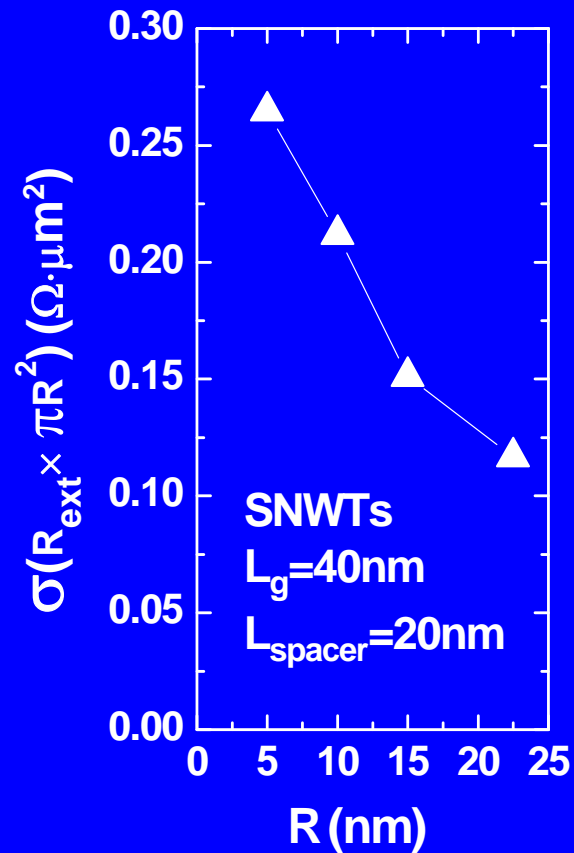
J. Zhuge, et al.,
IEDM 2009, PKU

Discussion - 1/2: SDE RDF (1)

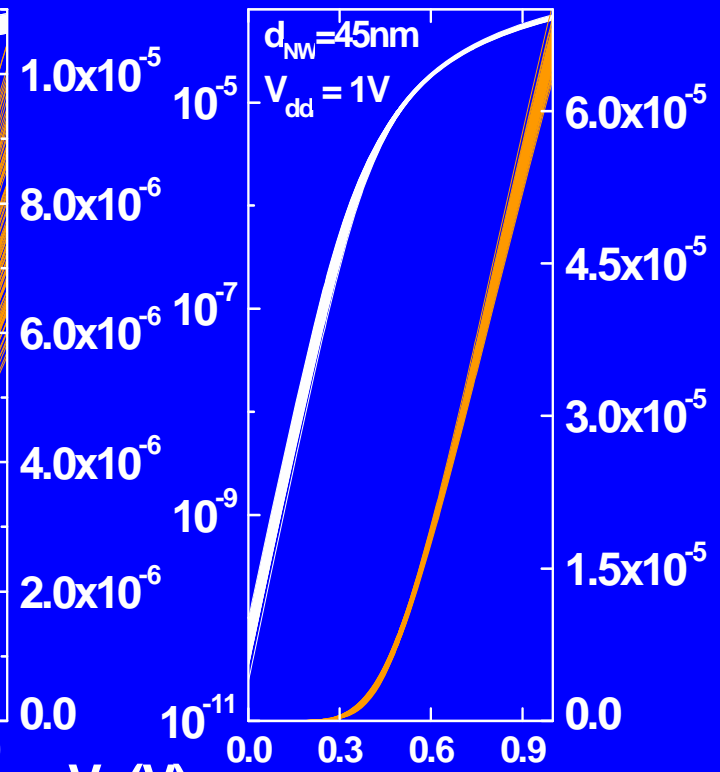


- Diameter-Dependent Annealing (DDA): thinner NW results in faster diffusion
 - R_{ext} reduction and variation
 - R_{eff} reduction and variation

Discussion - 2/2: SDE RDF (2)

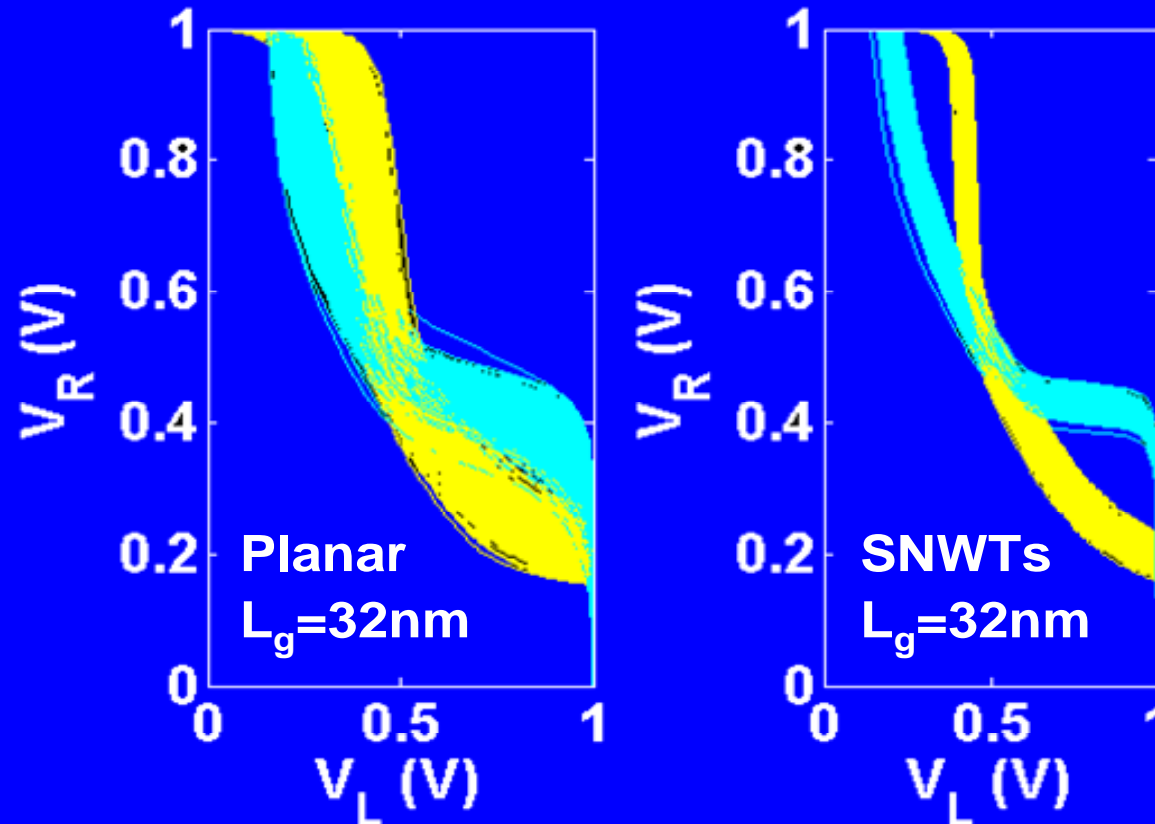


$d_{\text{NW}} = 10\text{nm}$



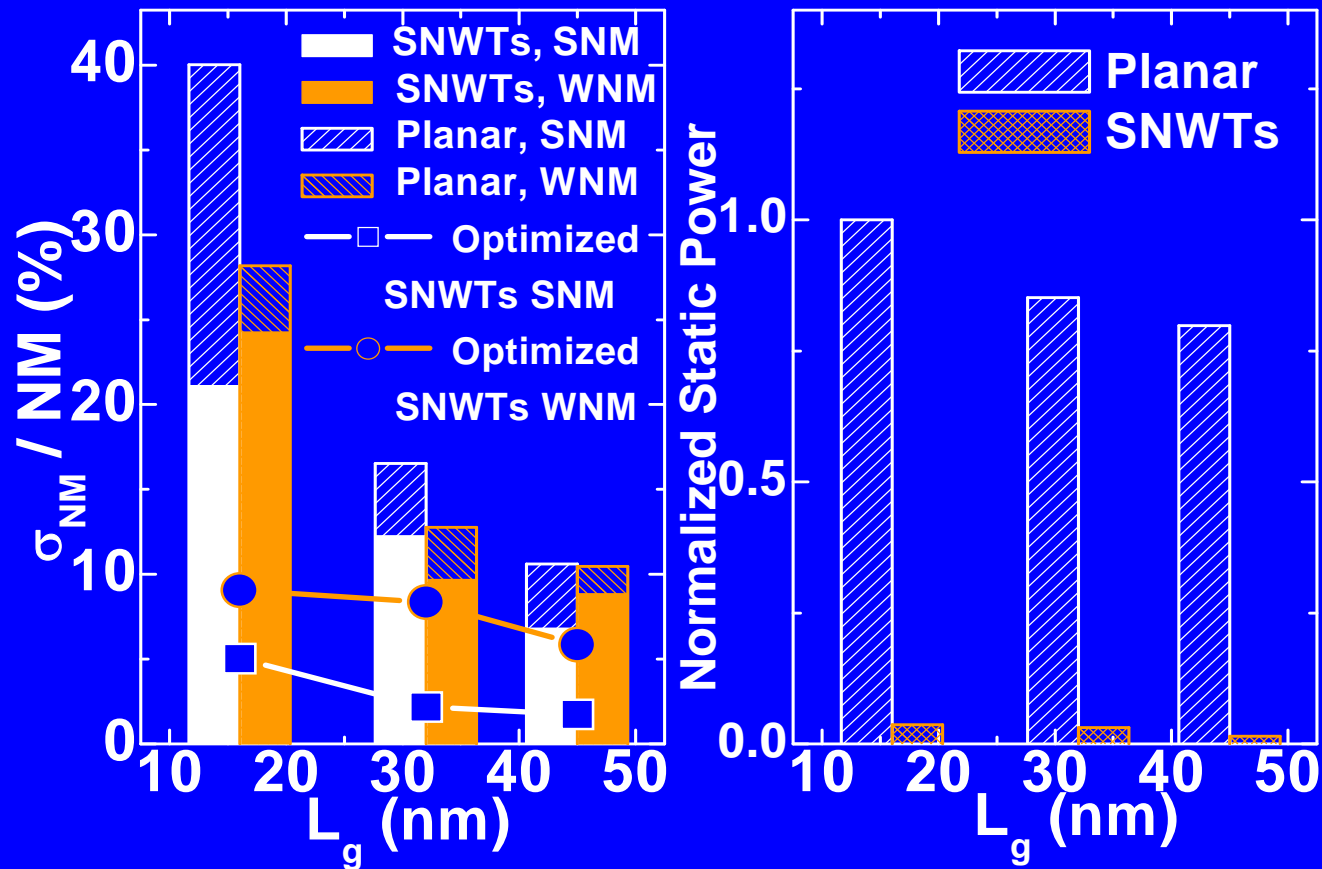
$d_{\text{NW}} = 45\text{nm}$

SNWT vs. planar MOSFET – Simulations -1/2



- **SNWT-based SRAM cells**
 - Larger NM and less variation of noise margin
 - intrinsic channel and excellent SCE-suppression

SNWT vs. planar MOSFET – Simulations -2/2

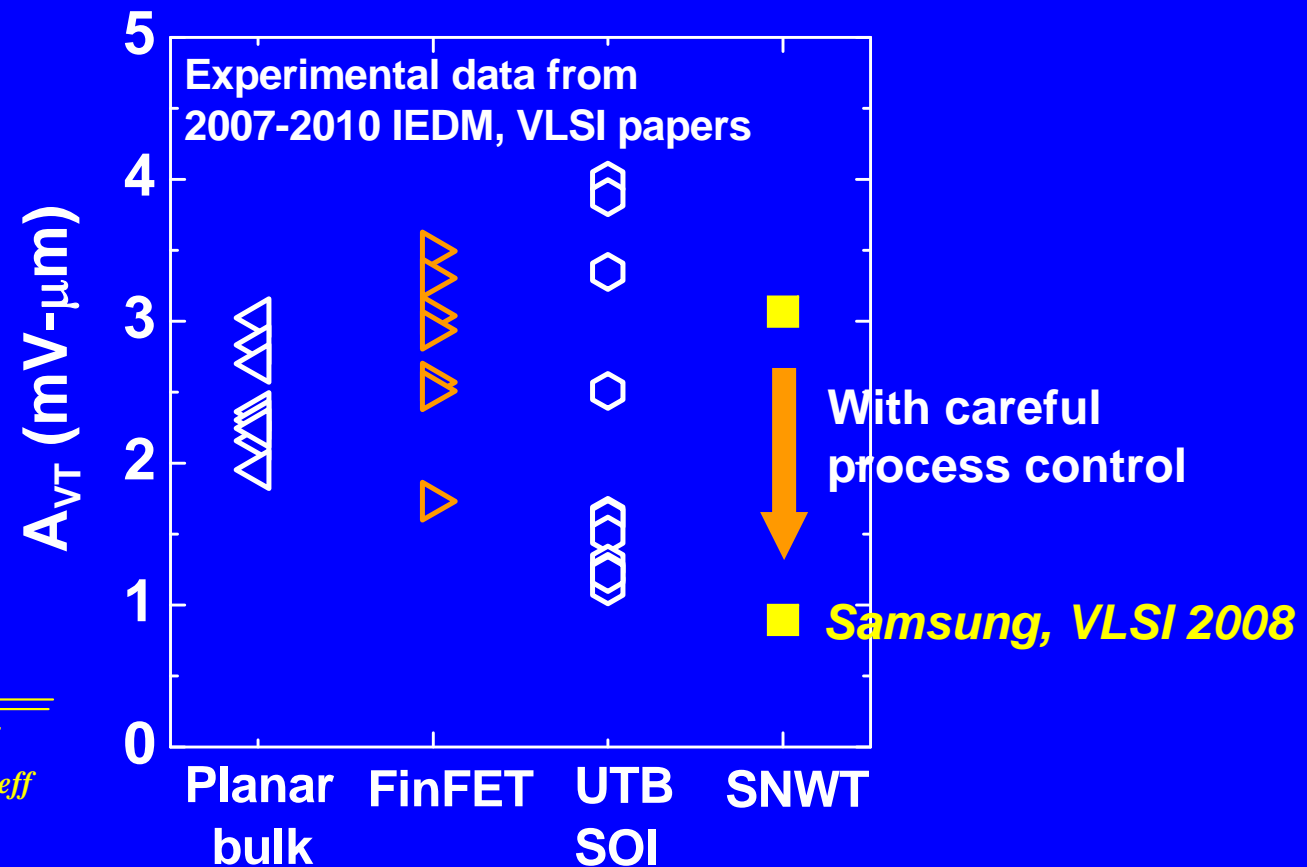


- Scaled SNWT-based SRAM cells
 - Less NM variation and much less static power consumption

Comparisons with FinFET and UTB SOI Devices

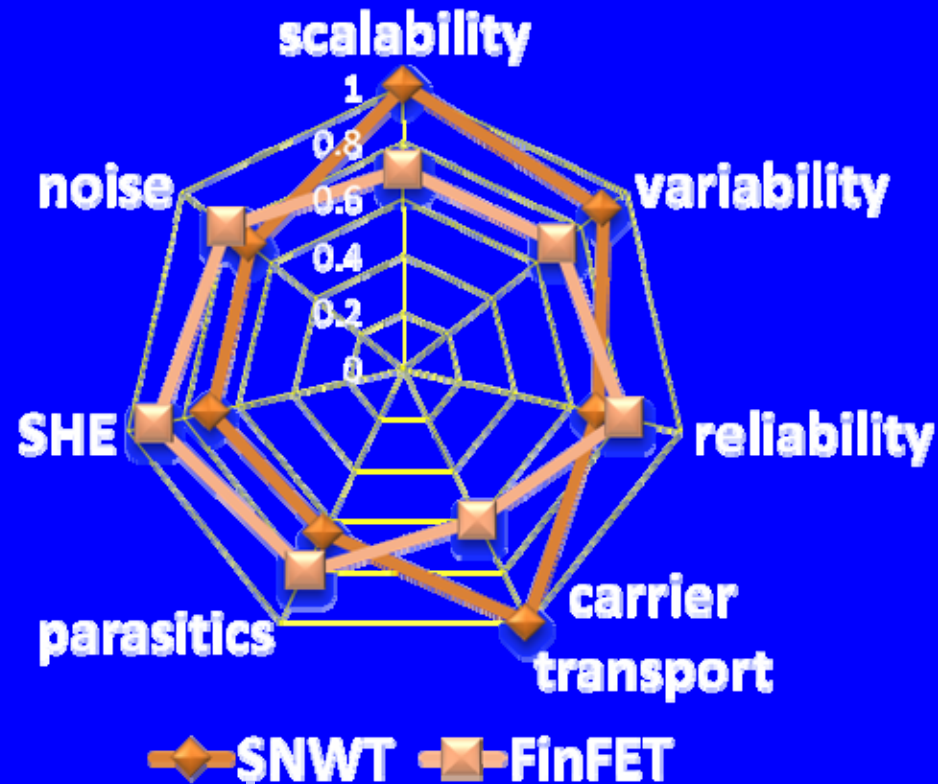
- Experimental demonstrations so far

$$\sigma \Delta V_T = \frac{A_{VT}}{\sqrt{L_{eff} W_{eff}}}$$



Main device characteristics Comparison with FinFETs

- First-order device-level comparisons with FinFETs

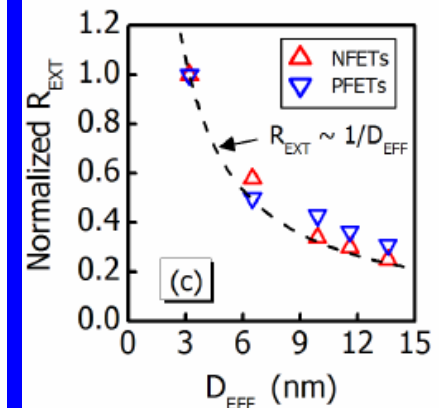
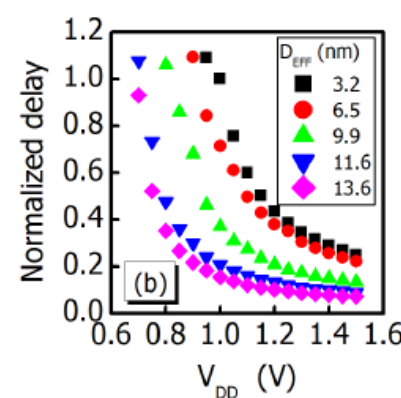
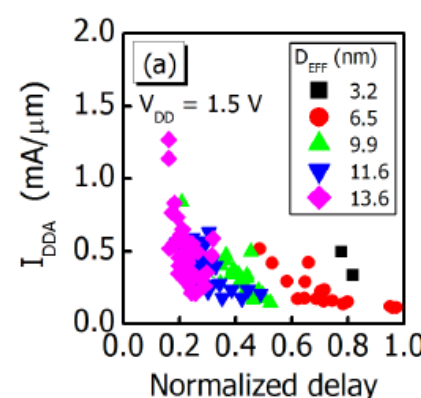
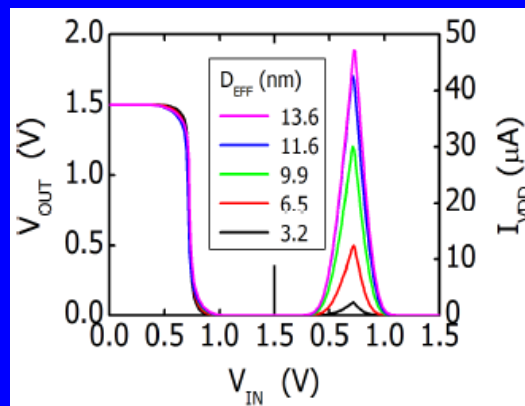
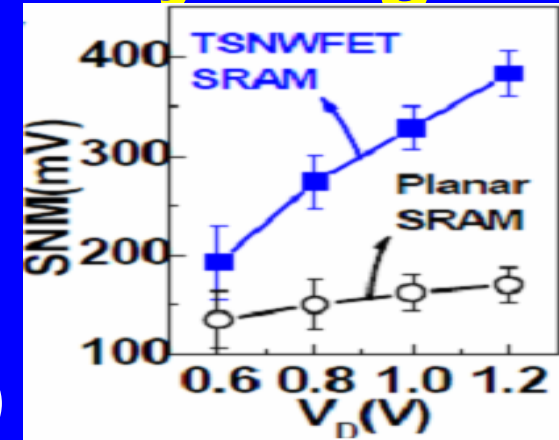


Outline

- Introduction
- Fabrication and integration
- Recent advances in understanding SNWTs
 - Parasitic effects
 - Self-heating effects
 - Variability
- **Recent nanowire circuit demonstrations**
- Summary

Circuit demonstration is at early stage

- SRAM (Samsung, VLSI 08)
 - Larger SNM than planar and FinFET devices
 - Smallest variation demo
- Current Mirror (Peking Univ., T-ED 11)
 - Good performance in both inversion and subthreshold regions
- 25-Stage Ring Oscillators (IBM, VLSI 10)
 - $d_{NW} = 3 \sim 14$ nm, $L_G = 25 \sim 55$ nm
 - Limited by the SDE series resistance, need further improvement



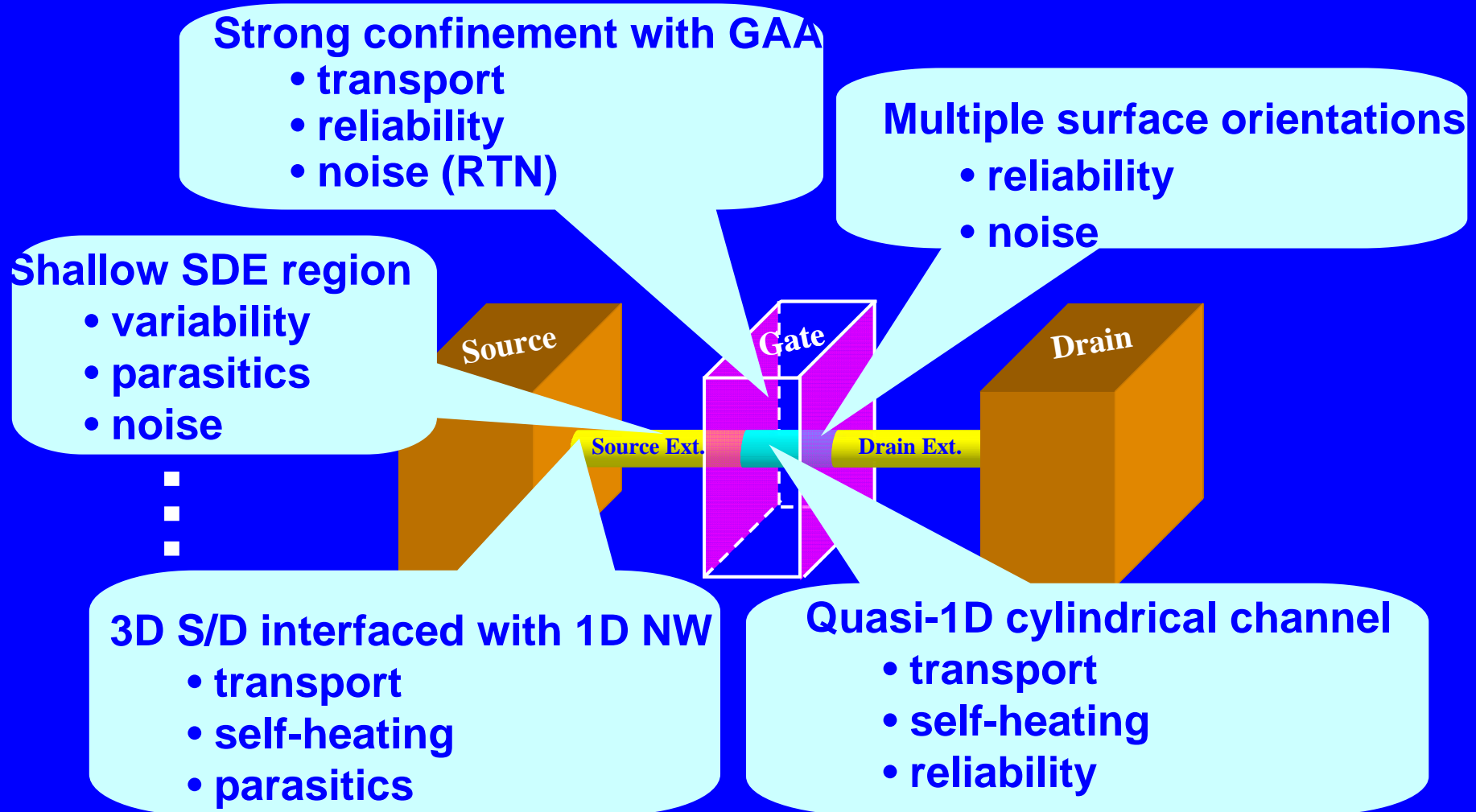
Outline

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- **Summary**

Key Messages for GAA SNWTs: *Summary*

- ✓ **Almost manufacturable: but still needs better process controllability**
- ✓ **Variability: lowest (static) variations**
 - **key variation sources for further optimization: diameter variation, WFV, NW LER, SDE RDF**
- ? **Relatively severe parasitic effects**
- ? **Non-negligible SHE even on bulk: thermal balanced design needed**
- ? **Circuit demonstration: still on the way**

Structure features should be included



Further in-depth understanding and special device-circuit co-design expected



Thank You Very Much!