CALL FOR PAPERS
Special Section on Reconfigurable Systems

The Institute of Electronics, Information and Communication Engineers (IEICE) Transactions on Information and Systems announces a forthcoming special issue on Reconfigurable Systems to be published in February 2018. We invite submissions of original and unpublished papers which will review and promote recent progress in the field of Reconfigurable Systems.

Demand for high-performance computing both with flexibility and low energy consumption is dramatically growing in the industry. Reconfigurable systems attract great interest as one of the solutions for the matter. The origin of reconfigurable systems, programmable logic devices or simple FPGAs, has evolved into today's complex system-on-chip FPGAs, dynamically reconfigurable FPGAs, and furthermore a variety of new reconfigurable computing devices. Exploring more effective hardware architectures and devices seeking for performance, flexibility, dependability, low-power, etc., is indispensable activities in this field. In order to utilize such hardware architectures and devices, design (programming) methodologies have been more and more important since techniques for conventional computing systems are not applicable to the new computing paradigm which reconfigurable systems may open, such as, the distinctive characteristic of dynamic reconfiguration. Sharing the experiences of case studies to apply the systems and methodologies to practical targets is also important for the systems to mature into popular products in the market. The objective of this special issue is to introduce and demonstrate the latest research activities on reconfigurable systems.

Scope:
Possible topics include, but are not limited to the followings.
- Reconfigurable Systems, Processors, Architectures, Devices
- FPGAs and PLDs
- Dynamically Reconfigurable Systems, Reconfiguration Techniques, Virtual Hardware, Adaptive Hardware
- Device and Circuit Technologies for Reconfigurable Systems
- Low Power, Asynchronous, or Dependable Reconfigurable Circuits and Systems
- System Software for Reconfigurable Systems
- Design Methodologies, High-level Synthesis, Test, and Verification for Reconfigurable Systems
- Applications of Reconfigurable Technology (e.g., High Performance Computing, IoT, Machine Learning, AI, Big Data, Cloud Computing)

Submission Guidelines:
The deadline for submission is May 2, 2017, JST. Manuscripts should be carefully prepared according to the guide line in the Information for Authors (available at http://www.ieice.org/eng/shiori/mokuji_iss.html). The preferred length of the manuscript is 8 pages for a paper and 2 pages for a letter. Only electronic submission through the web page (https://review.ieice.org/regist_e.aspx) is accepted. Choose ``[Special ED] Reconfigurable Systems'' from the list in ``Type of Section (Issue)/Transactions''.

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