Analysis of Control Strategy of Active Front End Converter for R-Load

Vibha B. Patel[1] Karan R. Thawani[2]

[1]Sakalchand Patel University, Visanagar, Gujarat, India [2]Hitachi Hirel Power Electronics Pvt Ltd., India

Abstract— This paper represents the simulation and analysis of a front-end converter. The term Active Front End Inverter refers to the power converter system consisting of the line-side converter with active switches such as IGBTs, the dc-link capacitor bank, and the load-side inverter. Active front end converter (AFE or FEC) converts the AC to DC or DC to AC. The basic objective of AFE is to regulate the DC output voltage and make the line side power factor unity. The main advantage of this converter is to eliminate the lower order harmonics or to reduce the total harmonic distortion (THD) caused by a large nonlinear load. And it is done by using the PWM technique. Sinusoidal pulse width modulation (SPWM) is a popular technique used for the control of output voltage. By changing the modulation index, both the frequency and magnitude of the output voltage can be controlled. The modulation index increases as the fundamental line voltage increases. Thus, by changing the modulation index we can able to change the voltage.

Keywords: total harmonic distortion (THD), PWM technique, Sinusoidal pulse width modulation (SPWM), AFC system

I. INTRODUCTION

Front end converters are becoming an interesting solution for power factor correction and low frequency current harmonic elimination in static power conversion systems. The term Front End Converter refers to the power converter system consisting of the line-side converter with active switches such as IGBTs, the dc-link capacitor bank, and the load-side inverter. The line-side converter normally functions as a rectifier. But, during regeneration it can also be operated as an inverter, feeding power back to the line. The line-side converter is popularly referred to as a PWM rectifier in the literature. This is due to the fact that, with active switches, the rectifier can be switched using a suitable pulse width modulation technique. The PWM rectifier basically operates as a boost chopper with ac voltage at the input, but dc voltage at the output. The intermediate dc-link voltage should be higher than the peak of the supply voltage [1]. This is required to avoid saturation of the PWM controller due to insufficient dc-link voltage, resulting in line side harmonics.

The required dc-link voltage needs to be maintained constant during rectifier as well as inverter operation of the line side converter. The ripple in dc-link voltage can be reduced using an appropriately sized capacitor bank [2][3]. The active front-end inverter topology for a motor drive application.

For a constant dc-link voltage, the IGBTs in the line-side converter are switched to produce at input terminals. The line-side PWM voltages, generated in this way, control the line currents to the desired value. When the dc-link voltage drops below the reference value, the feed-back diodes carry the capacitor charging currents, and bring the dc-link voltage back to reference value.

Today, the AFE systems can be used as an interesting solution to realize AC drives. The AFE's main advantages are the four quadrants operation mode and the full control in regenerative braking. Moreover, AFEs guarantee high power quality giving very good performance in terms of Power Factor (PF) and Total Harmonic Distortion (THD) of the supply currents and supply voltages on the ac side [4][5][6]. The two main objectives of the AFE are the regulation of the dc output voltage and the compensation for undesired harmonics on the line current [4] [7].

II. POWER CIRCUIT OF ACTIVE FRONT END CONVERTER

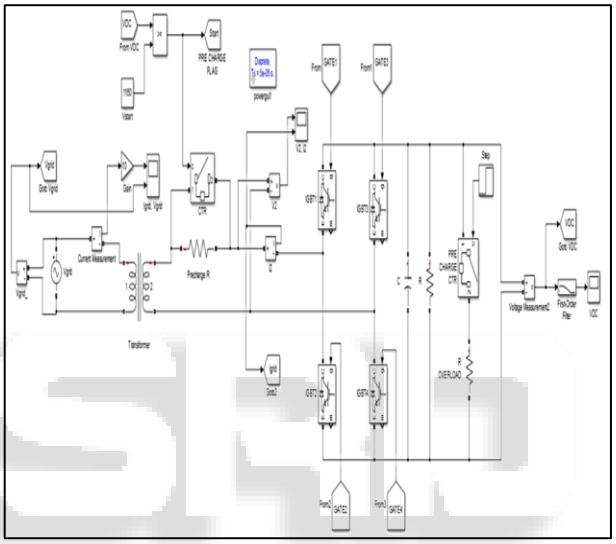

Fig. 2.1: Power Circuit of Active Front End Converter

The Power circuit is mainly divided into the following parts:

1) Single-Phase Step-Down Transformer
2) Pre-charge resistor and contactor
3) IGBT PWM Rectifier
4) DC Link or DC Bus

A. Single-Phase Step-Down Transformer

It is used to step down the grid voltage with the transformation ratio, V1/V2= 26.69. It is also used as a booster to step up the DC Voltage. Hence no other boosting inductor is required.

B. Pre-charge Resistor and Contactor

The capacitor acts as a short circuit at the moment instant when applying DC voltage, hence it draws a very large amount of current from the grid which may result in the damage of the power semiconductor device and the capacitor itself. Hence pre-charge resistor is used to limit the starting current drawn from the DC link capacitors and to smoothly charge the DC bus. It is then bypassed by the contactor when the sufficient DC link voltage is achieved.

C. IGBT Based PWM Rectifier

PWM Based IGBT rectifier is used to boost up the DC link Voltage to the 1800V. It also provides a unity power factor and reduces the THD in the input current.

D. DC Link or DC Bus

DC link capacitor is placed in parallel with the load to minimize the effects of voltage variations as the load changes. The DC-link capacitor also provides a low-impedance path for ripple currents generated by power switching circuits.

III. CONTROL CIRCUIT OF ACTIVE FRONT END CONVERTER

The Control Method is mainly divided into the following parts:

1) Start-up logic
2) Phase Lock Loop
3) SPWM Control Loop

A. Start-up logic

The pre-charge resistor is used to limit the starting current drawn from the DC link capacitors and to smoothly charge the DC bus. In the start-up control circuit, DC link voltage is compared with 1160 VDC. When the soft-start finishes and DC link voltage crosses the 1160V, then START=1 and pre-charge resistor is then bypassed by the contactor.

PWM Start Logic: It takes around 0.2 seconds to smoothly charge the DC bus through pre-charge resistor and PWM are started with a delay of 0.4 seconds. Hence by that time, DC link is built up through IGBT body diodes.
Hence when START=1 and the delay of 0.4 seconds is achieved, then the PWM flag is setup and the PWM control loop is started.

B. Phase Lock Loop

To maintain the input power factor to unity, the input grid voltage phase and frequency must be known. Hence Phase Lock Loop is used to generate a Theta (in radians) in such a way that this theta is the same as the theta of the input grid voltage.

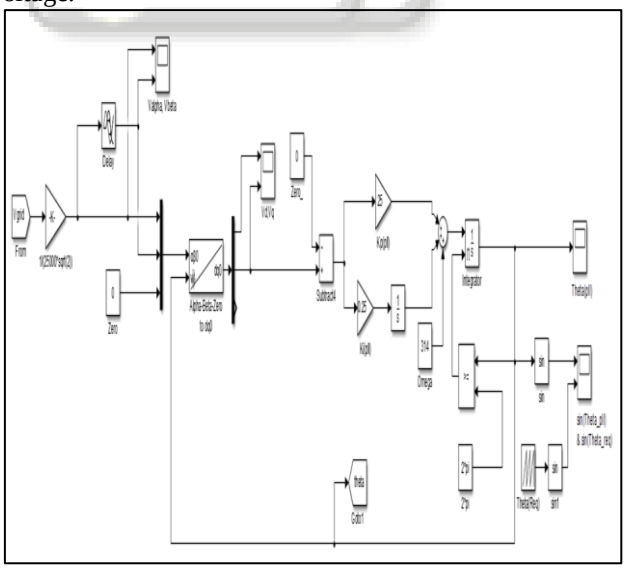

Fig. 3.1: Control Circuit of PLL

First, The Vgrid is scaled down by the gain of 25000*1.412. Then it is applied as an alpha component to the Alpha-beta stationary reference frame. Since we have only one phasor as an input, this alpha component is delayed by 90° to generated the beta component of the Alpha-beta stationary reference frame. These vectors are then converted into the DC quantity by transforming this vector into the dq-rotating reference frame.

Since we know that when the frequency and phase of the d-rotating reference frame is aligned with the alpha component, then the Vd = Peak amplitude of the alpha component and Vq = 0. Hence, this condition is used to control the speed of the dq-rotating reference frame in such a way that Vq becomes zero. The actual Vq is compared with the Vq(reference) i.e. 0. The difference between the actual Vq and Vq(reference) is called the error which is then applied to the PI controller. The aim of the PI controller is to reduce this error and generate the omega in such a way that this error becomes zero.

This omega is then integrated to generate the theta which is then fed back to the dq the rotating reference frame for the closed loop control of the theta.

C. SPWM Control

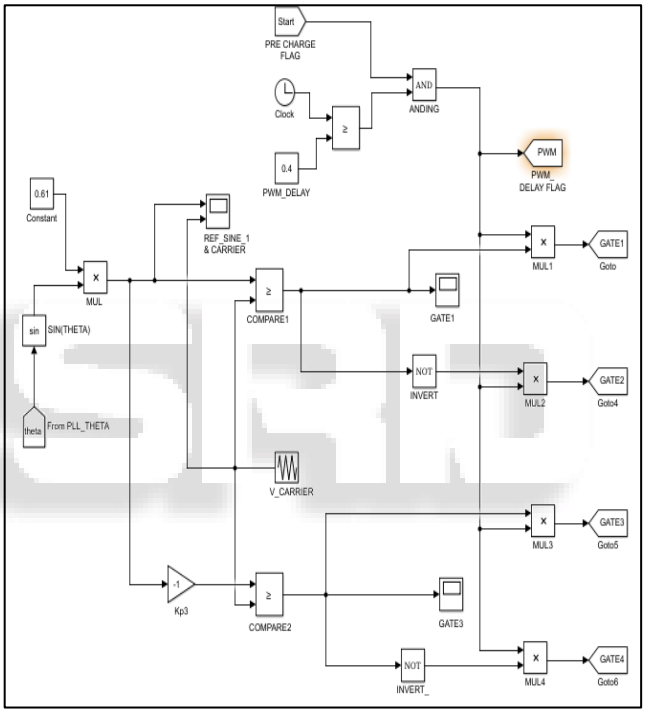

Fig. 3.2: SPWM Control Circuit for open loop

For now, the control circuit is implemented with a fixed modulation index of 0.61 which means open loop control of dc-link voltage. This control loop generates the gating signals for the power semiconducting devices. Theta obtained from PLL is used to generate the unity sine wave which is then multiplied with the fixed modulation index of 0.61 to generate the reference sine wave for Phase lag 1. This sine wave is then inverted which becomes the reference sine wave for phase lag 2. This both sine waves are then compared with the high frequency carrier wave for the generation of gating signals. When the amplitude of the reference sine wave 1 is greater than the carrier wave, the IGBT1 is turn on and invert logic is applied for the IGBT2. Similarly, when the amplitude of the reference sine wave 2 is greater than the carrier wave, the IGBT3 is turn on and invert logic is applied for the IGBT4.

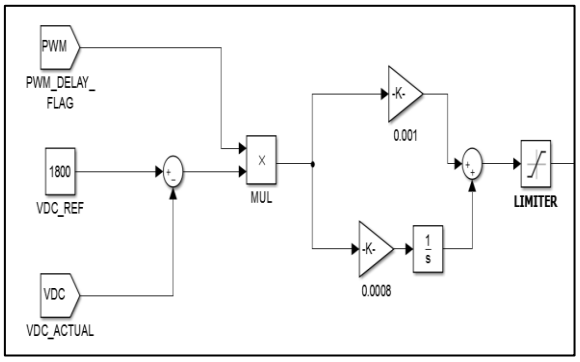

Fig. 3.3: DC Link Voltage Control Loop

This loop is started when the sufficient DC is built up through the pre-charge circuit and the PWM delay flag is set to high. This loop maintains the Output DC Voltage to the Vdc(reference) considering the allowable ripple voltage. Here, the actual DC Voltage is compared with the Vdc(reference) i.e. 1800V. The difference between the actual DC Voltage and Vdc(reference) is called the error in the DC voltage with reference to Vdc(reference). This error signal is applied to the PI controller. The aim of the PI controller is to reduce this error in the DC Voltage and produce the equivalent current signal.

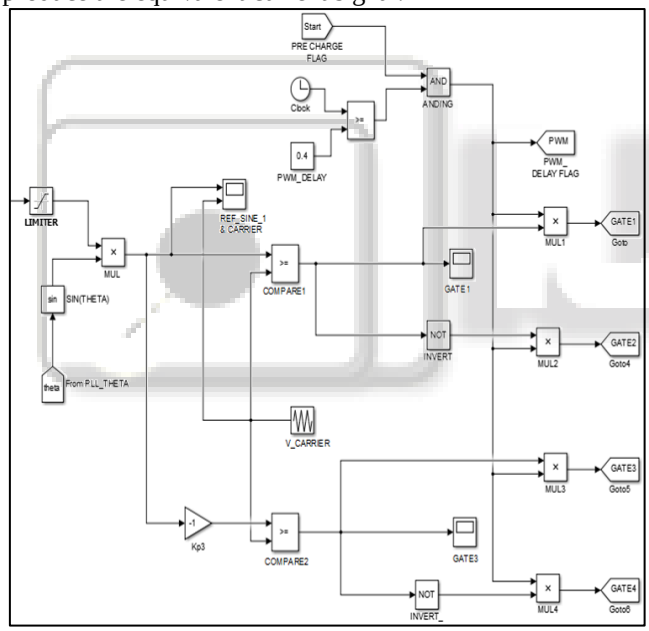

Fig. 3.4: SPWM Control Circuit for close loop

The input signal to this control loop is the error in the actual DC voltage to achieve the required VDC and to maintain the power factor to the unity. This control loop generates the gating signals for the power semiconducting devices. Theta obtained from PLL is used to generate the unity sine wave which is then multiplied with the output of the PI controller to generate the reference sine wave for Phase lag 1. This sine wave is then inverted which becomes the reference sine wave for phase lag 2. This both sine waves are then compared with the high frequency carrier wave for the generation of gating signals. When the amplitude of the reference sine wave 1 is greater than the carrier wave, the IGBT1 is turn on and invert logic is applied for the IGBT2. Similarly, when the amplitude of the reference sine wave 2 is greater than the carrier wave, the IGBT3 is turn on and invert logic is applied for the IGBT4.

IV. SIMULATION RESULTS

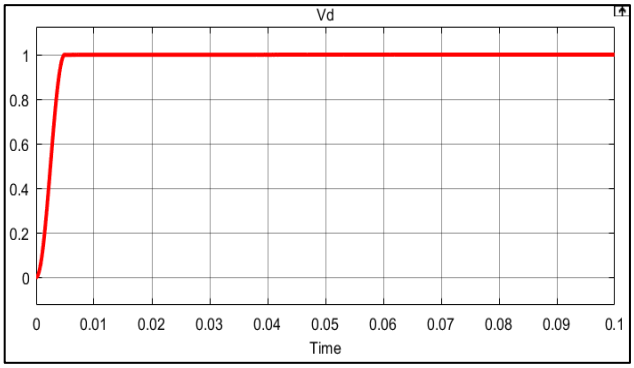

Fig. 5.1: Controlled Vd Generated from PLL

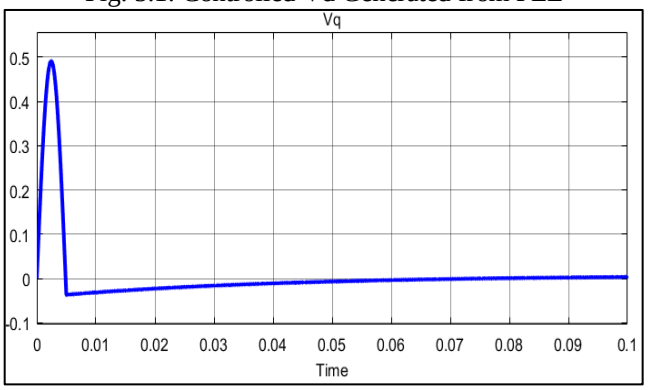

Fig. 5.2: Controlled Vq Generated from PLL

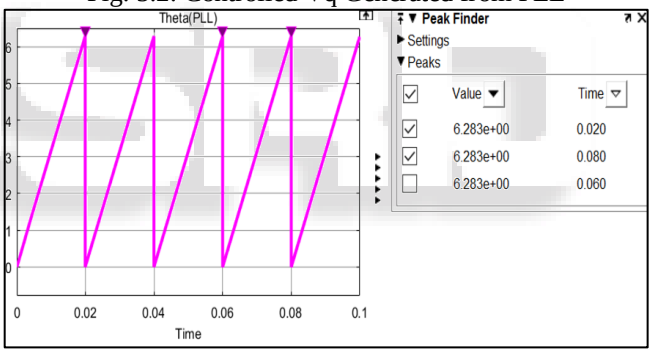

Fig. 5.3: Controlled Theta Generated from PLL

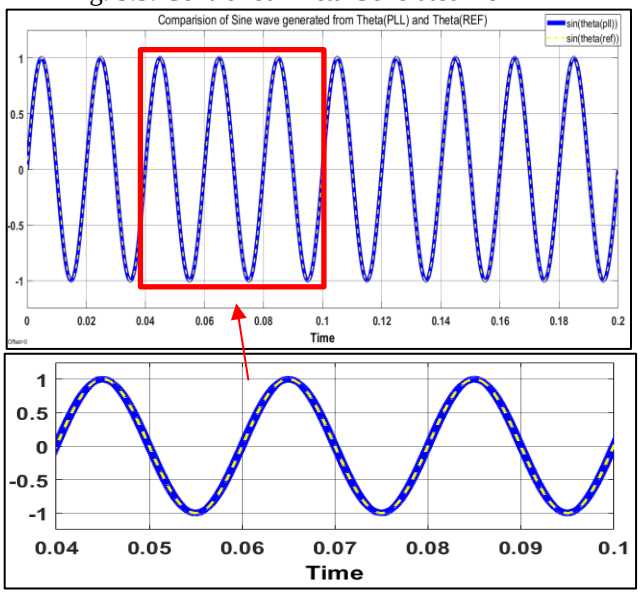

Fig. 5.4: Comparison of Sine Wave Generated from Theta(PLL) and Theta(REF)

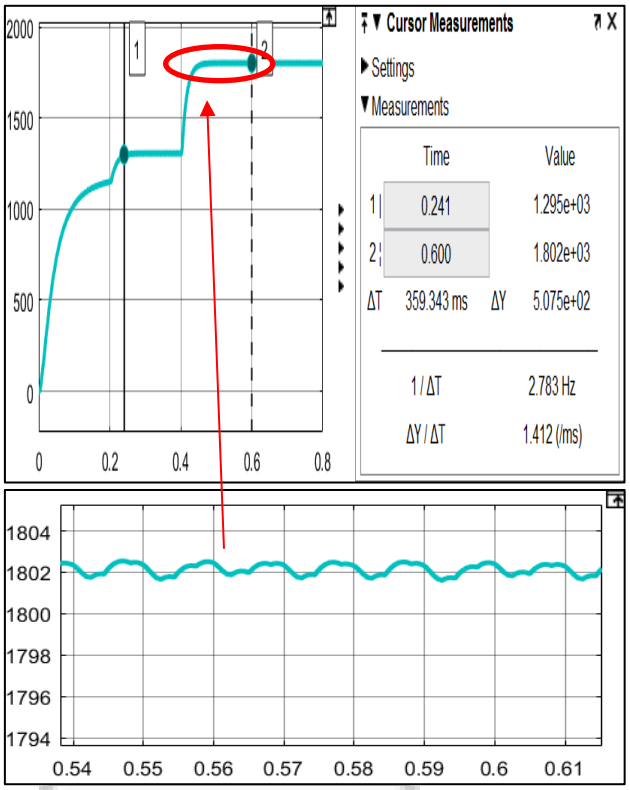

Fig. 5.5: Output DC Voltage Waveforms with SPWM Control

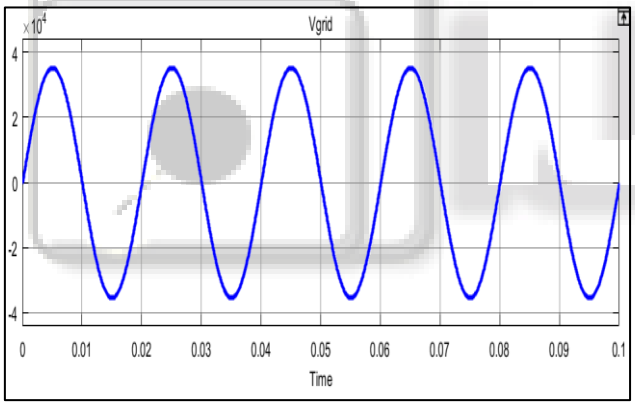

Fig. 5.6: Input Grid Voltage Waveform

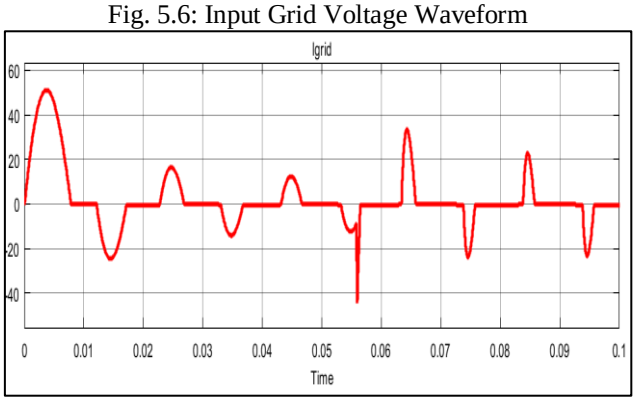

Fig. 5.7: Input Grid Current Waveform during Pre-charge Time

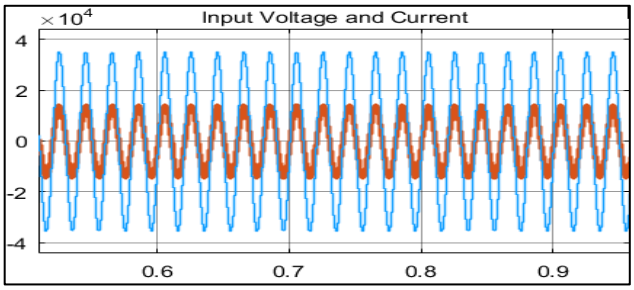

Fig. 5.8: Input Grid Voltage & Current Waveform at Steady State

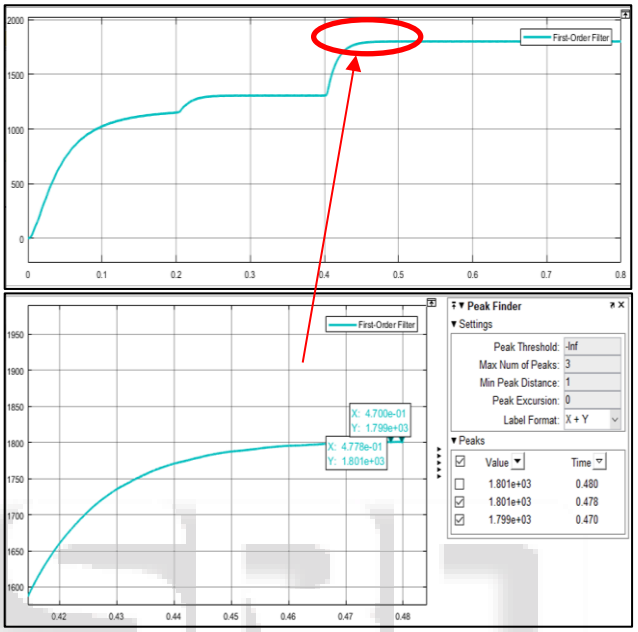

Fig. 5.9: Output DC Voltage Waveforms with SPWM Control for Close loop

Here, we can see the different results of the open loop and close loop proposed circuit with their analysis at different modulation index.

V. Conclusion

Closed loop AFC system is more reliable than open loop AFC system because it automatically adjusts the modulation index as load changes. Hence, we get the desired DC-link voltage from 0 to 100% rated load. Open loop means there is no feedback of DC-link voltage. By adjusting the modulation index, we get our desired DC-link voltage and it is for fixed defined load only. If the load will change, DC-link voltage will be changed because there is no feedback loop and there is no closed loop control of the DC-link voltage. Closed loop means there is the feedback of DC-link voltage and by controlling the DC-link voltage (Maintaining the DC-link voltage at the desired reference value in all load conditions), modulation index is automatically adjusted as load changes.

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