Enhancing Printed Circuit Board Layout Using Thermo-Mechanical Analysis

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Abstract
The use of high performance electronic assemblies in harsh environments subject solder interconnects to complex loading conditions that are primarily driven by the behavior of circuit card assembly and mounting constraints. These assemblies contain a variety of surface-mount devices which are sensitive to thermo-mechanical (TM) fatigue. Stresses generated by placing certain components within the vicinity of mechanical structures, such as standoffs and connectors, can further influence solder fatigue by increasing PCB strains. The mounting constraints can subject packages to loads which are not expected to occur under non-constrained PCB configurations often used in accelerated testing. In order to determine the influence of complex board constraints on electronic components, thermal simulations are performed using finite element analysis (FEA). Detailed models of large electronic assemblies are often tedious and time consuming to construct. In this study, TM simulations of electronic assemblies are implemented to investigate the effect of mounting conditions on board strains. The software used in this analysis enables fast integration of package level and printed circuit board (PCB) features from design files into comprehensive models enabling efficient analysis of the entire board level assembly under thermal loads. These simulations capture the contribution of both local and global coefficients of thermal expansion (CTE) mismatch in the vicinity of mounting conditions and components. The software package implemented in this analysis enables the prediction of board behavior of complex electronic assemblies under TM loads and provides an efficient approach to enhancing circuit board layout.

Introduction
Prediction of board level reliability of solder interconnects often depends on quantifying the CTE mismatch between the electronic component and the PCB. Special attention is placed toward the type of component for fatigue analysis as it dictates the solder joint geometry and effective CTE mismatch the joint will experience at a particular environment. As more intricate IC packages are integrated into harsh environments such as those experienced by automotive and aerospace applications the board level TM deformation becomes a primary concern. Board level reliability is directly influenced by the box level which incorporates the housing and mounting points on to the PCB. Decisions regarding mounting conditions are often made with the intent of the expected use environment. Rubber dampers, spacers and encapsulants can be used to provide shock and vibration attenuations. In some instances, selection of mounting conditions to fit specific load requirements could make the assembly more susceptible to different failure modes which were previously not considered to be a reliability concern. To explore the weakness of component layout, assemblies could undergo accelerated thermal cycling and vibration testing. Although experimental validation of board level assemblies provides useful information, they are costly and time consuming to perform. TM simulations of electronic assemblies offer a time and cost-effective alternative to physical testing. To provide a substitute for physical testing, FEA models should be able to capture certain failure mechanisms in the critical areas of the assembly. This could range from solder and plated through-hole fatigue to capacitor cracking which could occur under thermal loads. As most electronic assemblies and designs are unique, guidelines for board mounting conditions have not been adopted into known industry standards. Furthermore, the shape and construction of many board enclosures are geometrically complex which makes predicting their influence on boards under thermal loads even more challenging. Mounting points in PCB housings can constrain the thermal expansion of the board and induce mechanical loads due to the thermal expansion of the housing prior to noticeable expansion of the PCB itself. Large deformations due to board-housing interactions could induce excessive loads in solder interconnects. To avoid these design pitfalls one connection point on the board should be designed with a rigid attach in the X-Y (in plane) direction. The rest of the bolts should have a shoulder bolt with a smaller diameter than the hole as in Figure 1. This attach method assists in prevents the bending that can occur from the CTE mismatch between the housing and the board.

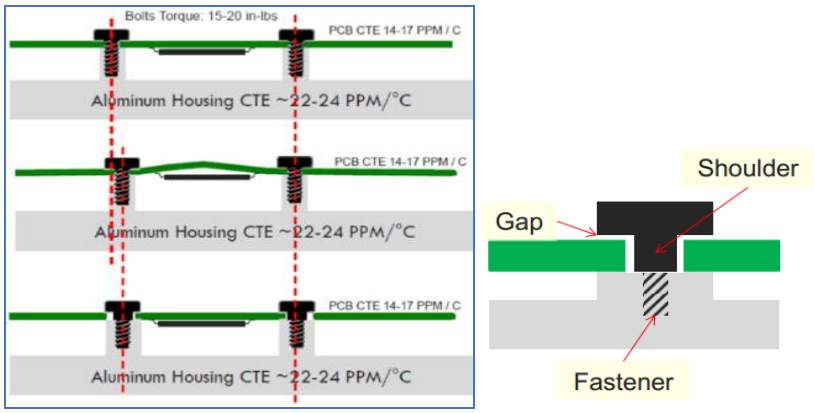

Figure 1. Effect of CTE mismatch and board constraint on leaded surface mount package

In addition to mounting configuration, over-constraining of PCBs and surface mount electronic packages can occur due to the addition of potting, mirroring, heat sinks and additional mounting conditions. An example of such a configuration is evident in the inclusion of heat sinks in Flip-Chip Ball Grid Array (FC-BGA) which have been known to shift the failure location from under the die shadow to corner joints due to the compressive preload and can result in low solder fatigue life prediction [1]. The constraint of PCBs has also been shown to influence the hermeticity of DC/DC power modules in TM analysis [2]. The most popular approach to determine solder joint reliability due to TM loads is to construct a detailed FEA model of the entire assembly. After the physical model is constructed, analysis can be performed at a desired temperature or due to local heat generation from power dissipation. Finite element simulations have been shown to be as accurate as modern test methods in predicting package warpage in flip-chip assemblies [3]. This approach enables integration of validated simulation methods to determine the loads packages experience in board level undergoing TM deformation. Mirrored configuration and package type generally govern the effective fatigue life solder interconnects can experience at a certain environment. Components configuration and board thickness have also been found to contribute to interconnect fatigue life as much as the package design itself [4]. Besides the effect of package type and solder alloy properties, the effect of board deformation on failure modes has not been extensively investigated. Many experimental test set ups for investigating board level reliability under TM loads have been developed in proprietary commercial applications with no widespread adoption by the high reliability electronic manufacturers. A reason for this is the effort required to develop such complex experimental programs and the lack of adaptability across product lines. FEA of entire assemblies offer an alternative to the costly testing and failure analysis. In recent years, results of board level TM simulations have been shown to correlate well with optical deformation measurements [5], further justifying the need for such simulations in the system design process. The influence of housing on assembly level PCB warpage has been also incorporated into TM simulations along with physics of failure based fatigue life predictions for solder interconnects [6,7]. The limitations of performing these simulations are set by the size of the assembly to be modeled and the time required to create each individual package and perform the analysis. Recently, a new approach has been developed similar to the one presented in this paper which enables creation of 3D FEA models from ECAD files [8]. This method enables accurate creation of PCB and package detail that provides sufficient simplifications that enable TM simulations in a shorter solution time without compromising the detail necessary to capture the stress behavior in solder interconnects.

The software package presented in this paper demonstrates recently developed TM analysis which complements the suite of mechanical and physics of failure based analysis methods for electronic components and assemblies [9, 10].The capabilities provided in these analyses are a culmination of numerical techniques and engineering principles interacting together to predict board behavior under thermal loads which otherwise were reserved for small scale or package specific simulations [11]. With the growing number of components in PCB assemblies, identifying critical components or potentially hazardous regions on the PCB for package placement were not effectively addressed. This paper demonstrates the effect of PCB mounting conditions could have on board behavior during TM loads and demonstrates the software package specifically designed to address these challenges.

Over-constrained PCB with BGA Package

Practical illustrations of the effect PCB mounting conditions have on surface mount components are lacking in literature. To demonstrate the influence of mounting conditions on second level solder interconnects, a test vehicle was designed. Solder joints in electronic packages such as BGAs are particularly sensitive to package and board warpage which occur often under thermal loads [12]. An increase in 0.6mm in initial warpage across the board assembly was found to reduce thermal fatigue life by almost 19 percent. Figure 2 depicts the test vehicle constructed to study package and board warpage under various

constraint conditions using Digital Image Correlation (DIC) system. Measurements of the test vehicle are currently ongoing and will be published in subsequent work. The test vehicle was constructed in a manner that will allow contribution of both chassis compliance, housing CTE and proximity of mounting points to the component. Commonly used electronics housing materials such as aluminum, steel and copper are used to alter the effect the housing CTE imposes on PCBs and the compliance standoffs introduce to constrained PCB warpage. An aluminum base plate with 8.8mm thickness with 25mm tall standoffs is used for initial modeling using features available in the software package described in the following sections. Thermal simulations of the assembly are performed at two temperature extremes indicative of those experienced during accelerated thermal cycling conditions of -45°C and 125°C. During thermal expansion and contraction of the test vehicle, the aluminum base plate with a CTE of 24 ppm/°C contracts and expands more than the PCB with a CTE of 17 ppm/°C while the 17mm BGA package with 256IO expands according to an effective CTE of approximately 10ppm/°C. Figure 3 shows the direction of material expansion relative to each peak temperature. Arrows are colored to represent the hierarchical CTE transition from component to housing. Figure 3C graphs the axial strain extracted from each solder joint along the diagonal of the BGA package in order to represent the influence of mounting constraints. In this figure Mount A refers to the farthest mounting conditions of Figure 3 and Mount B refers to mounting nearest to the BGA package. A control case with no aluminum standoff is used for comparison against the two mounting constraints. It is evident that the farthest mounting conditions with the largest distance from the component indicates similar results in peak axial strain which are recorded at the package corners. A die size with die shadow laying on the corner row BGAs was used for this analysis to induce large axial strains in the corner balls of the BGA. Under thermal cycling an increase in strain due to mounting conditions as evident in this simulation can result in significant reduction of cycles to failure. This example illustrates the influence PCB boundary conditions could have during TM analysis.

Automated Design Analysis

Constructing a detailed model of a large multi-layer circuit board using commercial finite element platform is intrinsically difficult and time consuming. The software package used in this analysis imports production design files containing information on each layer in the assembly and reconstructs a detailed 3D meshed geometry of the circuit card. The part description is taken from the design files and used to construct 3D geometry for leaded and leadless components alike. Individual properties of each package and associated material properties can be then be selected to outfit the specific component details. A wide variety of mold compound and electronic polymers are available in the built-in material library. This library contains information on the material's mechanical, thermal and electrical properties. Figure 4 illustrates the generated printed board layer and parts from the design file. Effective properties of the generated PCB are automatically calculated. These calculations provide approximation of the circuit card properties which will influence the CTE mismatch solder interconnects experience during thermal excursions. The PCB orthotropic properties and boundary conditions are highly influential on the fatigue performance of plastic packages. Improper selection of PCB material properties and boundary conditions can result in improperly capturing the lead deformations and result in unrealistic strain and fatigue life predictions in wire bonds [13].

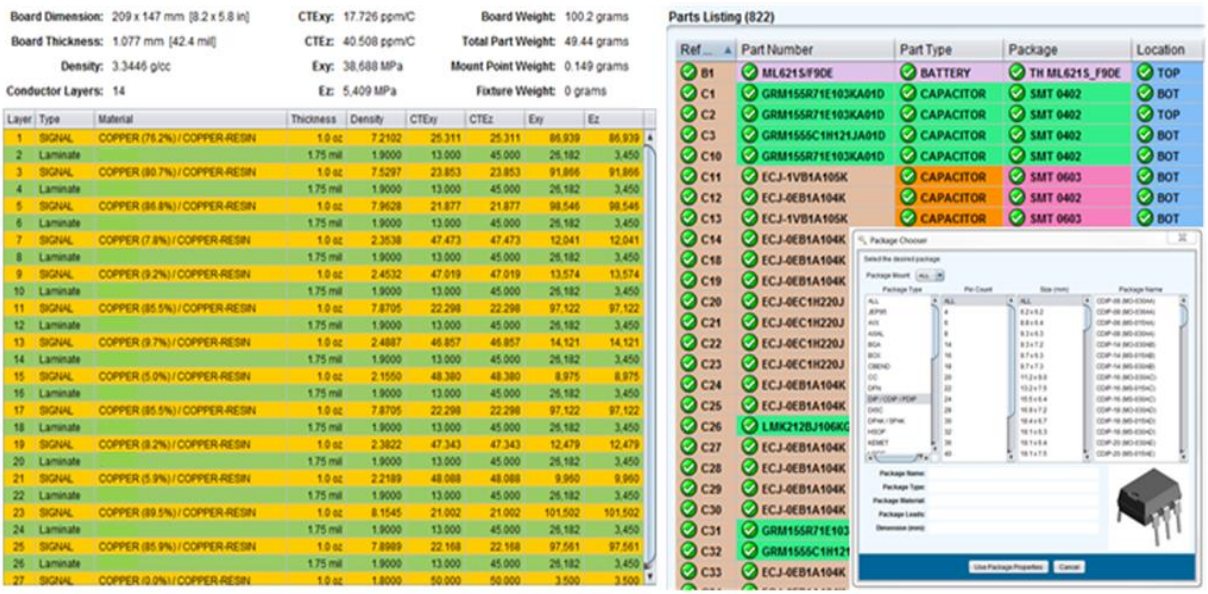

Figure 4. PCB layers and built in package manager

Case Study

The production FPGA evaluation platform was selected for the TM analysis due to design file availability and to demonstrate the capability of performing efficient analysis on a complex board assembly. The production FPGA platform consists of double sided board design with 14 active layers and has a length of 209mm and a width of 147mm. Figure 5 illustrates the board assembly along with the board layout generated by the automated design analysis software. For simplicity, the LCD located on a mezzanine layer and card assembly on the opposite side were not included in the simulation. Connecting the assembly to a chassis is enabled using six mounting points provided in the layout. Various connectors are placed on the board outline. Some of the rigid connectors can provide additional constraints on the board during thermal expansion and must be included for proper TM analysis. A total of 822 parts were modeled including connectors, active and passive components. Wire bonds were added to the simulation along with underfill to the 40x40mm FPGA with 900IO. Solder joints in the FPGA were modeled using Sn63Pb37 eutectic solder alloy elastic properties. The selected underfill CTE is 23 ppm/°C with modulus of 11GPa.

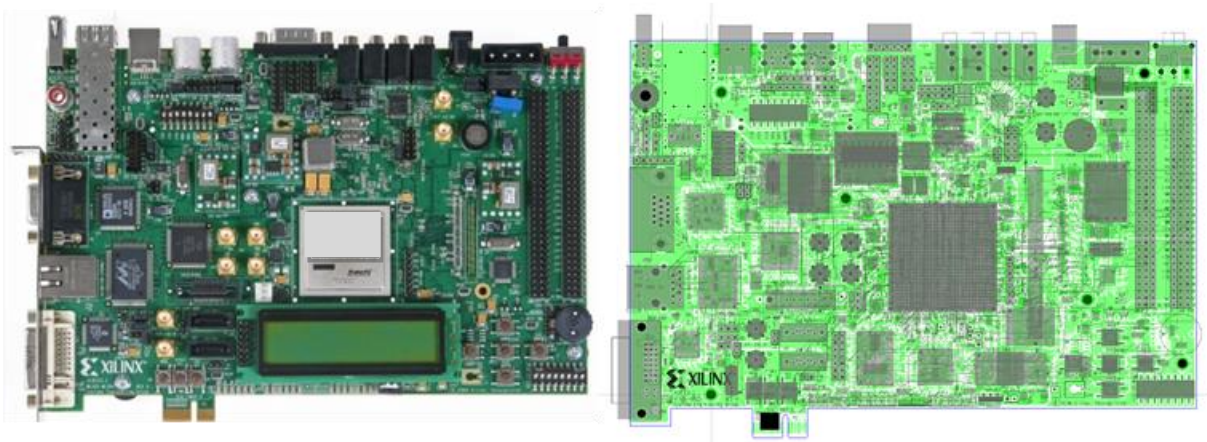

Figure 5. a) Picture of production FPGA board b) Layout of board assembly generated by automated design analysis

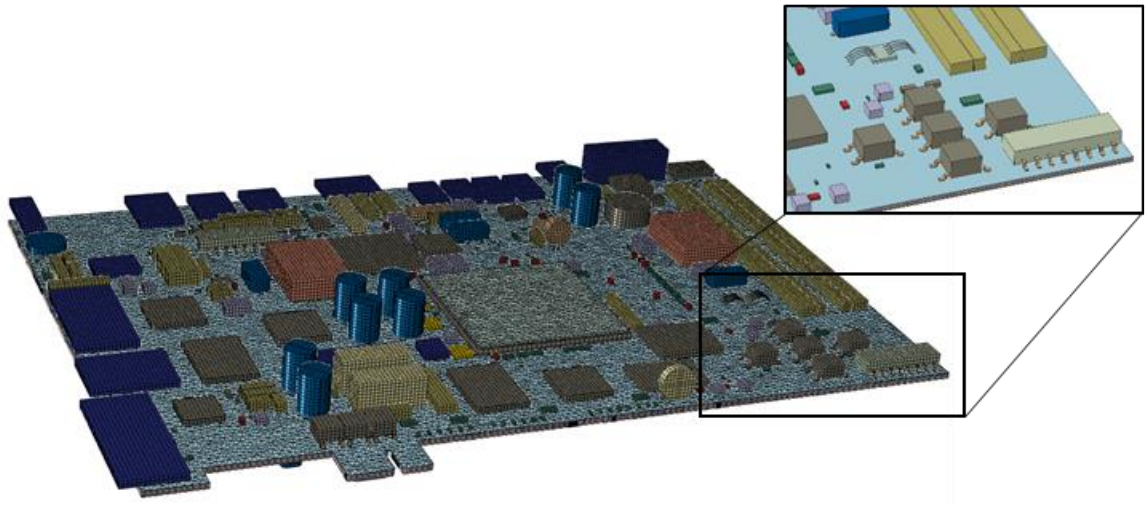

Figure 6. Fully meshed 3D model of production FPGA assembly with 2mm PCB mesh.

The software package allows meshing of three-dimensional geometries of components and leads using several element types such as solid and shell elements. First and second order elements can be selected for regions involving contact areas to reduce solve time. Automatic meshing of the entire assembly is achieved using 6-node linear triangular prism elements. This process avoids geometric redundancies and provides for consistent meshing with automatically generating the geometry of the PCB and components. Figure 6 illustrates the fully meshed model with 653,116 elements. Solder joints in the FPGA package are modeled using solid rectangular elements to avoid localized over-stiffening effects between the packages and PCB due to bending that can cause shear locking. The influences between using reduced integration and full integration elements in modeling solder fatigue have been shown to result in large differences in calculated strain [14]. Using linear solid elements offers an appropriate choice for modeling BGA solder joints while providing shorter computation time. Temperature

dependent elastic deformation of solder interconnects was used without modeling the creep deformation of the alloy. For modeling of complex inelastic behavior in solder interconnects, the PCB assembly can be generated in the software package and imported into commercial finite element software. Note that the solve time is comprised of model meshing and post processing graphical results. Mesh convergence was performed on a fully constrained board with minimum edge length of 1.5mm and package size mesh of 1mm. Solder strain decreases to an elastic strain value of 0.002 with an increase in the number of elements in the PCB as shown in Table 1. It is possible to further decrease PCB and package mesh to achieve greater resolution but at a cost of increased solve time. Solder joint strain was taken from the element centroidal value rather than the integration points. The element centroidal value is more indicative of the behavior experienced by the solder alloy in this particular simulation. Strain values in integration points at the interface of bonded mesh with large mismatch in element size could influence mesh convergence results. Figure 7 represents a close-up side view of the board assembly around the FPGA package. Both sides of the board can be seen populated with components and the PCB layers with various properties as calculated based on averaging the fraction of copper, glass and resin content on each layer. Estimating the properties of each layer is performed by an effective calculation which are then combined to provide effective PCB properties such as the Young's modulus and CTE.

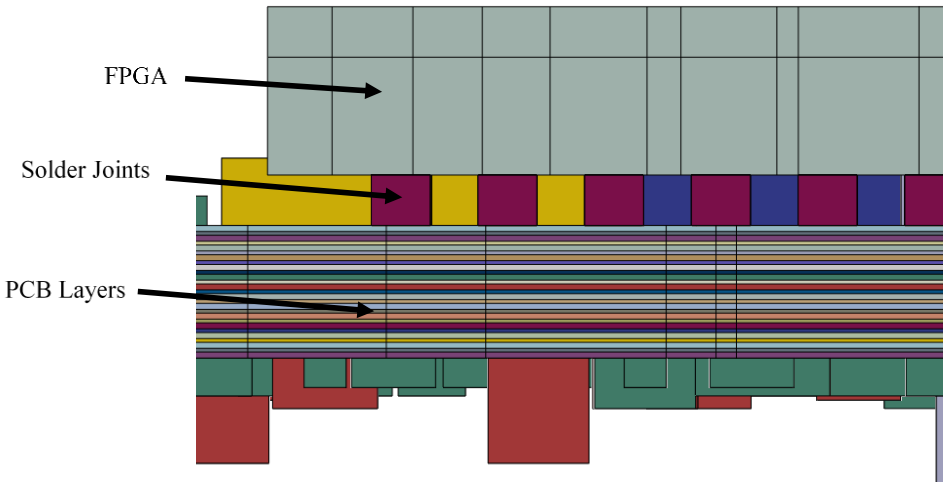

Figure 7. Close up of FPGA package showing PCB layers and solder joints.

Table 1. Influence of PCB element size on solder strain

PCB ELEMENT SIZE (MM)	MAXIMUM SOLDER STRAIN (FPGA)	NUMBER OF ELEMENTS IN MODEL	SOLVE TIME (MINUTES)
2	0.00200	649,854	177
3	0.00210	321,408	53.7
4	0.00249	204,558	32.2
5	0.00305	148,095	25.2

The boundary conditions of the board assembly were applied at mounting points constraining them while applying uniform temperature to the entire assembly. The software package provides built-in predefined mount point setting. This feature enables efficient application of desired constraint conditions to mount points directly in the layer viewer of the assembly. This feature can be used to select the type of constraint and share the interaction with the board, housing or heat sink attachments. Since standoffs of PCBs have thermal and mechanical properties, the board cannot be assumed to move independently from its mounting points. Therefore, selecting an appropriate constraint will generate realistic boundary conditions reminiscent to the ones experienced by the physical assembly. Figure 8 illustrates the predefined mounting conditions available for boundary conditions. Each boundary condition type can be assigned to a material property defined from the material library provided in the software package. Additional user defined materials can be added to the material library as needed. The difference between the types of mounting conditions is defined by the location at which they interact

with the PCB. The number of nodes at which constraints are determined is provided as user defined input and allows for closely matching the respective geometry used in the physical board. Mounting points in the production FPGA assembly were selected in order to illustrate the effect of mounting location and degrees of freedom in the boundary condition have on TM deformation.

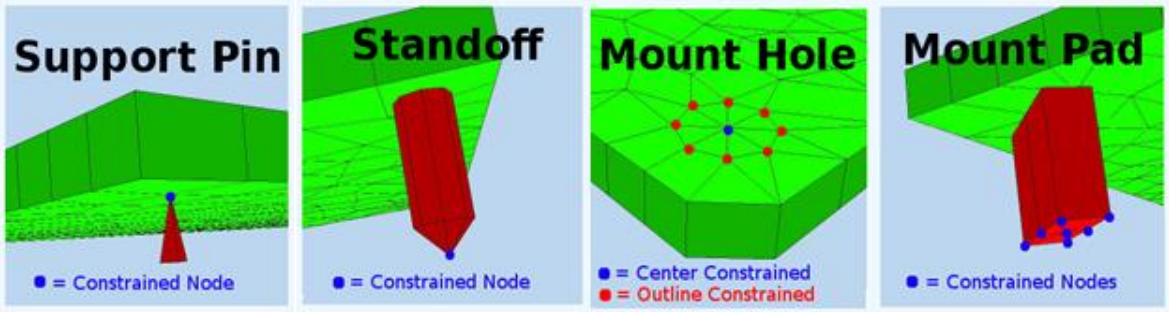

Figure 8. Predefined Boundary Conditions for mounting points.

Figure 9 shows the four PCB mounting configurations selected for the analysis. Boundary conditions 1 through 4 referenced here as BC1 to BC4 are comprised of mount hole type boundary conditions. The only variation between the mount holes is the axis constraint as indicated by the red square surrounding mount holes which are free to move in the x and y directions (in-plane).This allows for board movement during thermal expansion in the unconstrained axis similar to PCBs which utilize shoulder bolts with smaller diameter with unrestricted in-plane expansion of the PCB. Slotted holes can provide the same strain relief as shoulder bolts but consume larger PCB real estate.

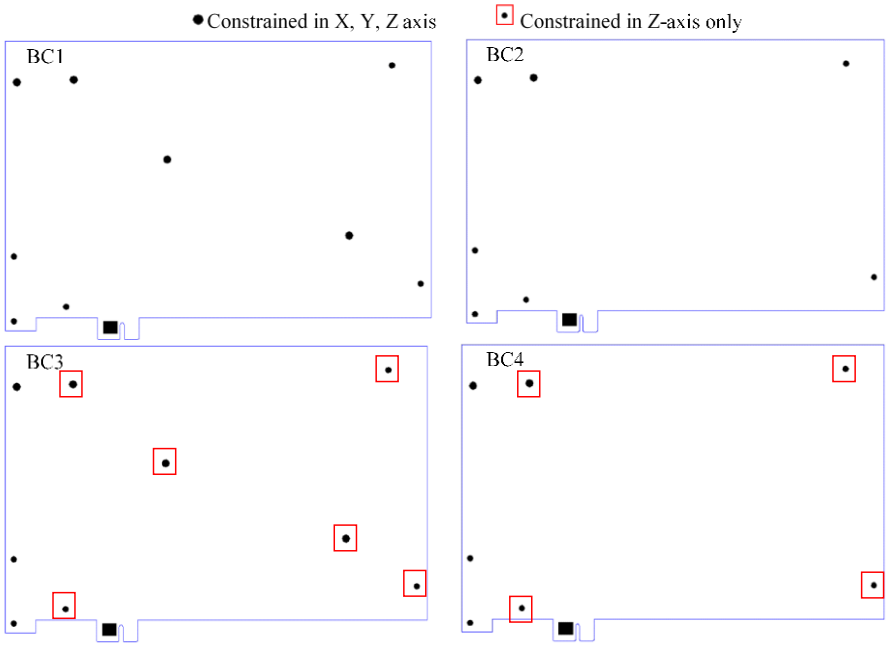

Figure 9. Boundary Conditions used for production FPGA PCB

Predicting the board deflection of the complex BGA assembly is the primary goal of the TM analysis. As previously mentioned, boundary conditions and PCB glass style and orientation can have substantial influence on the board response which will in turn influence the strain on leads and interconnects. Leaded packages are often more resilient to board warpage due to the higher compliance brought by the lead geometry compared to leadless devices. The size of the package is also a dominant factor. Large bottom terminated components are greatly influenced by gradient in PCB deflection across their geometry. The amount of warpage can dictate the type of failure these devices can experience under temperature fluctuations. At low enough temperatures, the device might only experience a strain level that will place it well within the high cycle fatigue failure probability. At moderate temperatures, the board warpage can induce substantial plastic deformation in solder interconnect, copper traces, vias and result in a low cycle fatigue failure mechanism that occurs during accelerated thermal

cycling. Worst case could be experienced under high temperature fluctuation which can induce an over-stress failure and cause device failure on the first or second thermal excursions the assembly will experience. Pad cratering is a failure mode that has been linked to both overstress and low cycle fatigue failures in electronic packages. As the FPGA package is the largest component in the assembly, it is critical to board warpage that can change between the boundary conditions BC1 to BC4. Figure 10 illustrates the equivalent board warpage for each of the PCB boundary conditions. BC1 illustrates an over-constrained configuration which restricts board warpage at all the mounting points indicated by the black circles and squares in the layout. The first copper layers of trace are superimposed on the deformation map of the PCB to emphasize the influence of mounting locations. Copper traces can be seen at low and high deformation regions and in close proximity to the mount points themselves. This can cause high localized strains surrounding mount points and potentially induce large strains in copper traces. BC3 shows reduction in the peak deformation magnitude of the PCB compared to BC1. Reduction in the peak gradient is favorable but is not always beneficial to all components as it can shift the critical location to a different area on the board. Similar behavior is observed between BC2 and BC4 with fewer mount points around the FPGA package.

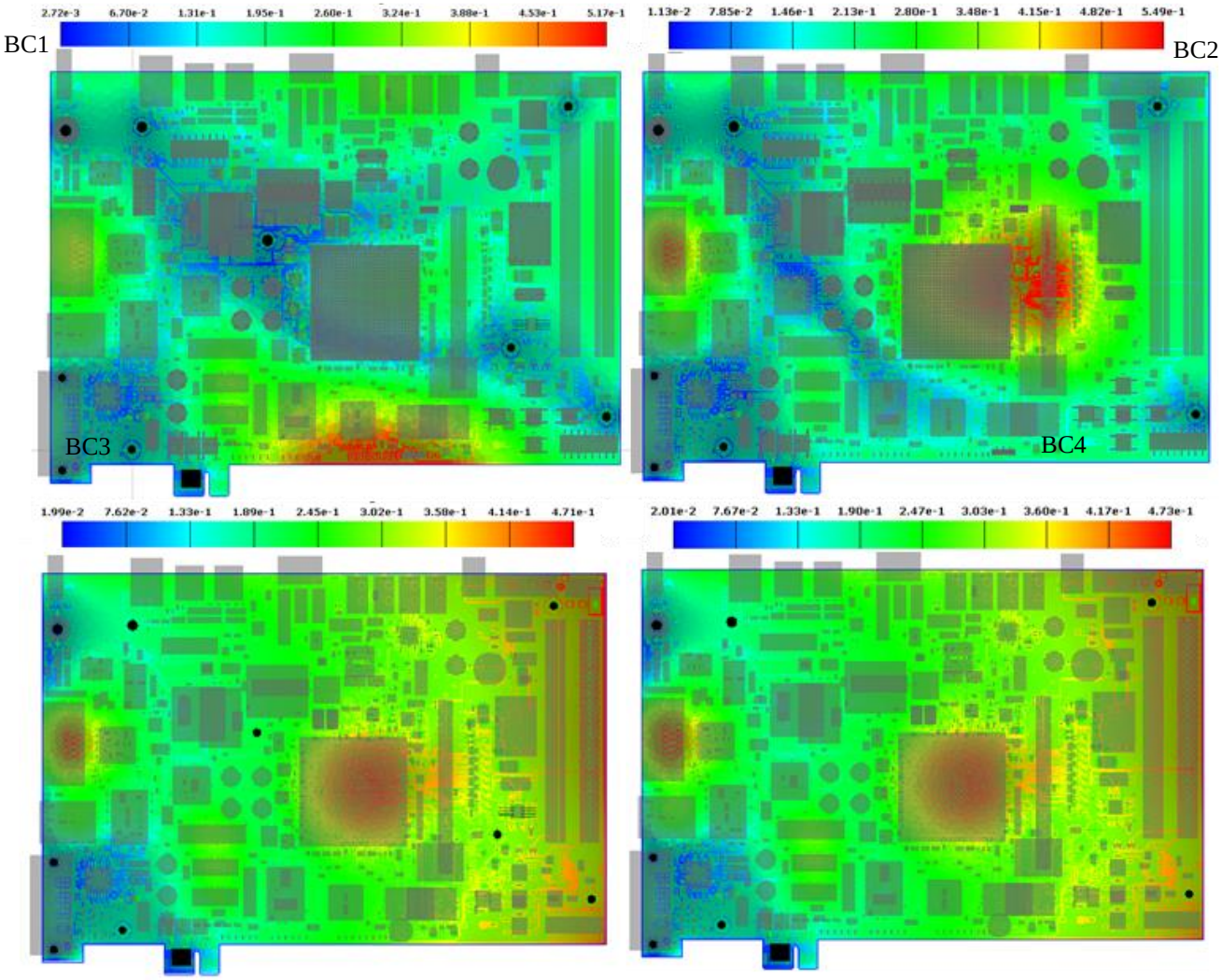

Figure 10. Equivalent board displacement at 125°C boundary conditions BC1 to BC4 superimposed on first copper layer.

The importance of performing TM analysis is to determine the interconnect strain in addition to the board response to thermal excursions. As a shift in peak board strain location can shift by altering mounting conditions, the sensitivity of components to different load magnitudes can also be affected. Figure 11 shows PCB board behavior magnitude with components using BC1 and BC3. As the shoulder bolt type constraints are added to the PCB lower PCB strain response is predicted but a higher peak deflection at the unconstrained areas of the board is observed. A shift in the critical location can be seen around the FPGA components. Looking the PCB behavior, it is impractical to determine the exact influence on 2nd level solder interconnects.

After extracting the deformation gradient across the FPGA solder joints, a larger deformation gradient can be observed across the less constrained condition of BC3. This larger deformation gradient across the package is sufficient to induce larger solder strain and shift critical joint location in the area array of the component regardless of underfill presence. Even with underfill applied to constrain the package to the PCB, the board behavior due to mounting conditions can overcome the benefit of underfills under thermal loads. Therefore, selecting proper boundary conditions should be made with consideration to known critical components in the assembly.

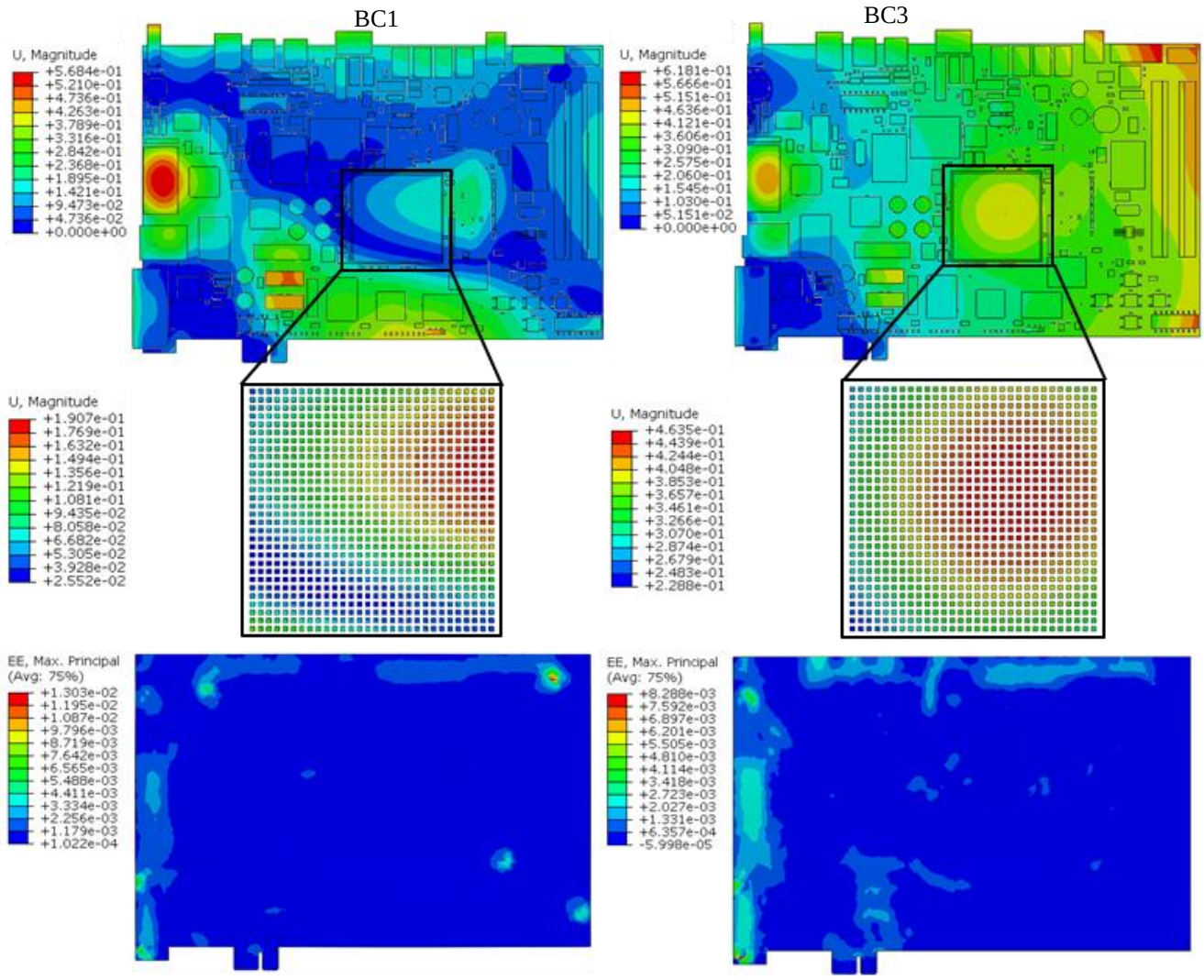

Figure 11. Equivalent board displacement, FPGA displacement and maximum principal board strain at 125°C for boundary conditions BC1 to BC3.

Conclusions

In this paper, TM analysis was performed to illustrate the importance of selecting proper PCB mounting conditions. The software package used in the analysis was demonstrated to effectively process design files into 3D models for thermal stress analysis. The built-in materials library enables accurate control of board and package material properties which greatly influence the CTE mismatch surface mount components experience under thermal loading. Boundary conditions demonstrate the influence on board displacement and solder interconnect strain magnitude. Changes in the boundary conditions can shift failure location in the board based on package specific sensitivity to applied thermal loads. Reducing PCB strain does not always guarantee reduction in solder interconnect strain magnitude. More specifically, the displacement gradient of the PCB across critical components could provide better indication of interconnect strains. Using such advanced software as the one demonstrated in this paper enables parametric study on the influence of mounting conditions during thermal loading of entire assemblies. Future analysis will include the PCB and housing interaction along with thermal gradients across the PCB. The approach presented here illustrates the importance of predicting system level analysis in the layout design process.

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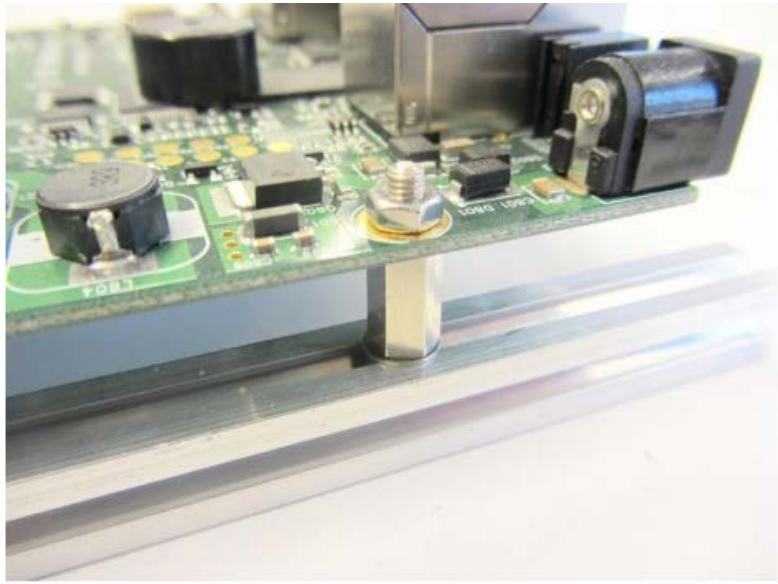
Outline

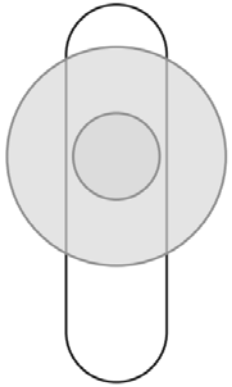
- Introduction
- Reliability of constrained components
- Over-constrained PCBs
- Practical Examples
- Over-constrained Surface Mount Components
- Case Study
- Application to Complex Designs
- Conclusion

Introduction

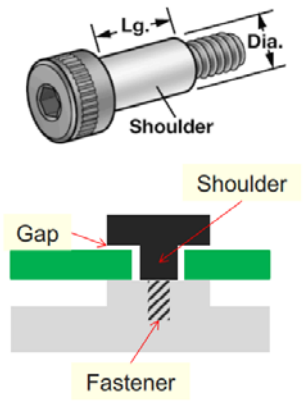
- Printed Circuit Boards (PCBs) are integrated into products using mounting points placed on layout.
- PCBs are connected to housing using bolts, fasteners and adhesives.
- These mounting points can over-constrain the PCB.
- Why should we care? What can we do about it?



Slots

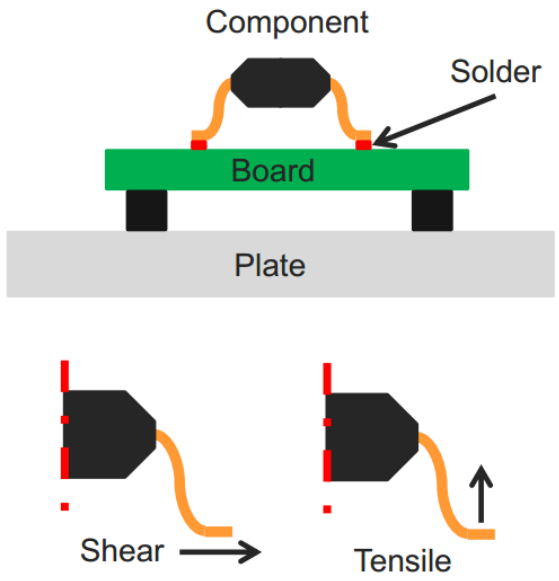


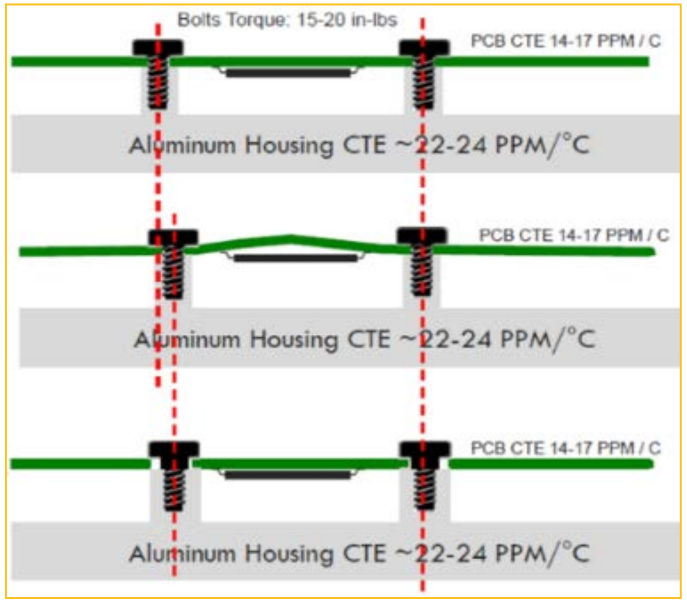
Shoulder bolts

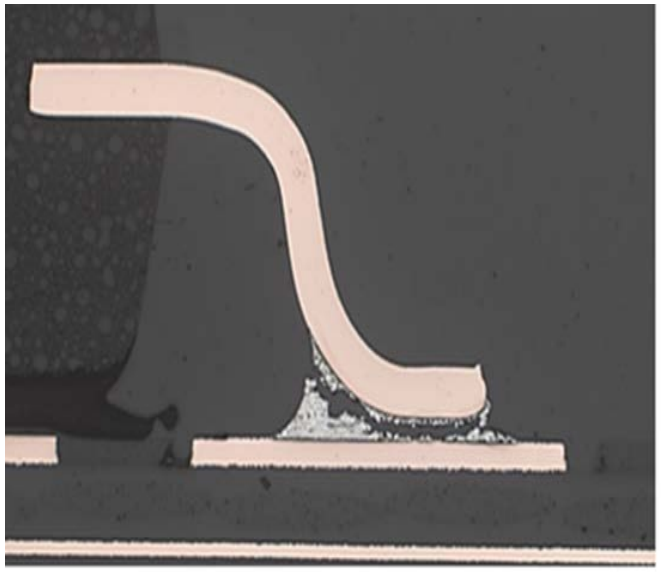


Reliability of Surface Mount Components

- Accelerated life testing of electronics focus on the CTE mismatch between the device and PCB.
- Over-constraining the PCB can change the loads interconnects experience under thermal excursions.
- Can result in lower time to failure compared to unconstrained configuration.
  - *Failure of QFP in less than 400 thermal cycles, QFN in less than 200 cycles*





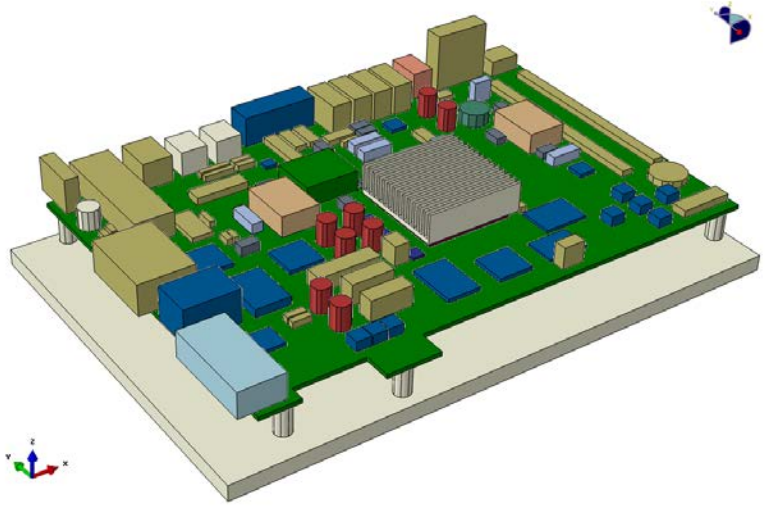


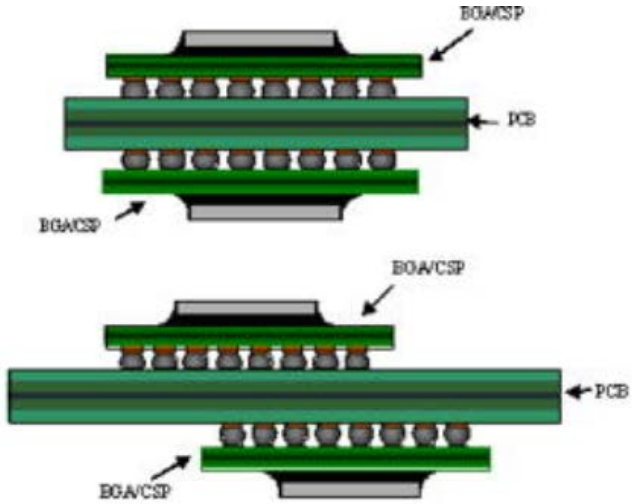
Over-constraining PCBs

- Mount points
- Heat sinks
- Pottings
- Mirroring

Affects package level reliability

Reduces overall board level system reliability

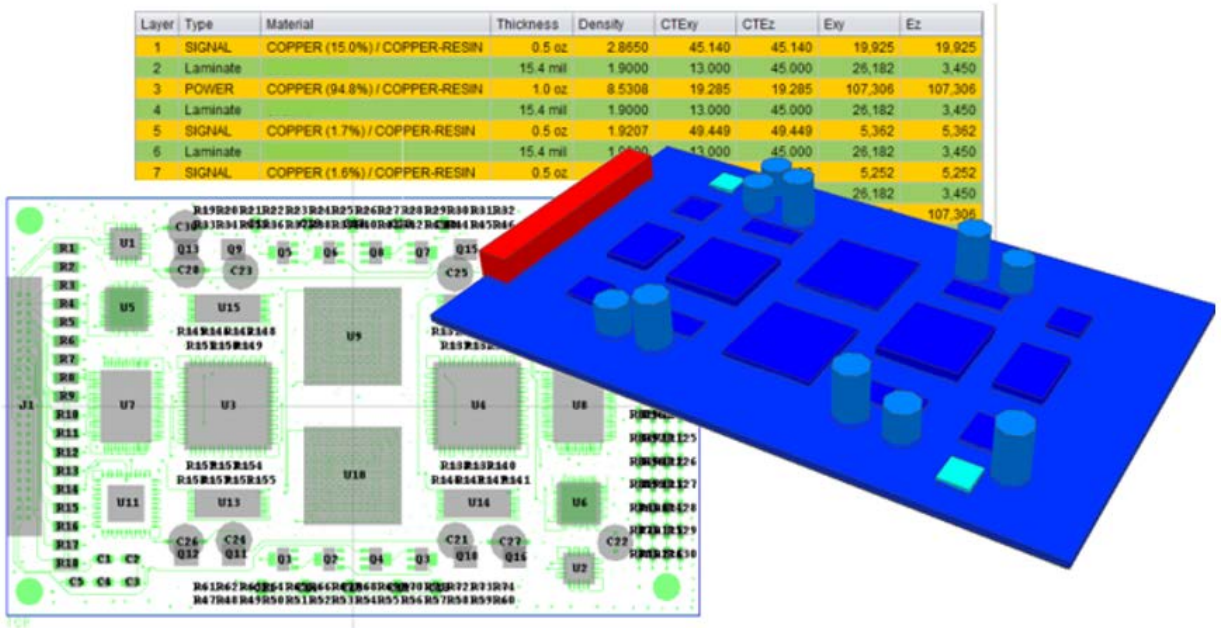




Chaparala, S., J. M. Pitarresi, S. Parupalli, S. Mandepudi, and M. Meilunas. "Experimental and numerical investigation of the reliability of double-sided area array assemblies." *Journal of electronic packaging* 128, no. 4 (2006): 441-448.

Example: Over-constrained PCB

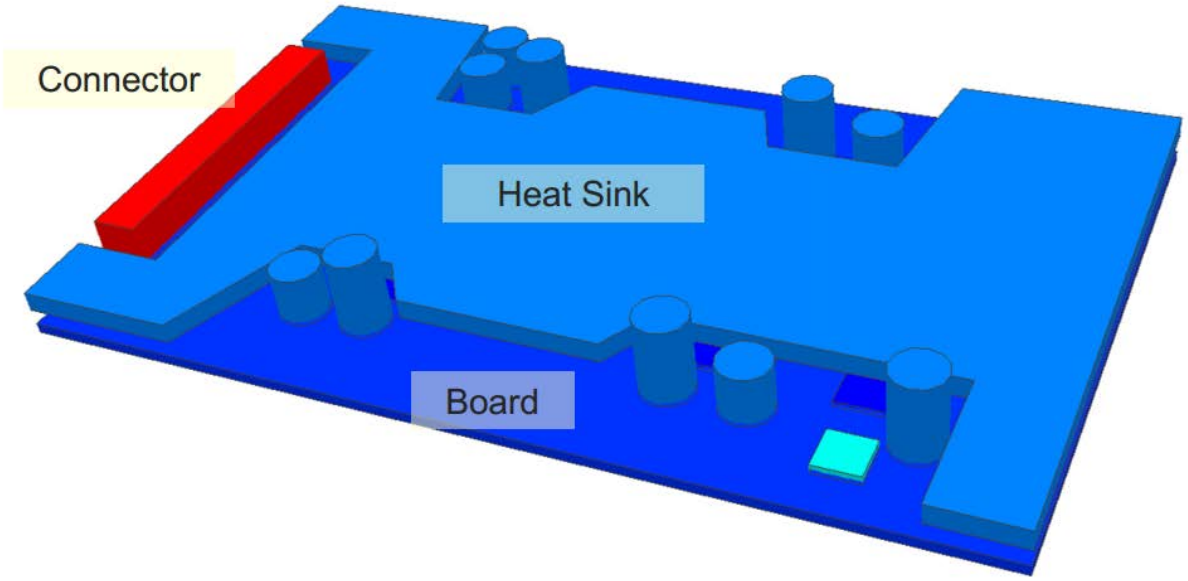
- Constrain PCB using heat sinks, mounting points.
- Perform isothermal load simulation in FEA. Start at 25°C. Strain and deformation at -40°C and 100°C.
- Example board to illustrate over-constrained conditions.

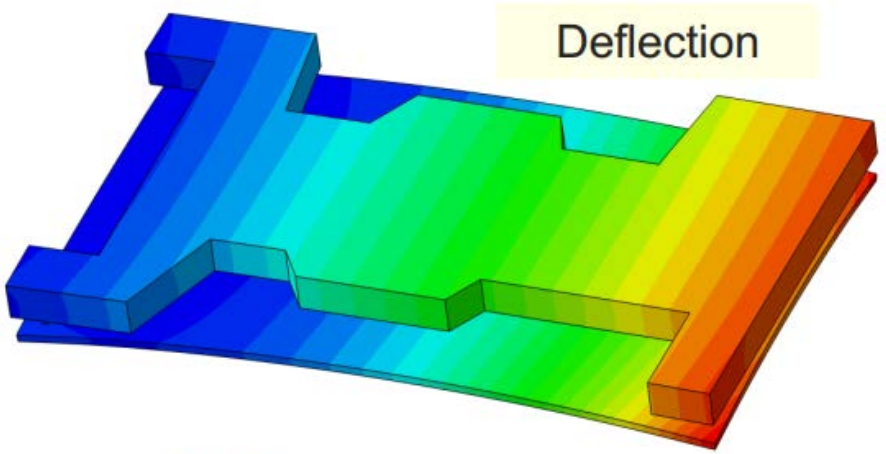


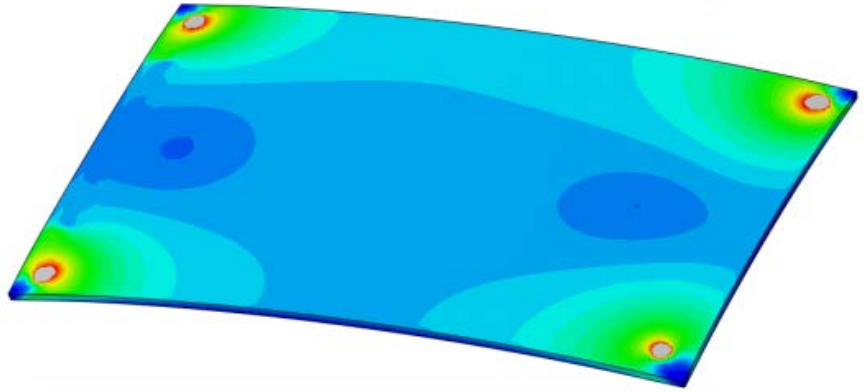
Layer	Type	Material	Thickness	Density	CTExy	CTEz	Exy	Ez
1	SIGNAL	COPPER (15.0%) / COPPER-RESIN	0.5 oz	2.8650	45.140	45.140	19,925	19,925
2	Laminate		15.4 mil	1.9000	13.000	45.000	26,182	3,450
3	POWER	COPPER (94.8%) / COPPER-RESIN	1.0 oz	8.5308	19.285	19.285	107,306	107,306
4	Laminate		15.4 mil	1.9000	13.000	45.000	26,182	3,450
5	SIGNAL	COPPER (1.7%) / COPPER-RESIN	0.5 oz	1.9207	49.449	49.449	5,362	5,362
6	Laminate		15.4 mil	1.9000	13.000	45.000	26,182	3,450
7	SIGNAL	COPPER (1.6%) / COPPER-RESIN	0.5 oz				5,252	5,252
							26,182	3,450
								107,306

Example: Board with Heat Sink

- Attach heat sink to PCB with standoff. Board supported by connector alone.
- Effective CTE mismatch is not valid for board bending
- Strain concentrated close to mount points
- Damage models cannot accurately predict solder fatigue under complex shear and bending loads



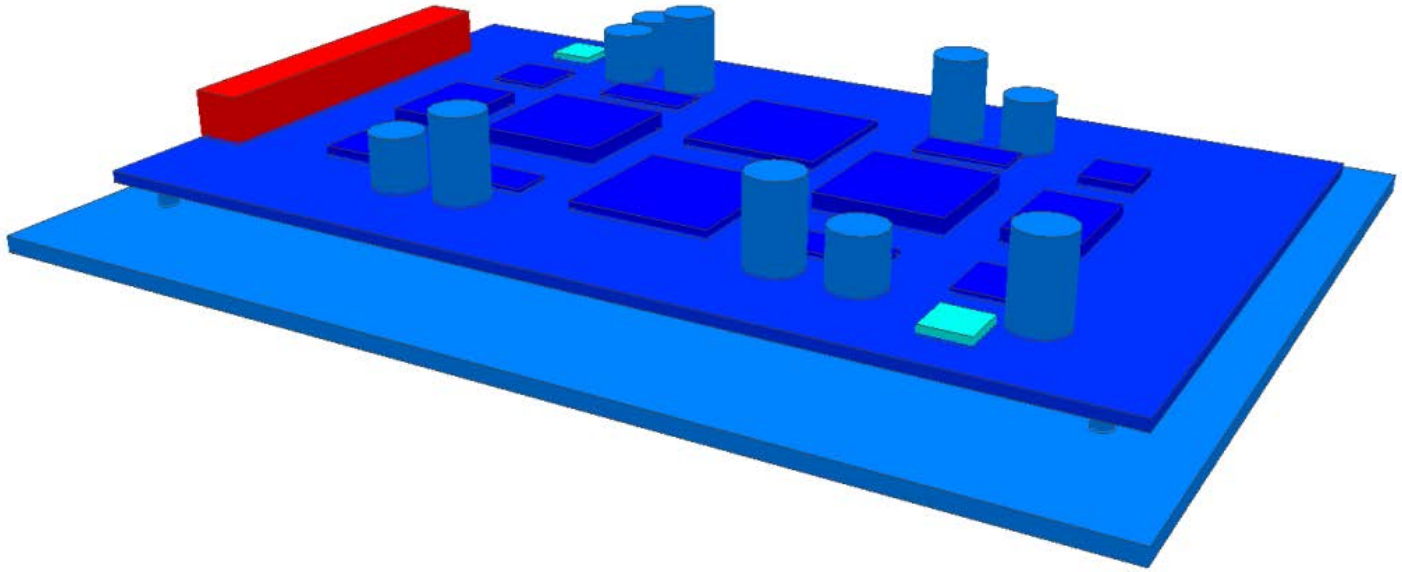


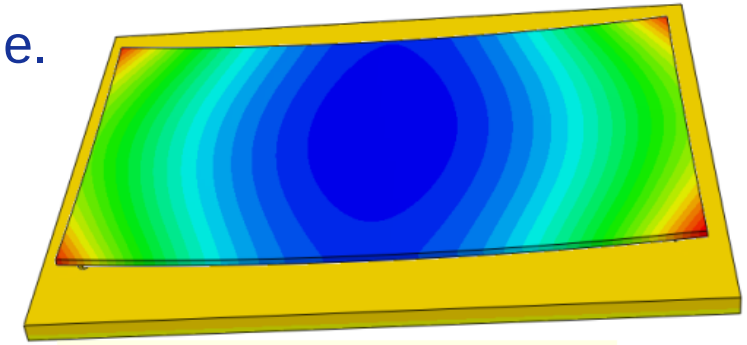


900 Max Microstrain at 100°C

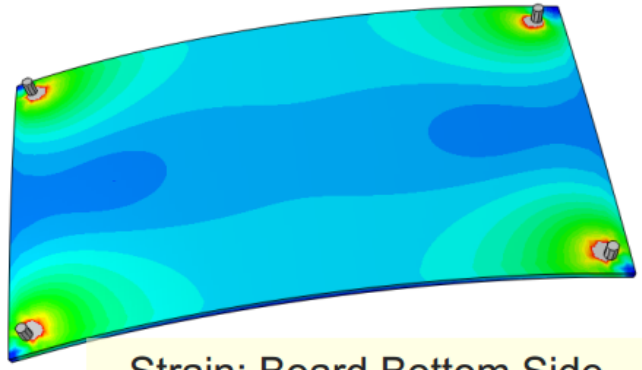
Example: Board Attached to Housing

- Board connected to aluminum plate with standoffs.
- Plate is constrained at the bottom surface (i.e. adhesives).
- Board experienced bending motion 0.3mm maximum deflection over span.
- 600 micro strain maximum. Board stretches more on the bottom side.
- Highest strain close to mount points.





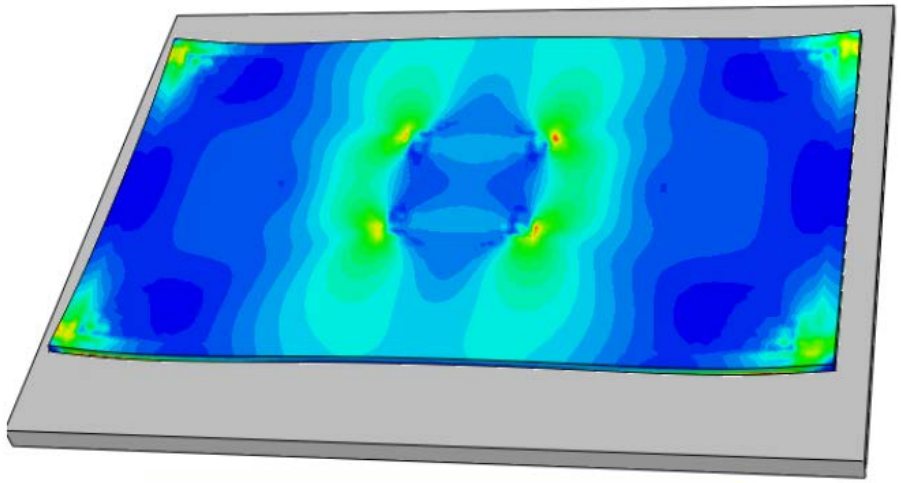
Out-of-Plane Deflection



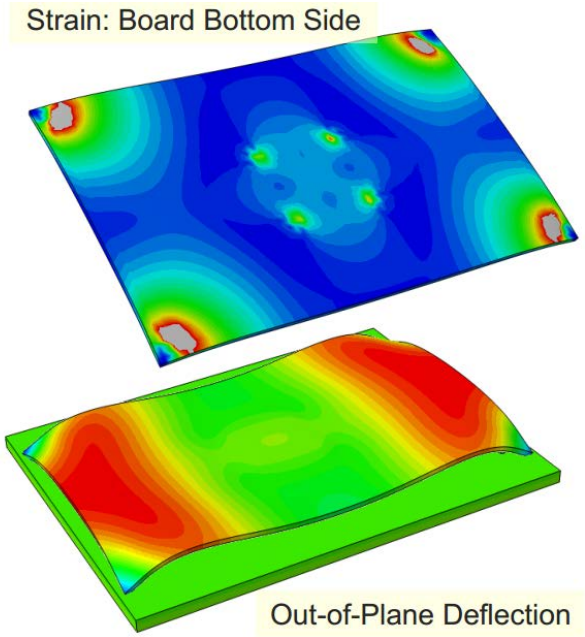
Strain: Board Bottom Side

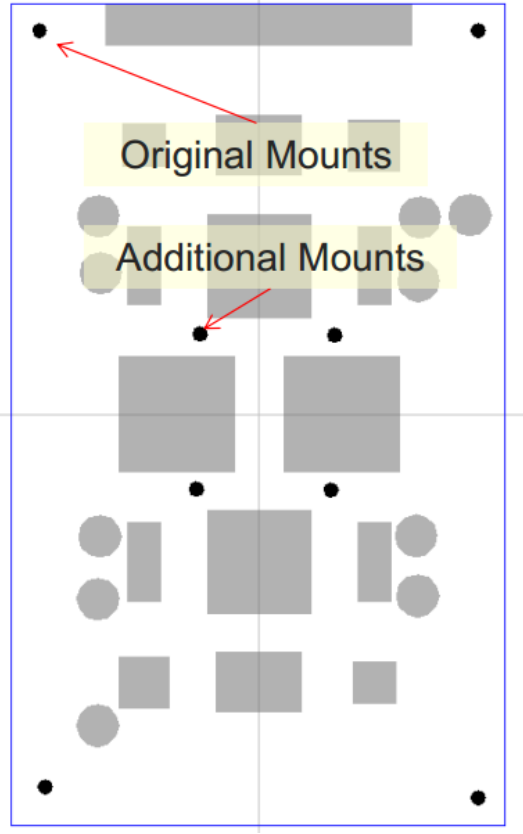
Example: Adding More Mount Points

- Additional mount points are added to prevent bending.
- Top side of the board at 100°C reaches 500 με near additional standoff.
- Bottom side of the board at 100°C reaches 700 με near perimeter of mount points.
- Out-of-plane deflection at lower temperature – board buckling
- Additional mount points do not prevent buckling mode



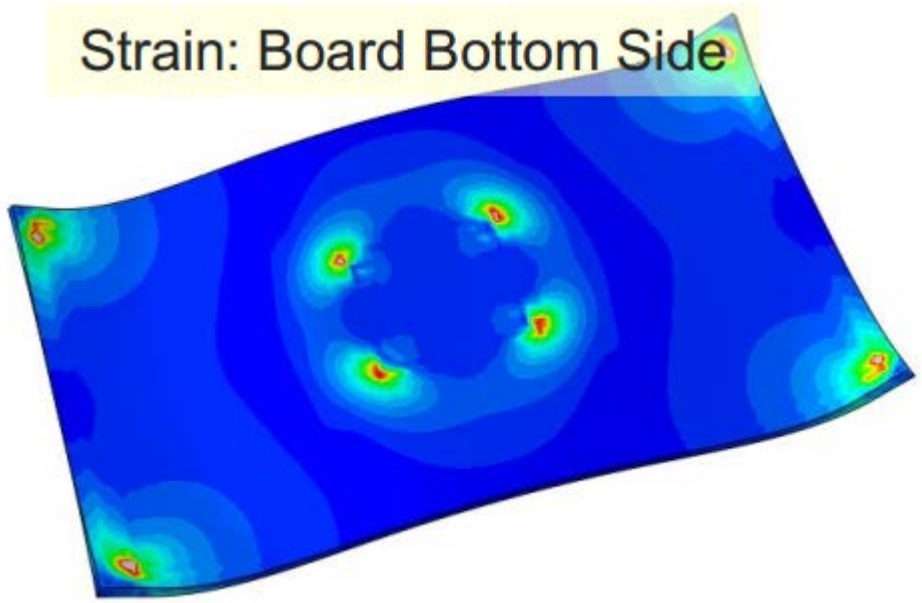
Strain: Board Top Side at 100°C

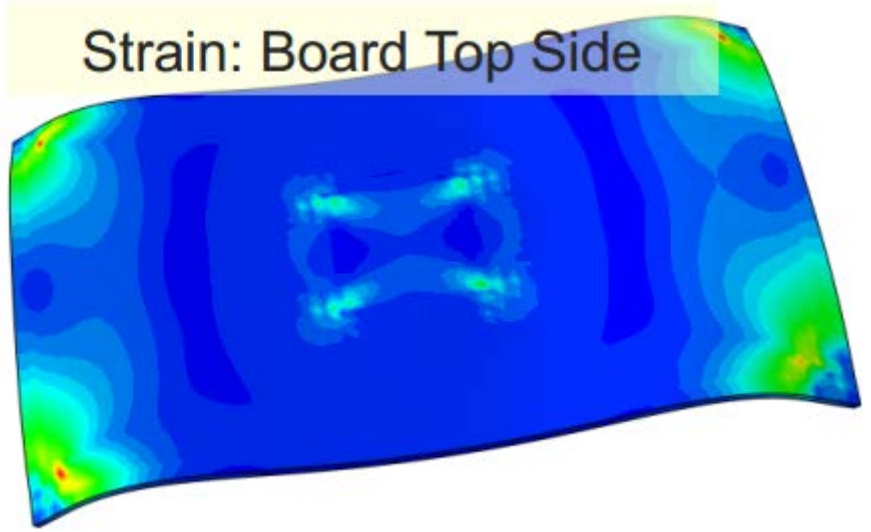




Board Buckling at Lower Temperatures

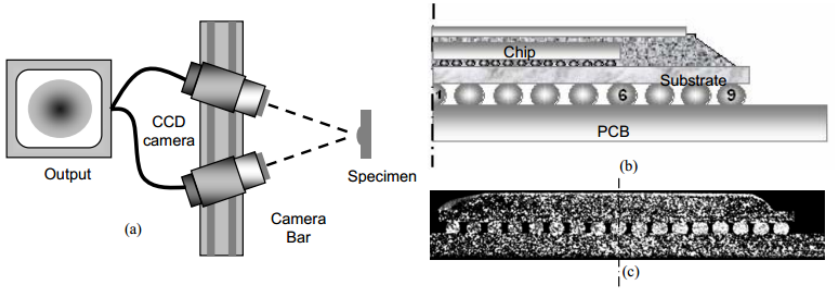
- Buckling occurs due to a higher shrinkage in the housing than the board
- Maximum deflection is 0.05mm, compared to 0.3mm with 4 corner mount
- Spans are smaller between mount points.
- Bottom side 500 με near mount points. Top side 500 με near PCB corners
- Cold temperature buckling prone to pad cratering and overstress failure



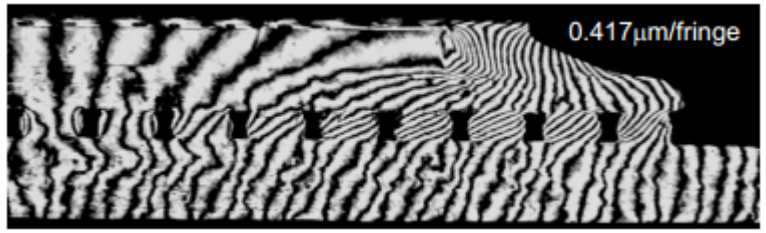


Test and Simulations

- Test for CTE
  - Attach strain gauges to board
  - Digital Image Correlation (DIC) or Moiré Interferometry
- Test for effect on component reliability
  - Temperature cycling test
  - Compare different mounting configurations
- Simulations
  - Isothermal load results for effect of mounting conditions
  - Track strain energy density in solder for life prediction



Schematic of 3-D Digital Image Correlation with cross section of test sample

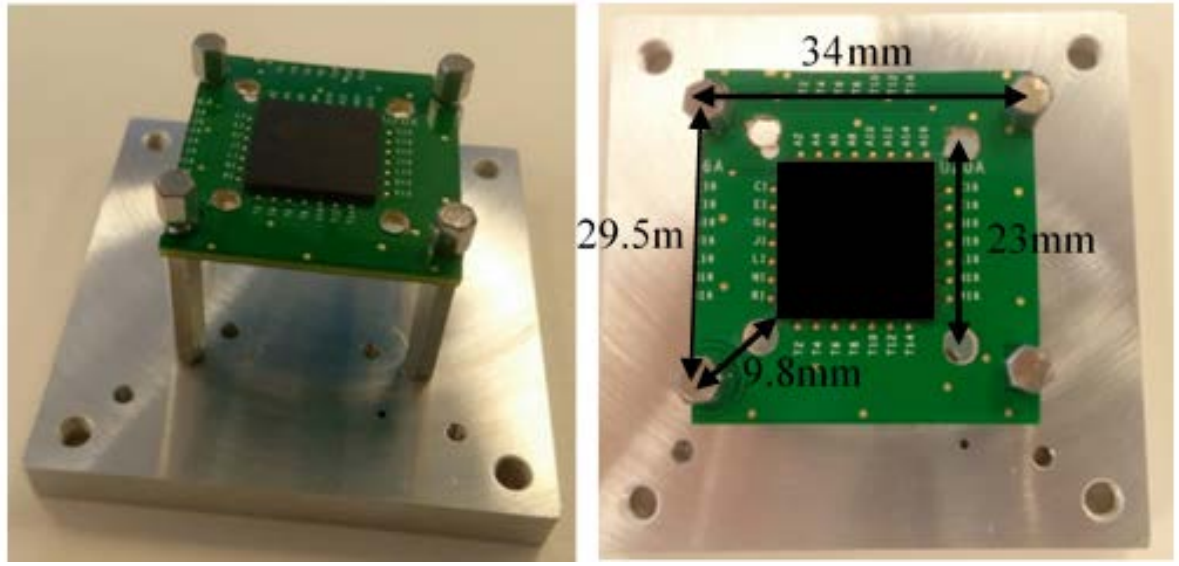


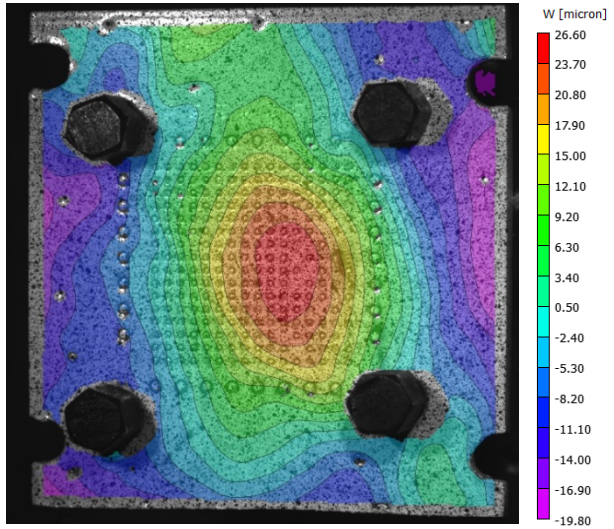
Contour plot of u deformation field of the die-shadow solder joint obtained from Moire Interferometry

Park, S. B., Ramji Dhakal, and Rahul Joshi. "Comparative analysis of BGA deformations and strains using digital image correlation and Moiré interferometry." In *Proc. SEM Annu. Conf. Expo. Experim. Appl. Mech*, pp. 1-8. 2005.

Over-constrained Surface Mount Components

- Digital Image Correlation (DIC) used to measure package and board warpage.
- Test vehicle attached using aluminum standoffs to aluminum plate.
- Standoff height can change to accommodate housing compliance.
- Aluminum expands more than the PCB contributing to PCB constrain conditions based on temperature.

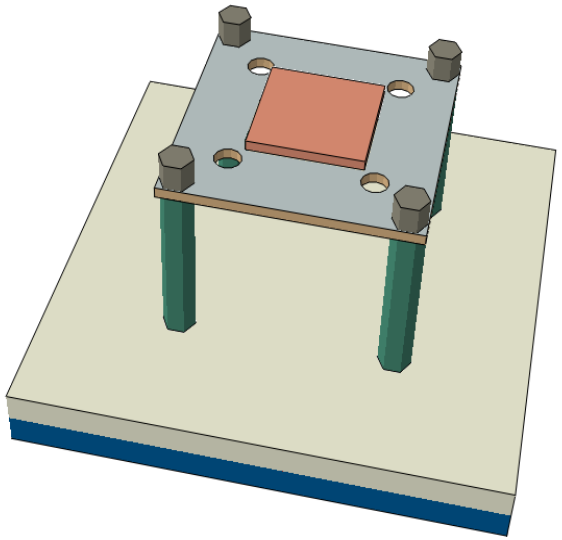


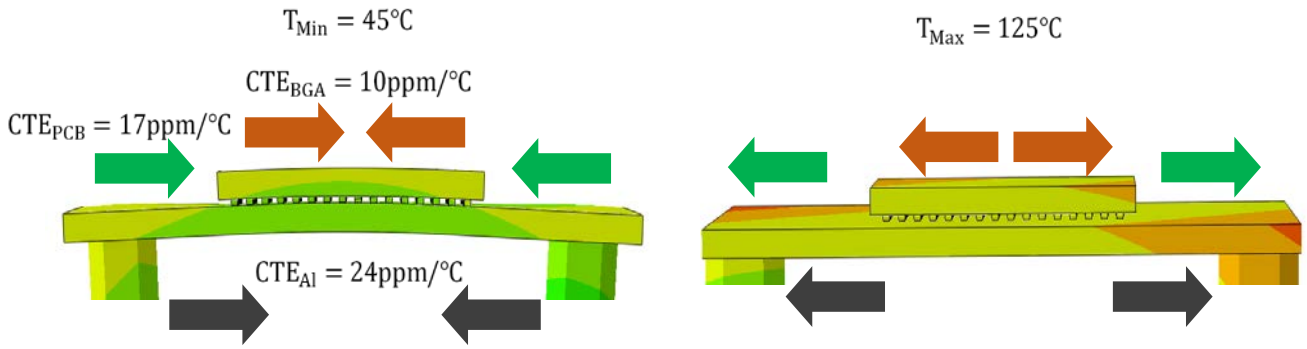


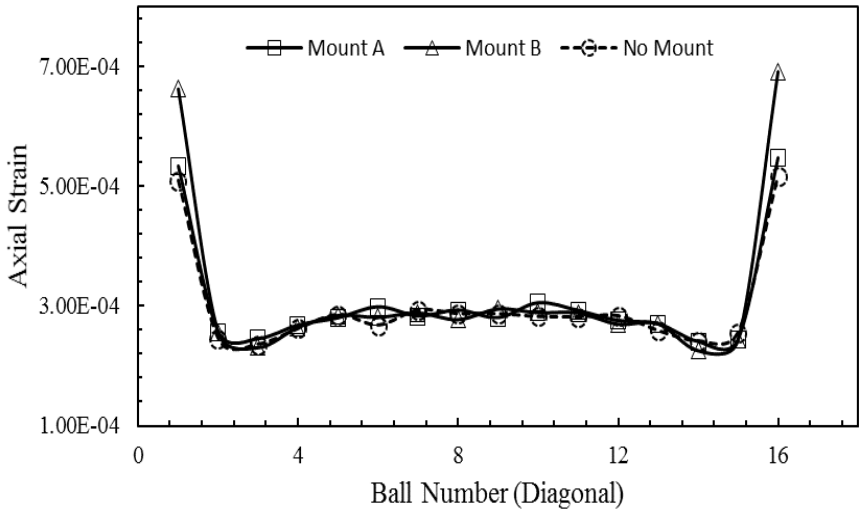
Relative out-of-plane Displacement

Over-constrained Surface Mount Components

- Aluminum stage contracts and expands more than the PCB reducing PCB warp under high temperatures.
- Lowering or increasing PCB warpage can increase load transfer to solder interconnects.
- Selecting PCB thickness can mitigate buckling under cold temperatures.

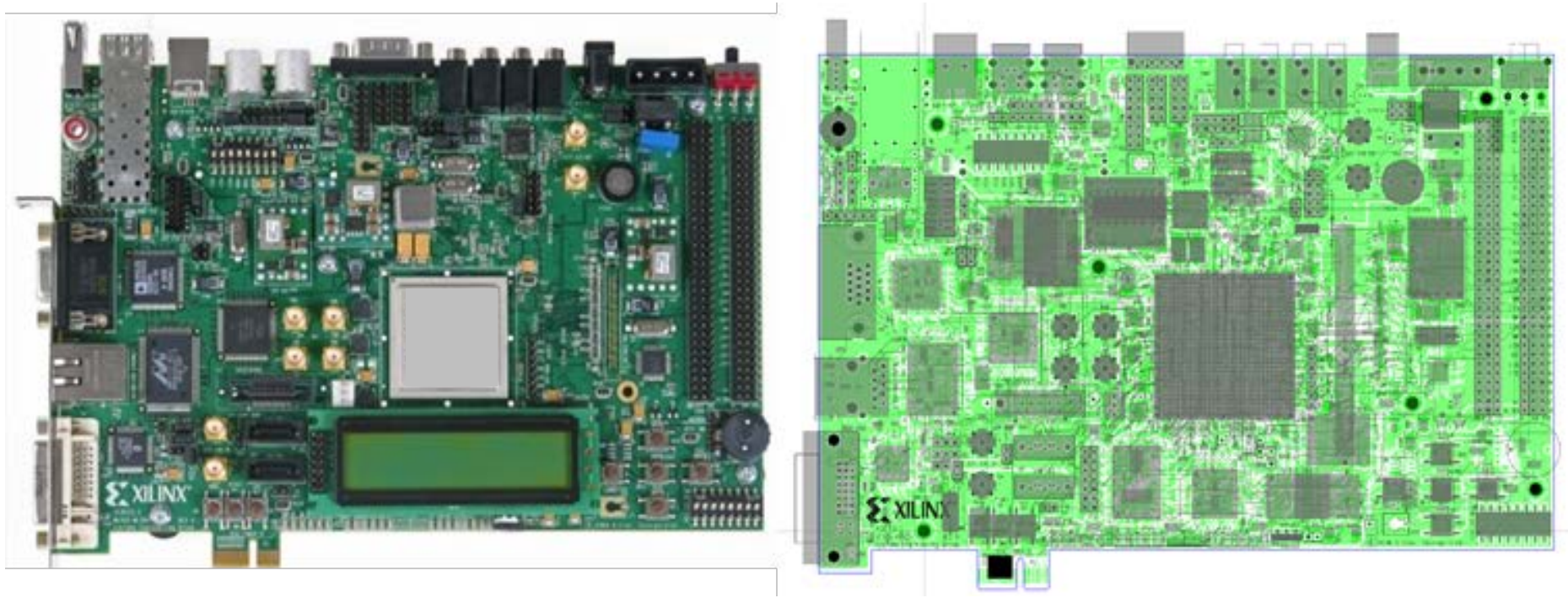






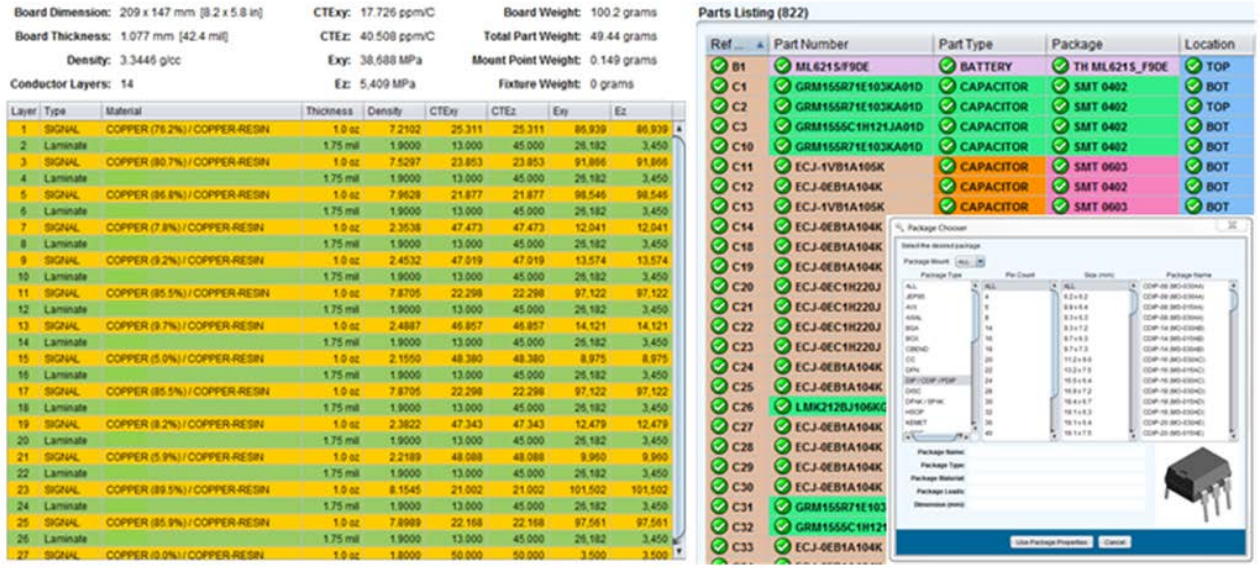
Case Study

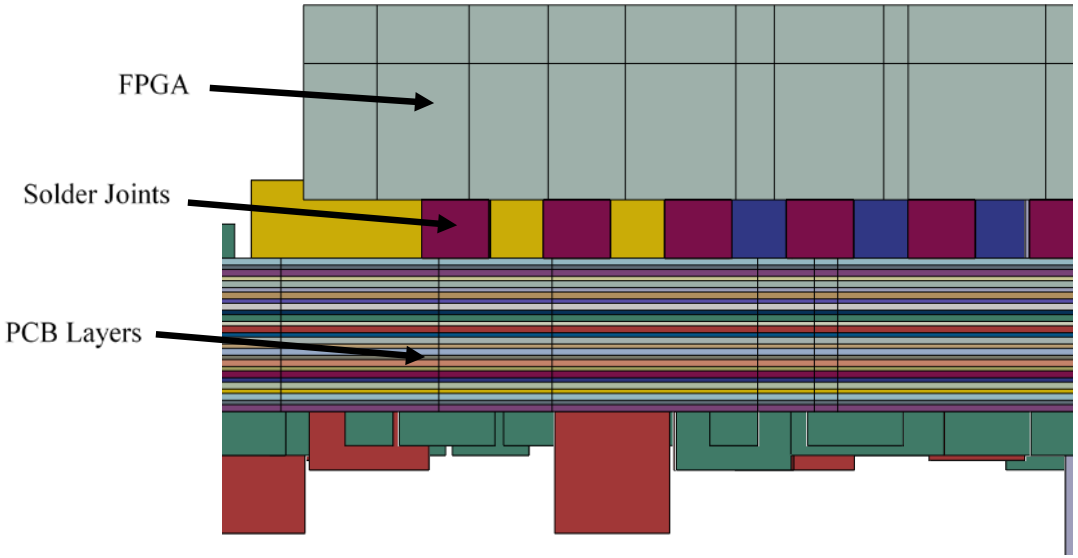
- Production FPGA board used for thermo-mechanical analysis.
- Model generated from production design files and parts list.
- Main component of the PCB includes a 900 IO 40mm FPGA.



Layout

- Stack up information provides information on each copper and resin/glass layer of the assembly.
- Software determines the weight fraction of each layer and calculates an effective property used as input in the layered model.
- Each component is automatically populated according to its location on the PCB with package specific material properties.





Reliability of Surface Mount Components

- PCB dimensions of 209 mm by 147 mm
- 822 passive and active components placed on both sides of the PCB.
- Solder joints modeled as Sn63Pb37 eutectic solder.
- Underfill of 23 ppm/°C and 11 GPa added to FPGA for analysis.
- 2mm PCB mesh size with 635,116 element in entire model.
- Solder strain converges at PCB mesh size of 2mm.

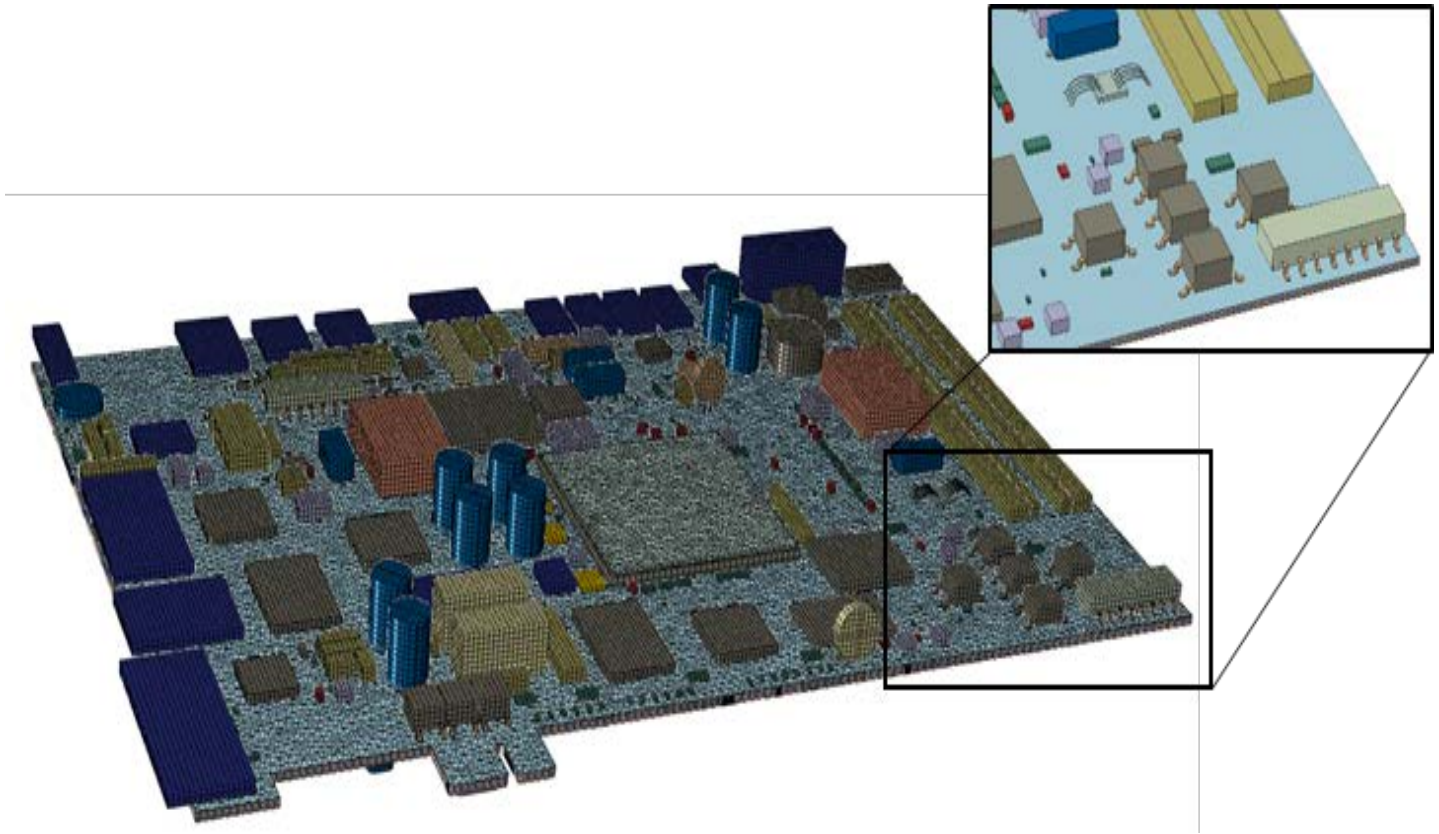
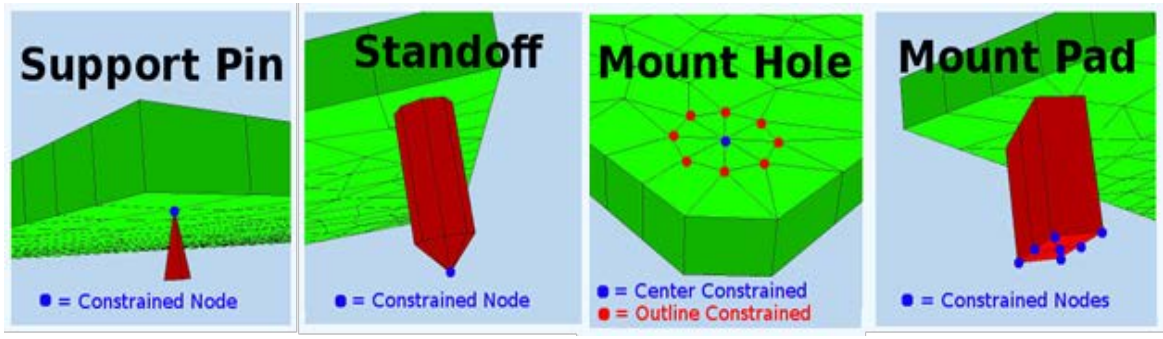


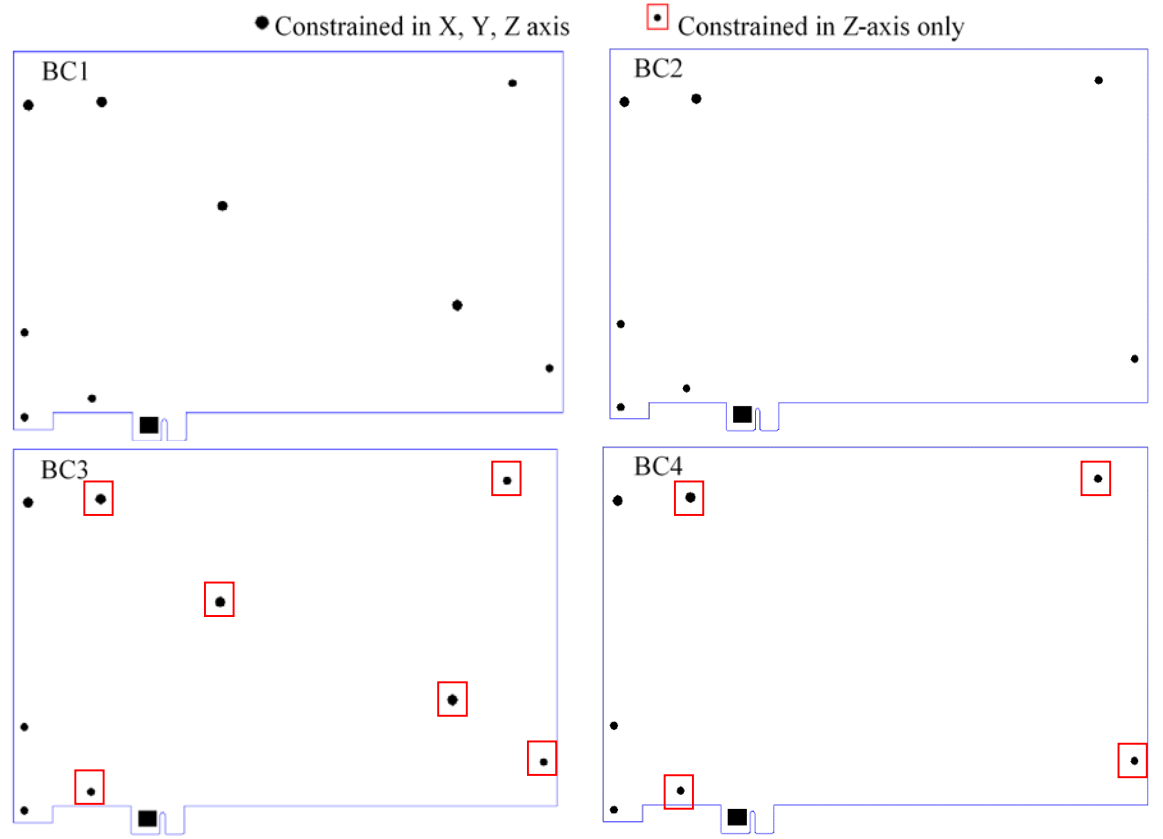
Table 1. Influence of PCB element size on solder strain

PCB ELEMENT SIZE (MM)	MAXIMUM SOLDER STRAIN (FPGA)	NUMBER OF ELEMENTS IN MODEL	SOLVE TIME (MINUTES)
2	0.00200	649,854	177
3	0.00210	321,408	53.7
4	0.00249	204,558	32.2
5	0.00305	148,095	25.2

Boundary Conditions

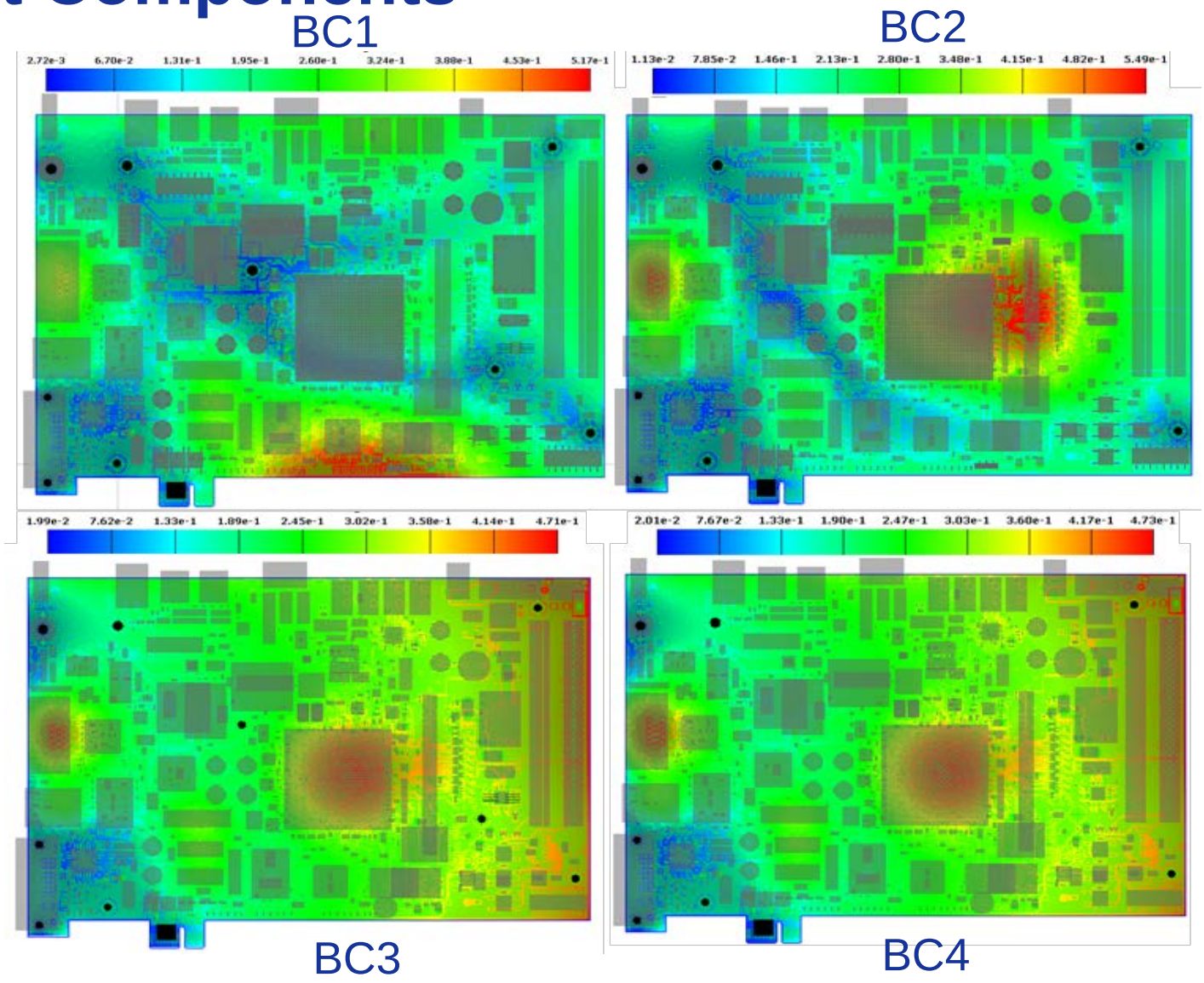
- Software provides built-in boundary conditions to suit different idealized mounting types.
- Each constraint type shape and size can be manipulated to fit necessary clamping on the board outline.
- PCB edge connectors should be modeled as fully constrained mount points as they are physically coupled to the board.
  - ***BC1:*** *9 fully constrained mount points*
  - ***BC2:*** *7 fully constrained mount points*
  - ***BC3:*** *3 fully constrained mount points + 6 shoulder bolts (free in the x-y motion)*
  - ***BC4:*** *3 fully constrained mount points + 4 shoulder bolts (free in the x-y motion)*





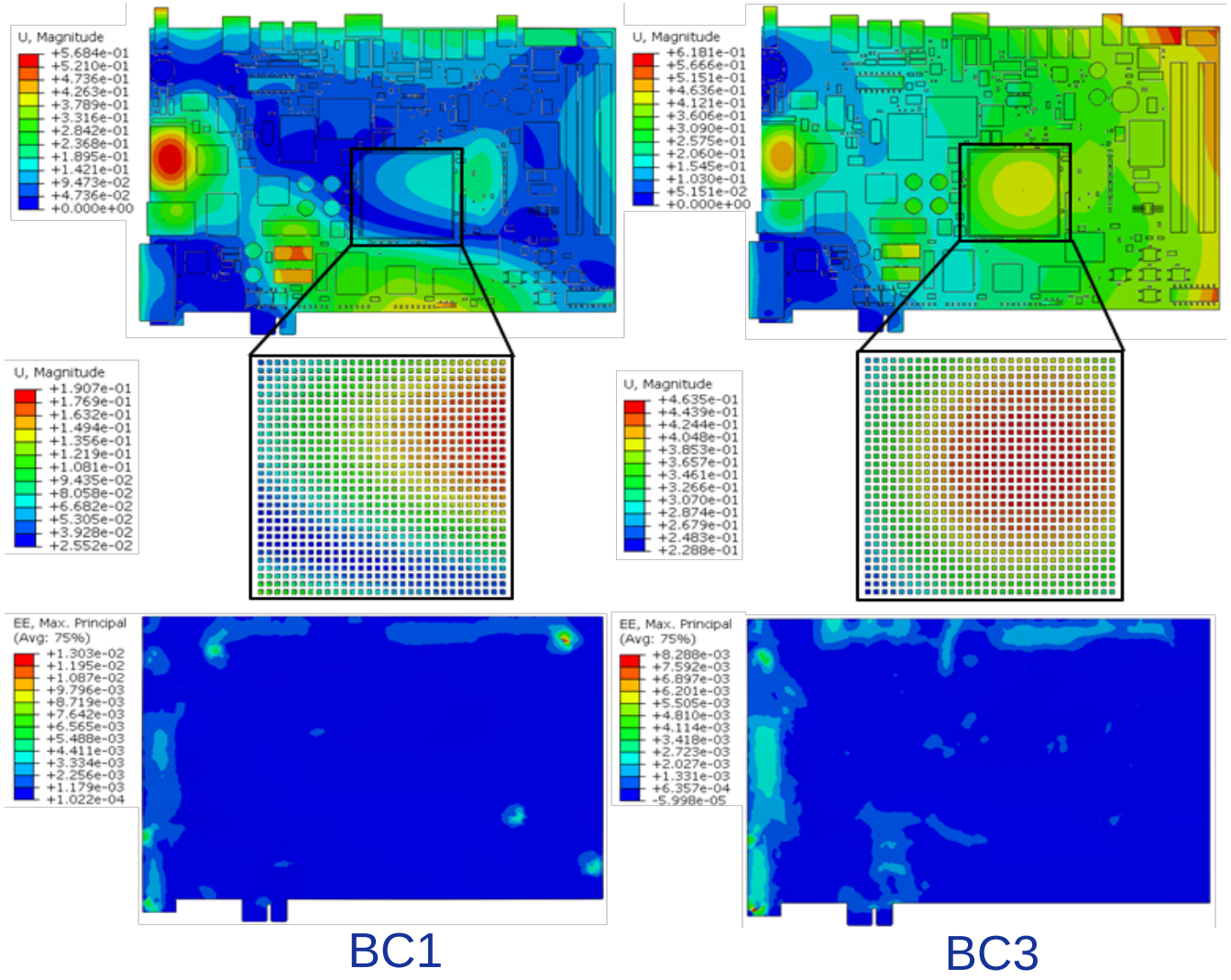
Reliability of Surface Mount Components

- Reducing the number of fully constrained mount points does not influence peak displacement as much as on shifting its location on the board.
- The fewer mounting points of BC4 have similar effect of lowering board stiffness as seen in BC3 which replaced fully constrained mount points with shoulder bolts.
- Reduced peak displacement can effectively shift the location of maximum PCB displacement to a more critical area of the board.



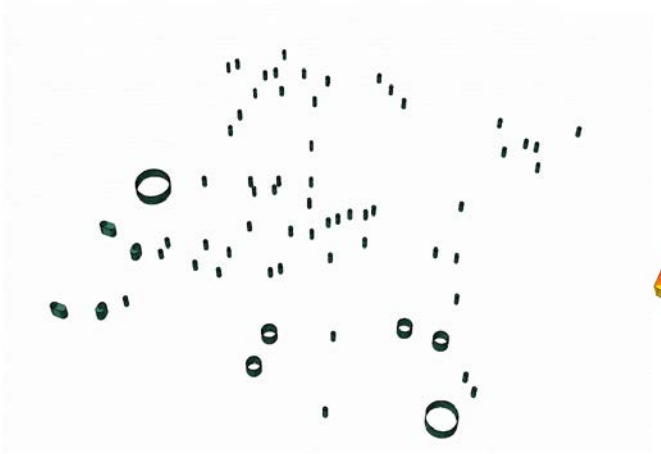
Reliability of Surface Mount Components

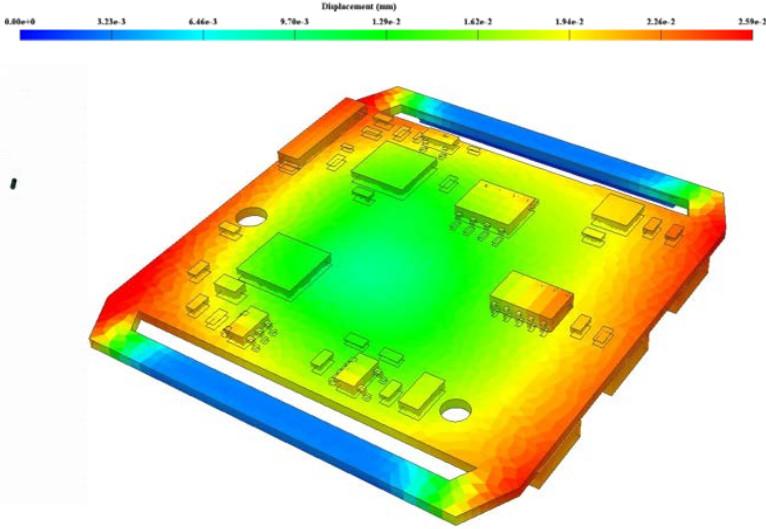
- Relative deformation contours indicate increased displacement gradient.
- Reducing mounting constraint around middle of PCB provides for increased PCB flexure due to existing perimeter mounts.
- Deformation gradient increases at the FPGA resulting in larger 2nd level interconnects strain by 19%.
- PCB warpage drives solder strain even with underfill BGA application and can shift failure location in the package.

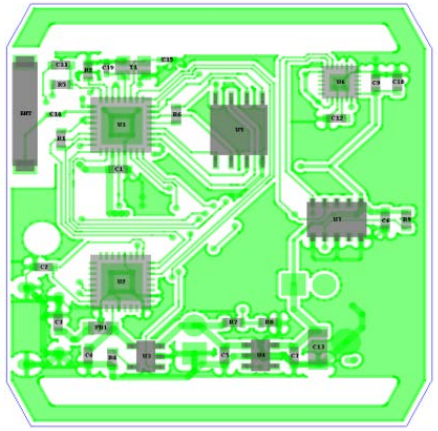


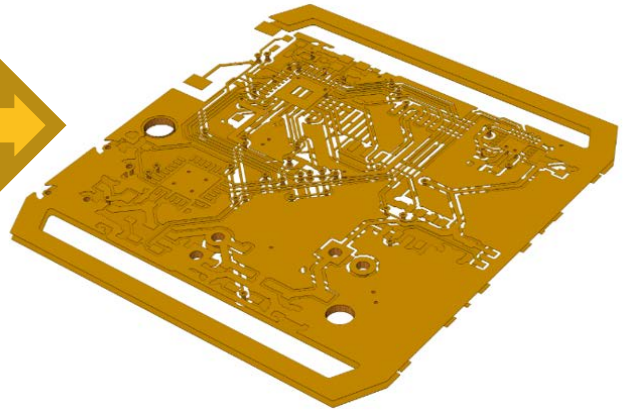
Application to Complex Designs

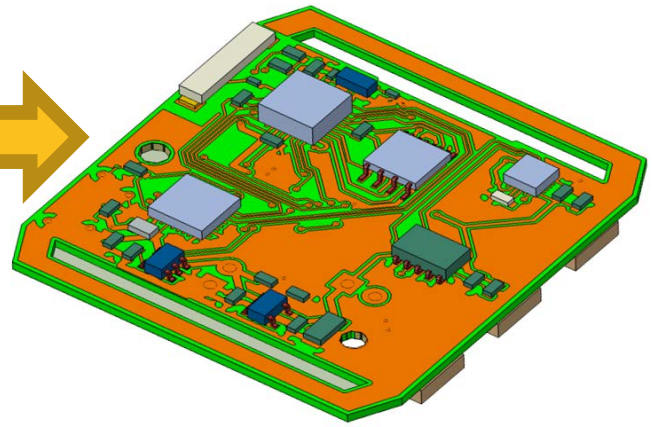
- Extend thermo-mechanical analysis to predict failure in plated through-holes, copper traces and solder joints.
- Example of a smart watch under thermal loads.
- Create and solve complex designs in ***hours!***
- Parametric study of product lifecycle.

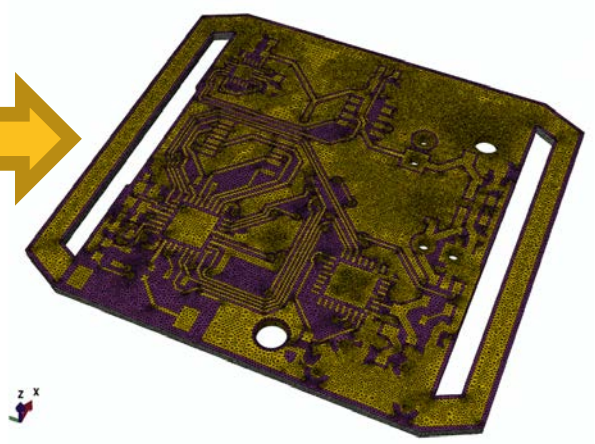












Conclusion

- Software demonstrated to perform Thermo-mechanical analysis on complex board level models generated from production design files in order to predict the influence of mounting conditions on board level and package level loads.
- Over-constrained PCBs can result in larger interconnect strain and shift critical location and subject components not previously considered to be under risk to increased probability of failure.
- PCB stack-up and mounting conditions can be optimized to reduce PCB strain in desired locations.
- Reducing PCB strain ***does not*** guarantee reduction in interconnect strain. Thermo-mechanical analysis provides details on PCB deformation gradient which enables understanding of solder joint strain.
- Housing should be coupled to PCB during thermo-mechanical analysis to determine optimal clamping points in order to reduce solder strain.

Questions?

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