A 20-Gb/s 1 : 2 demultiplexer in 0.18-μm CMOS*

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Abstract: A 1 : 2 demultiplexer (DEMUX) has been designed and fabricated in SMIC's standard 0.18-μm CMOS technology, based on standard CML logic and current-density-centric design philosophy. For the integrity of the DEMUX and the reliability of the internal operations, a data input buffer and a static latch were adopted. At the same time, the static latch enables the IC to work in a broader data rate range than the dynamic latch. Measurement results show that under a 1.8-V supply voltage, the DEMUX can operate reliably at any data rate in the range of 5–20 Gb/s. The chip size is 875 × 640 μm^2 and the power consumption is 144 mW, in which the core circuit has a share of less than 28%.

Key words: demultiplexer; latch; CML; design philosophy
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1. Introduction

Historically, high charge carrier mobility materials, such as GaAs, Si(Ge), and InP, are required for applications in optical-fiber communications with data rates beyond 10 Gb/s. Recently, however, with the rapid advances of CMOS technologies, such as continuous scaling of transistors down to the 32-nm node, more ICs for high-speed communication systems beyond 10 Gb/s, up to 40-Gb/s and even higher, have been realized in CMOS technologies. Moreover, in consideration of the fabrication cost, power consumption, and integration scale, standard CMOS technology is preferable. The fields occupied historically by high-speed technologies are gradually being occupied by CMOS technologies.

A DEMUX is an essential building block used in high-speed, long-haul optical communications or short-haul I/O interfaces to deserialize a high-speed data stream into several parallel data streams of lower speed. Based on state-of-the-art processes, a 40-Gb/s 1 : 2 DEMUX in 120-nm CMOS[1], a 40-Gb/s 1 : 4 DEMUX in 90-nm CMOS[2], a 20-Gb/s 1 : 4 DEMUX in 130-nm CMOS without inductors[3], and a 20-Gb/s 1 : 2 DEMUX in 180-nm CMOS[4] have been implemented. This paper will present a 20-Gb/s 1 : 2 demultiplexer in 0.18-μm CMOS, which is based on the standard CML logic and the current-density-centric design philosophy. It shows potential regarding low cost, a high peak speed and a broad operation range.

2. Design methodology

CMOS current-mode logic (CML) has many advantages[5], such as a small internal voltage swing, reduced time jitter and crosstalk, and good common mode suppression characteristics. Therefore, all sub-circuits of the DEMUX are designed in CML logic. Under a supply voltage of 1.8 V, the internal single-ended signal swing is generally chosen between 400 and 600 mV, in view of the tradeoff of speed and reliability.

Current-density-centric design philosophy[5, 6] rather than raditional V_{GS}-centric design philosophy was employed throughout the whole design. One of the advantages of this philosophy is the discovery of the invariance of characteristic current densities, such as the peak f_T (approx. 0.3 mA/μm) and peak f_{MAX} (approx. 0.2 mA/μm) current densities of Si and SOI n-channel MOSFETs as a result of constant-field scaling[7]. So, the constant current densities will facilitate the design porting across different technology nodes and foundries[7]. Figure 1 shows the simulated transconductance per micron of gate width as a function of drain current per micron of gate width, i.e., current density, for various V_{ds} values in this CMOS technology.

In this design philosophy, the channel width of the CML differential pair is sized relative to the total bias current, so the switching device is biased at about one-half of its peak f_T current density J_{pfT}[6].

3. Circuit design

Figure 2 shows the block diagram of the 1 : 2 DEMUX. It

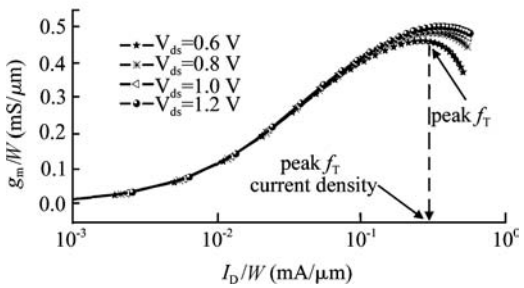

Fig. 1. Simulated transconductance per micron of gate width as a function of the drain current per micron of gate width for various V_{ds}.

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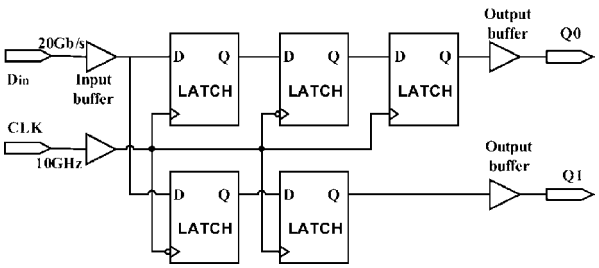

Fig. 2. Block diagram of the 1 : 2 DEMUX.

is composed of two input buffers, two output buffers, and five latches, which form the core of the DEMUX cell. In this architecture, the input data and clock signal are first amplified and reshaped through each input buffer. Then, they enter the DEMUX core. Finally, each output data signal from the DEMUX core is amplified, reshaped, and buffered by each output buffer.

3.1. Data input

The data input buffer in a DEMUX is the highest speed portion of the whole circuit. It isolates the circuit core from the outside, and provides the core with a high-quality input signal to insure the proper operation of the IC, by amplification and reshaping. So, in some sense, a DEMUX is half-baked without input buffers.

However, the introducing of the data input buffer brings along many problems, such as power consumption, chip area, and even restricted speed performance[3, 8]. Among them, the reduced speed performance is an important reason why some ICs do not have data input buffers. For example, Reference [3] mentions that owing to the bandwidth limitation of the input buffer, the supply voltage must be lifted from 1.2 to 1.5 V in order to reach a data rate of 20 Gb/s.

Usually, there are two to five stages in a high-speed data input buffer[2, 8, 9]. A two-stage buffer is adopted in the circuit. There exists a tradeoff between power consumption and speed. Under a constant current density biasing and a constant voltage swing, the current can be increased by making the load resistors smaller. While increasing the power consumption, it will, at the same time, decrease the time constants at the output nodes; thus, higher speeds can be achieved. However, such an improvement cannot be obtained without limits, because to increase the current, the transistor size has to increase, leading to a bigger capacitance at the output nodes.

Owing to the restriction of the low supply voltage, broad bandwidth techniques, such as cascode and cherry-hooper, cannot be applied. So, the shunt inductive peaking technique is introduced to enhance the bandwidth for the highest data speed.

A larger inductor (L) gives a larger bandwidth extension but poorer pulse fidelity, whereas a smaller L yields less bandwidth improvement but better pulse response[10]. How to decide depends on circuit requirements or tradeoff. Here, the maximally flat frequency response is preferred, which will improve the bandwidth by over 70%. A pair of 1.2 nH inductors is used.

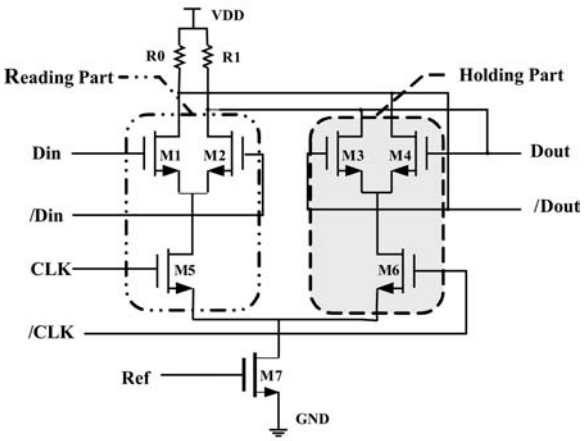

Fig. 3. Latch circuit.

3.2. Latch

Just as in any sequential logic circuit, the latch plays a vital role in the DEMUX. It determines the timing and function of the whole circuit and affects the achievable speed range and the power dissipation. Owing to the advantages mentioned above, today, the CML latch and its variations prevail throughout high-speed latch designs in any technology.

The prevailing latches can be generally categorized into four groups, where the topologies involved with passive elements, such as inductors and transformers, are not included. The four groups are:

I. The standard CML latch[1].

II. The pseudo-differential latch, where the tail current source is removed[11].

III. The parallel-current-switching (PCS) configuration[12] and the folded CML latch[13], where the clock switching pairs are folded and parallel with the data switching pairs.

IV. The dynamic loading latch[14], where the clock switching pairs are in common gate configuration and the loads are dynamically controlled.

Except for the standard CML latch and the folded CML latch, other latches suffer from shortcomings, such as more jitter, crosstalk, and worse common mode suppression characteristics. Moreover, the PCS latch and the folded CML latch exhibit a lower speed than standard CML latches[12, 13].

At the same time, according to the relative size between the holding differential pair and the reading differential pair, as shown in Fig. 3, these latches are also divided into two: static and dynamic. When the former is smaller than the latter by a certain fraction, the latch is regarded as dynamic[3, 15, 16]; otherwise, it is called as static[1]. It is generally believed that the dynamic latch can obtain higher speed. However, this is achieved at the expense of narrower operating range and worse internal waveforms. Furthermore, worse waveforms usually occur with a worse S/N ratio and a larger jitter, which usually are improved by adding a buffer after each latch at the expense of a higher power consumption[3]. In addition, these latches can be biased by one current source per latch[4], or by coupling two latches where the two pairs of reading switching transistors and two pairs of holding switching transistors are

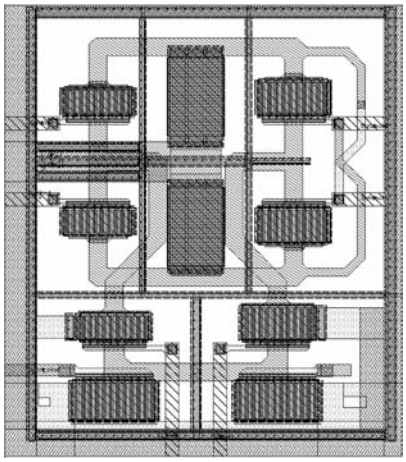

Fig. 4. Layout of the latch.

biased independently[1, 3, 14]. However, the latter will generally result in a redundant latch, which will increase the power consumption[3].

Based on the reasons mentioned above, these alternatives are weighed and the standard static CML latch is selected for the DEMUX, where each latch is biased by a current source. The optimum gate width ratio of 3 : 4 between the reading and holding pairs and the loads of 100 Ω are determined by calculation and optimization.

3.3. Output buffer

Usually, there are two to four stages for high-speed data output buffers. Usually for two-stage buffers, the inductor peaking technique is implemented to improve the bandwidth of the buffer[1]. As a trade-off between the area and the power consumption, the output buffer is composed of three-stage differential pairs, which is a tapered CML buffer chain. It is readily proven that the minimum delay is obtained by dividing the delay equally over all stages, which can be realized by gradually scaling up all stages with constant taper factor[17].

To satisfy the current switching requirement, the voltage swing of the former stage must exceed the maximum input differential voltage of the following stage[17]; i.e.

$$R_{\mathrm{D1}} I_{\mathrm{SS1}} \geq \sqrt{\frac{2I_{\mathrm{SS2}}}{\left(\mu_{\mathrm{n}} C_{\mathrm{ox}} \left(\frac{W}{L}\right)_2\right)}},$$

where μ_{n} and C_{ox} are the average electron mobility in the channel and the gate oxide capacitance per unite area, R_{D1} and I_{SS1} are the load resistor and the tail current of the former stage, I_{SS2} is the tail current of the following stage, and $(W/L)_2$ is the ratio of the width (W) and the length (L) of the channel of the following stage.

In addition, a pair of 75-Ω matching resistors are adopted as loads.

4. Layout and Implementation

Figure 4 shows the layout of the latch, which measures 50 μm by 57 μm. According to this figure, symmetry is also held inside the cell as far as possible, by dividing the tail current source transistor into two identical transistors.

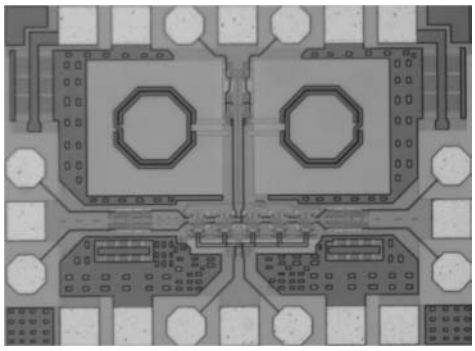

Fig. 5. Chip micrograph of the 1 : 2 DEMUX.

Figure 5 shows a chip photograph of the whole 1 : 2 DEMUX IC. The total chip area is 875 × 640 μm^2, including the pads. The high-speed data is received by the top pads, and the clock signal enters via the bottom pads. The left and right pads are used for data output.

5. Measurement results

The performance of the fabricated DEMUX was evaluated on-wafer by employing a Cascade Microtech probe station. To gain an insight into the operating range of the DEMUX, a 400-mV$_{\mathrm{pp}}$ $2^{31} - 1$ pseudo-random bit sequence (PRBS) input data pattern with different rates was applied. A 600-mV$_{\mathrm{pp}}$ single-ended clock signal with half corresponding data rate must be applied at the same time, which first passed a 90 ° phase shifter, then through a balun in the front of the IC. The 90 ° phase shifter was used to adjust the relative phase between the clock and the data for an optimal sampling point, and the balun was used to perform the single-ended to differential conversion for the differential-ended clock input required by the IC.

An Agilent 86100A Infinium DCA wide-bandwidth oscilloscope was employed to receive, display and analyze the output signals. Figure 6 shows the output single-ended data eye diagrams for 2.5, 5, and 10 Gb/s with a data input rate of 5, 10, and 20 Gb/s, respectively. Each plot in Fig. 6 displays two single-ended output eye diagrams, captured simultaneously from two output ports.

All measurements were executed using a 1.8 V supply voltage. The measured total power consumption of the IC is 144 mW, in which the core circuit accounts for about 28%. From Fig. 6, it can be found that the single-ended output swing is above 200 mV. Figure 7 shows the output single-ended data eye diagrams of 2.5 and 10 Gb/s when STM16/OC48 and STM64/OC192 masks are applied, respectively.

A comparison with results from previously published studies is tabulated in Table 1. Specially, three 1 : 2 DEMUXs are compared in detail. It needs to be pointed out that due to the existence of only four latches in both Ref. [1] and Ref. [4], a phase difference of half a clock cycle occures between the two demultiplexed data signals. Moreover, the absence of data input buffers in Ref. [1] and Ref. [4] makes them difficult to implement in a real application, just as mentioned in Section

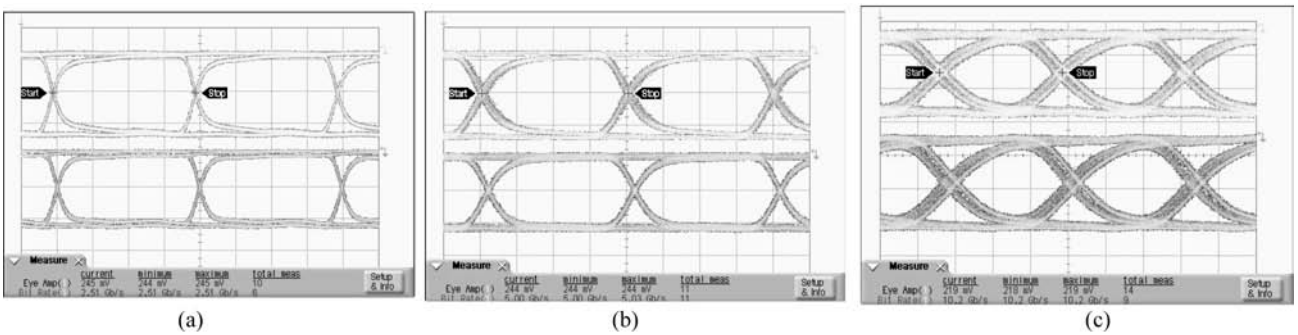

Fig. 6. Output single-ended data eye diagrams at (a) 2.5 G/s, (b) 5 Gb/s, and (c) 10 Gb/s with a data input rate of 5 Gb/s, 10 Gb/s, and 20 Gb/s, respectively.

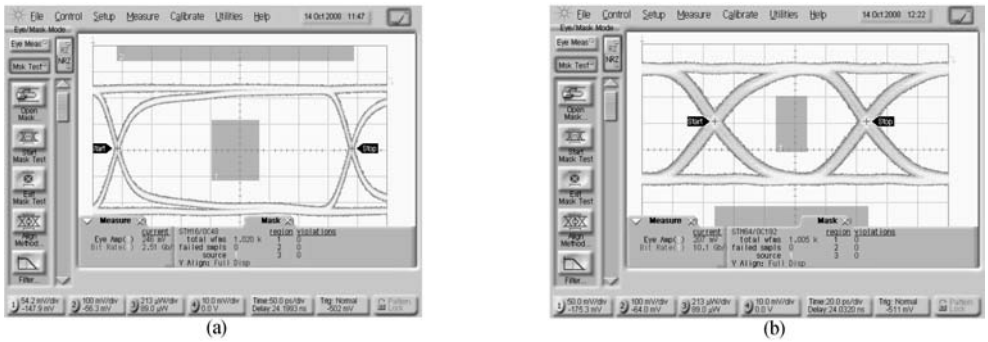

Fig. 7. Output single-ended data eye diagrams at (a) 2.5 Gb/s and (b) 10 Gb/s when STM16/OC48 and STM64/OC192 masks are applied, respectively.

Table 1. Performance comparison of the high-speed CMOS DEMUX.

Parameter	This paper	Ref. [18]	Ref. [4]	Ref. [1]	Ref. [3]	Ref. [2]
Technology	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.12-μm CMOS	0.13-μm CMOS	90-nm CMOS
Function	1 : 2	1 : 8	1 : 2	1 : 2	1 : 4	1 : 4
Maximum data rate (Gb/s)	20	10	20	40	20	40
Supply (V)	1.8	2	2	1.5	1.2	1.2
$P_{\rm diss}$ (mW)	144	102	150	108	210	62
Data input buffer (Y/N)	Y	–	N	N	Y	Y
Area (μm^2)	875 × 640	–	920 × 820	630 × 470	1050 × 920	2400 × 2800

3.1. However, even if these two shortcomings are ignored for the moment, our DEMUX still possesses a better performance than that in Ref. [4] with respect to the supply voltage, power consumption and area. Among the three DEMUXs having input data buffers, the inductive peaking technique occupying a large chip area is not adopted in Ref. [3]. So, its peak speed is restricted. In addition, it should be added that the capacitive-splitting CML latch consuming larger space and the composite latch, consisting of a conventional dynamic CML latch followed by a buffer, which consumes more power, are used in Ref. [4] and Ref. [3], respectively In contract, a compact static CML latch, which consumes less space and less power, is adopted in this work.

6. Conclusions

A 1 : 2 DEMUX has been designed and fabricated in SMIC's 0.18-μm CMOS technology. The DEMUX operates at a maximum data rate of 20 Gb/s, takes up an area of 875 × 640 μm^2, and consumes 144 mW of power at a 1.8-V supply voltage.

This work possesses the following characteristics: a current-density-centric design philosophy, the standard CML logic style, a data input buffer for the integrality of the DEMUX, the shunt inductive peaking technique to enhance the bandwidth for the highest data speed, the compact static latch for broader operation range, optimization and elaborate layout. Based on these characteristics, this DEMUX shows a superior performance, as shown in Table 1.

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