

Layout Design and Optimization of RF Spiral Inductors on Silicon Substrate *

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Abstract: The effects of key geometrical parameters on the performance of integrated spiral inductors are investigated with the 3D electromagnetic simulator HFSS. While varying geometrical parameters such as the number of turns (N), the width of the metal traces (W), the spacing between the traces (S), and the inner diameter (ID), changes in the performance of the inductors are analyzed in detail. The reasons for these changes in performance are presented. Simulation results indicate that the performance of an integrated spiral inductor can be improved by optimizing its layout. Some design rules are summarized.

Key words: silicon substrate; spiral inductor; quality factor; self resonance frequency

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1 Introduction

Planar spiral inductors have become essential elements of communication circuit blocks, such as voltage-controlled oscillators (VCOs), low-noise amplifiers (LNAs), mixers, and intermediate frequency filters (IFFs)^[1]. To meet the need for greater portability, increased functionality, and lower cost of today's wireless communication systems, integrated planar spiral inductors with small form factors, high Q , and high self-resonant frequencies on silicon substrate are highly desired. However, the performance of inductors on silicon needs to be further improved for RFICs because of the structure design and substrate loss. The most important concern in designing silicon spiral inductors is obtaining inductors with the desired inductance values that at the same time have high enough quality factors. To achieve this, the structure and layout geometry of the inductors must be well designed to induce magnetic coupling between the spiral windings, reduce the series resistance of the inductors' metal spirals, and reduce loss through the substrate.

Much research has focused on the design, modeling, and optimization of spiral inductors on silicon substrate^[2-8]. However, spiral optimization is a never-ending job, and there remains great incentive to design and optimize spiral inductors fabricated on Si substrates. In this paper, spiral inductors are analyzed by using a 3D HFSS (high frequency structure simulator) to study the influence of layout on an inductor's performance in the multi-GHz frequency range. Spiral inductors with different geometrical parameters and the same substrate are simulated and analyzed. The key geometrical parameters include the number of turns (N), the width of the metal traces (W), the spacing between the traces (S), and the inner diameter (ID). As these parameters are varied, the characteristic of the inductors are simulated and analyzed.

2 Modeling of spiral inductors

Silicon spiral inductor design involves a complex trade-off between layout parameters and process parameters. In this work, all inductors are simulated and analyzed using the same substrate structure. The Si substrate and SiO₂ isolation pa-

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rameters are set up based on the Bi/CMOS data. In the bipolar process or Bi/CMOS processes, the Si substrate resistivity is typically between 10 and $30 \cdot \text{cm}^{[9]}$. For our simulations, we have chosen to use $10 \cdot \text{cm}$. The substrate setup is thereby simplified to a $300\mu\text{m}$ Si substrate with a resistivity of $10 \cdot \text{cm}$ with a $9.8\mu\text{m}$ SiO_2 layer that has a permittivity of 4.0 and a $0.7\mu\text{m}$ -thick layer of glass on the top of the Si.

The substrate structure is shown in Fig. 1(a). In this inductor, aluminum traces are used as active devices. A bottom metal layer (M1) and interconnection metal layer (M2), separated by a SiO_2 layer, form the feed line and spirals of the inductor, respectively. M1 and M2 can be interconnected with bias. They are 2 and $0.5\mu\text{m}$ thick, respectively. Figure 1(b) shows a top view of the spiral inductor.

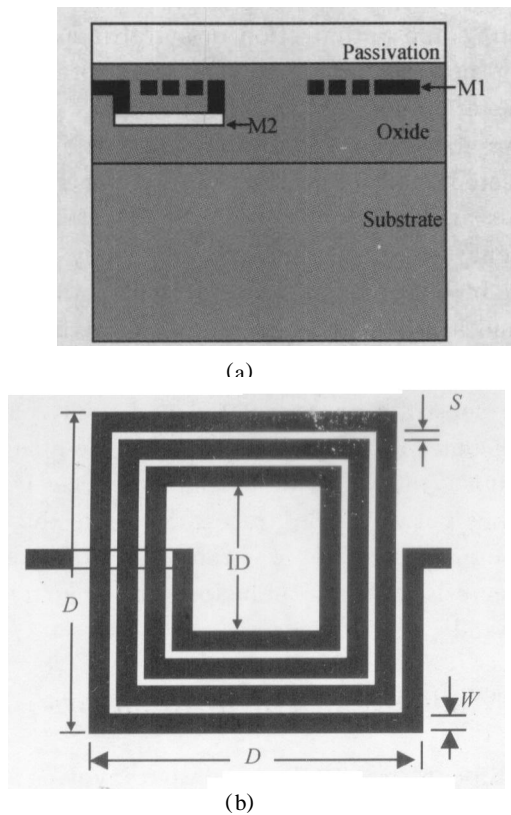


Fig. 1 Simplified cross-sectional view (a) and simplified top view (b) of the spiral inductor

The HFSS system generates complete electromagnetic (EM) field solutions and the associated port characteristics and S -parameters. Y parameters can be deduced from the S -parameters in a defined range of frequencies for individual inductors. The effective inductance L and the quality factor Q

of the inductors are calculated by the equations^[10]

$$Q = -\frac{\text{Im}(Y_{11})}{\text{Re}(Y_{11})} \quad (1)$$

$$L = \frac{-1}{2 f \text{Im}(Y_{11})} \quad (2)$$

The maximum Q (Q_{\max}) and self-resonance frequency (SRF) are easily derived from the Q - f curve.

3 Results and discussion

3.1 Variation of the number of turns (N)

Four inductor types are chosen for simulation to investigate the variation of N . All four types have the same layout parameters except for the number of the turns. The inner diameter (ID) is $136\mu\text{m}$, the metal line width is $12\mu\text{m}$, and the line spacing is $4\mu\text{m}$. Figure 2 shows a comparison of the Q factors and inductances L for various values of N .

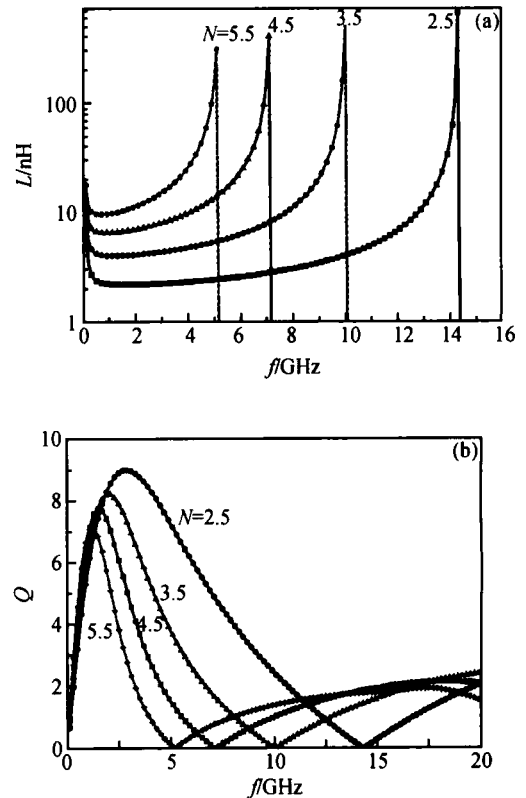


Fig. 2 (a) Simulation results of the spiral inductor inductance for different values of N ; (b) Simulation results of the spiral inductor Q factor for different values of N

Table 1 Simulation results of spiral inductors with various values of N

Inductor	N	Q_{max}	$f_{\phi_{max}} / \text{GHz}$	Inductance/ nH	SRF/ GHz
1	2.5	9.02	2.9	2.23	14.3
2	3.5	8.24	2.0	4.09	10.1
3	4.5	7.76	1.5	6.67	7.2
4	5.5	7.16	1.2	9.90	5.2

When varying the number of turns, the inductances with the same frequency are clearly enhanced as the number of turns increases. The reason for the enhancement of the inductances is obvious. However, Q_{max} and SRF have the opposite tendency. As the number of turns increases, increased metal loss and substrate coupling are the main reasons for the decrease of Q_{max} . The decrease of SRF is mainly due to the enhancement of inductance and capacitive coupling between the metal traces as well as to the substrate. Although inductance is clearly enhanced as the number of turns increases, the result is an increase in the area of the inductors, which is not beneficial for integration.

3.2 Variation of spacing between traces (S)

Five inductor types are chosen for simulation to investigate the variation of S . All five types have the same layout parameters except for the spacing between the traces. The inner diameter is $120\mu\text{m}$, the metal line width is $8\mu\text{m}$, and the number of the turns is 2.5. As the spacing between the traces increases from 8 to $40\mu\text{m}$, the performance of the spiral inductors as a function of S is shown in Fig. 3 and Table 2.

Table 2 Simulation results of the spiral inductors for different values of S

Inductor	S	Q_{max}	$f_{\phi_{max}} / \text{GHz}$	Inductance/ nH	SRF/ GHz
L1	8	8.61	3.6	1.99	18.4
L2	16	7.58	3.6	1.96	18.1
L3	24	6.97	3.5	1.99	17.5
L4	32	6.68	3.6	2.10	17.1
L5	40	6.25	3.6	2.13	16.5

Figure 3(a) and Table 2 show that the inductances at the same frequency have no obvious change in the low frequency range when the spacing between the traces increases. However, Q_{max} decreases with the increase of the spacing. As the spacing decreases, the substrate coupling has no obvious change, so the changes of $f_{\phi_{max}}$ and SRF are not obvious. The reason for the decrease of Q_{max}

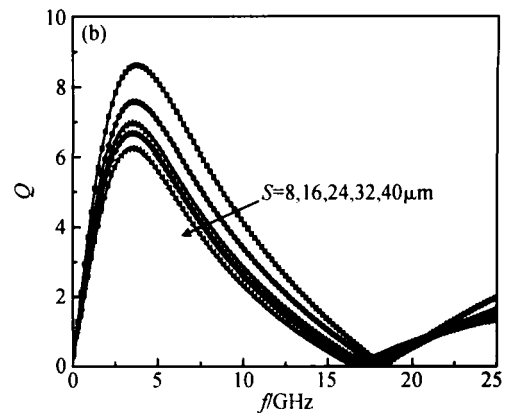
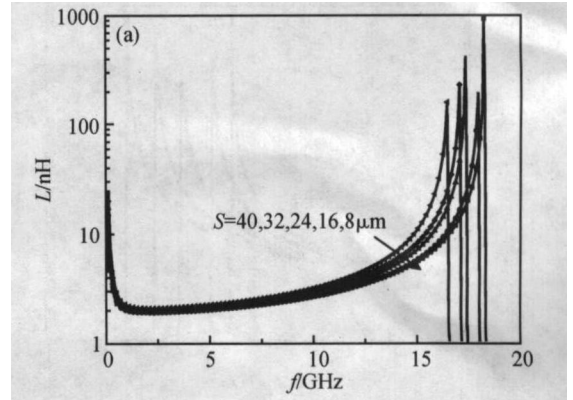


Fig. 3 (a) Simulation results of inductance for different values of S ; (b) Simulation results of Q factor for different values of S

is that the increase of the spacing between adjacent metal traces lowers the magnetic coupling of the adjacent metal traces.

3.3 Variation of width of the metal traces (W)

Five inductor types are chosen for simulation with different trace widths W . The inner diameter, the line spacing, and the number of turns remain constant while the width of the metal traces are increased by increments of $4\mu\text{m}$. The inner diameter is $120\mu\text{m}$, the line spacing is $4\mu\text{m}$, and the number of turns is 3.5. The performance of the spiral inductors for trace widths from 8 to $24\mu\text{m}$ are illustrated in Fig. 4 and Table 3.

Table 3 Simulation results of the spiral inductors for different values of W

Inductor	W	Q_{max}	$f_{\phi_{max}} / \text{GHz}$	Inductance/ nH	SRF/ GHz
L1	8	7.73	2.6	3.66	12.2
L2	12	7.89	2.2	3.50	11.2
L3	16	7.95	2.0	3.48	10.3
L4	20	7.56	1.7	3.52	9.2
L5	24	7.39	1.6	3.54	8.5

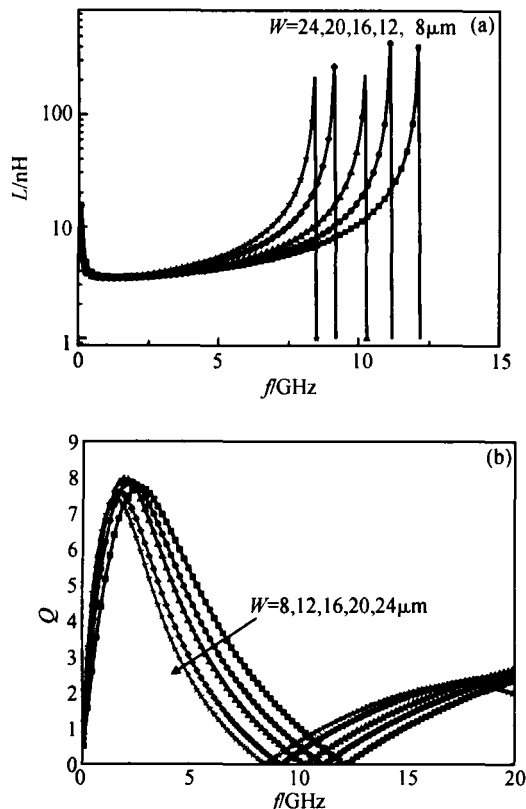


Fig. 4 (a) Simulation results of inductance for different values of W ; (b) Simulation results of Q factor for different values of W

Figure 4(a) shows that in the low frequency range the inductance has no obvious change. In the high frequency range, the inductance becomes larger as the width of the metal traces increases. Q_{max} increases as the width of the metal traces increases from 8 to 16 μm . The AC resistance of a conductor is determined by the current distribution over its cross-section, which is in turn determined by the skin-depth of the conductor^[11]. The increase of the effective width of the metal traces contributes dominantly to the reduction of the series resistance of the inductors. This is why the Q -factors of the inductors increase as the metal width increases from 8 to 16 μm . However, when the metal width increases from 16 to 24 μm , the increase in effective width is negligible. The series resistance of the inductors increases. Thus Q_{max} has a tendency to decrease with the increase of the width of the metal traces. The reason for the decrease of SRF and $f_{Q_{max}}$ is the enhancement of inductance and capacitive coupling between the metal traces and the substrate.

3.4 Variation of inner diameter (ID)

Four inductor types are chosen for simulation with different ID values. All four types have the same layout parameters except for their inner diameters. The metal line width is 12 μm , the line spacing is 4 μm , and the number of turns is 3. 5. The performance of spiral inductors for ID from 90 to 180 μm is illustrated in Fig. 5 and Table 4.

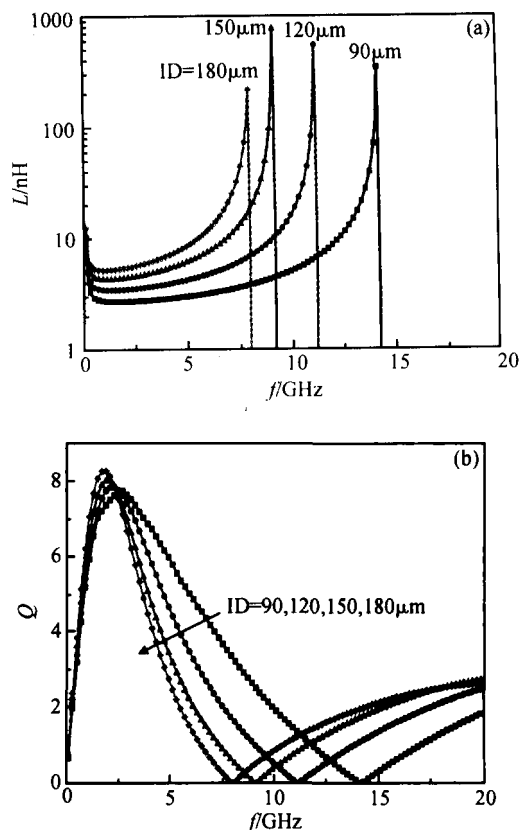


Fig. 5 (a) Simulation results of the spiral inductor inductance for different values of ID; (b) Simulation results of the spiral inductor Q factor for different values of ID

Table 4 Simulation results for different values of ID

Inductor	ID/ μm	Q_{max}	$f_{Q_{max}}/GHz$	Inductance/nH	SRF/GHz
1	90	7.81	2.6	2.74	14.1
2	120	7.89	2.2	3.50	11.1
3	150	8.06	2.0	4.41	9.1
4	180	8.33	1.8	5.35	8.0

Figure 5 shows the Q values as a function of frequency for various spiral inductors with different inner diameters. The reduction of the diameter gives rise to the reduction of the Q value at lower frequencies. As the ID decreases, the proximity effect becomes significant enough to induce

an eddy current in the metal traces, consequently increasing the series resistance^[12]. This also implies that the substrate loss in an inductor with a smaller diameter is less than in one with a larger diameter.

4 Conclusion

The design of a spiral inductor on silicon substrate involves a complex trade-off between design parameters. Here we summarize some "design rules".

(1) While effective inductance increases with the number of turns, the metal loss and the substrate coupling also increase. The increase of the number of turns also requires a larger area.

(2) The strip width must be optimized on the basis of the skin depth of the conductor. Excessively increasing the conductor width causes a downward shift in the peak Q -factor and also makes the Q -factor more sensitive to changes in operating frequency.

(3) The spacing between adjacent metal traces should be small enough to optimize the magnetic coupling.

(4) The reduction of diameter gives rise to the reduction of the Q value at lower frequencies.

References

[1] Mohan S S, del Mar Hershenson M, Boyd S P, et al. Simple

accurate expressions for planar spiral inductances. *IEEE J Solid-State Circuits*, 1999, 34: 1419

[2] Chao C J, Wong S C, Kao C H, et al. Characterization and modeling of on-chip spiral inductors for Si RFICs. *IEEE Trans Semicond Manuf*, 2002, 15: 19

[3] Long J R, Copeland M A. The modeling, characterization, and design of monolithic inductors for silicon RF IC's. *IEEE J Solid-State Circuits*, 1997, 32: 357

[4] Burghartz J N, Edelstein D C, Ainspan H A, et al. RF circuit design aspects of spiral inductors on silicon. *IEEE J Solid-State Circuits*, 1998, 33: 2028

[5] Wang X N, Zhao X L, Zhou Y, et al. Fabrication and performance of novel RF spiral inductors on silicon. *Microelectronics Journal*, 2005, 36: 737

[6] Burghartz J N. Status and trends of silicon RF technology. *Microelectron Reliab*, 2001, 41: 13

[7] Yang Rong, Li Junfeng, Zhao Yuyin, et al. A novel local-dielectric-thickening technique for performance improvements of spiral inductors on Si substrate. *Chinese Journal of Semiconductors*, 2005, 26(5): 857

[8] Liu Chang, Chen Xueliang, Yan jinlong. Novel substrate pn junction isolation for RF integrated inductors on silicon. *Chinese Journal of Semiconductors*, 2001, 22(12): 1486

[9] Yue C P, Wong S S. Physical modeling of spiral inductors on silicon. *IEEE Trans Electron Devices*, 2000, 47: 560

[10] Lin Shiwei, Guo Lihui. Influence of metal layer thickness of spiral inductors on the quality factor by 3-D EM simulation. *5th International Conference on ASIC*, 2003, 2: 1117

[11] Talwalkar N A, Yue C P, Wong S S. Analysis and synthesis of on-chip spiral inductors. *IEEE Trans Electron Devices*, 2005, 52: 176

[12] Cranicckx J, Steyaert M S J. A 1.8-GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors. *IEEE J Solid-State Circuits*, 1997, 32: 736

硅基螺旋电感的几何参数设计和优化*

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摘要: 使用三维电磁场模拟的方法对相同硅衬底结构下不同布图结构的螺旋电感进行了模拟和分析. 通过改变电感匝数、电感金属的宽度和间隔以及电感的内径, 模拟和分析了电感性能的变化. 给出了引起电感性能变化的原因. 结果表明优化电感的几何参数可以有效地改善电感性能. 得出了一些实用的设计原则, 可有效地指导射频集成电路中集成电感的设计.

关键词: 硅基; 螺旋电感; 品质因子; 自振荡频率

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