# Multifunction Voltage-Mode Filter Using Single Voltage Differencing Differential Difference Amplifier

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**Abstract.** In this paper, a voltage mode multifunction filter based on single voltage differencing differential difference amplifier (VDDDA) is presented. The proposed filter with three input voltages and single output voltage is constructed with single VDDDA, two capacitors and two resistors. Its quality factor can be adjusted without affecting natural frequency. Also, the natural frequency can be electronically tuned via adjusting of bias current. The filter can offer five output responses, high-pas (HP), band-pass (BP), band-reject (BR), low-pass (LP) and all-ass (AP) functions in the same circuit topology. The output response can be selected by choosing the suitable input voltage without the component matching condition and the requirement of additional double gain voltage amplifier. PSpice simulation results to confirm an operation of the proposed filter correspond to the theory.

## 1 Introduction

In analog image processing system, the filter is the main circuit that is used to separate the desired signal from undesired ones. Especially, the versatile filter called as multifunction filter has been gained significant attention and has become an interesting research topic. Because the multifunction filter can provide several filter responses in the same circuit topology [1]. The multiple inputs single output (MISO) multifunction filter belongs to popular filter structures. An important feature of this structure is the generation of several output transfer functions, i.e., high-pas (HP), band-pass (BP), band-reject (BR), low-pass (LP) and all-ass (AP) with single output node while the output response can be selected by suitable input signals. The popular way to select the input signal is to use the digital or electronic switch which is easily controlled by microcomputer or microcontroller. So, the MISO filter structure should not require the double input signal to avoid the addition al amplifier.

The voltage differencing differential difference amplifier (VDDDA) is the interesting active building block. This active device consists of three subtraction /addition voltage signal terminals with electronically tunable transconductance. With this feature, it can be found the VDDDA based analog circuits in the literature for examples, first order voltage mode filter [2], sinusoidal oscillator [2], inductance simulator [4], single input multiple output voltage mode filter [5]-[6], multiple input multiple output voltage mode filter [7] etc. Recently, the VDDDA based three inputs single output voltage mode multifunction filter [8] was published. This filter is attractive because it is minimum number of active element consisting of single VDDDA, single resistor and two capacitors. The natural frequency and quality factor can be electronically controlled. However, the inverting double gain voltage amplifier is required for getting the all-pass response.

In this paper, a voltage mode multifunction filter based on single voltage differencing differential difference amplifier (VDDDA) is proposed. The filter with three input voltages and single output voltage is constructed with single VDDDA, two capacitors and two resistors. Its quality factor can be adjusted without affecting natural frequency. Also, the natural frequency can be electronically tuned via adjusting of bias current. The filter can offer five output responses, high-pas (HP), band-pass (BP), band-reject (BR), low-pass (LP) and all-ass (AP) functions in the same circuit topology. The output response can be selected by choosing the suitable input voltage without the component matching condition and the requirement of additional double gain voltage amplifier. PSpice simulation results to confirm an operation of the proposed filter correspond to the theory.

## 2 Circuit configuration and analysis of the proposed filter

### 2.1 VDDDA

In order to understand the proposed filter, the brief details of the active building block, VDDDA are given in this section. The symbolic representation of VDDDA is shown in Fig. 1(a). It has five input voltage terminals, called as V+, V-, Z, P and N ports. The Z port is also the output current terminal and the W port is the output voltage. Ideally, the impedance at V+, V-, Z, P and N

ports are assumed to be infinite while the impedance at W port exhibits low. The equivalent circuit is illustrated in Figure 1(b). In this design, the VDDDA is constructed from CMOS technology as illustrated in Figure 1(c). The idealization of VDDDA's parameters implies that

$$I_{v+} = I_{v-} = I_{v_N} = I_{v_P} \tag{1}$$

$$I_z = g_m \left( V_{v+} - V_{v-} \right) \tag{2}$$

$$V_w = V_Z - V_{v_N} + V_{v_P} \tag{3}$$

The transconductance gain of VDDDA is proportional to bias current $I_B$ and is given by

$$g_m = \sqrt{I_B \mu C_{ox} \left( W / L \right)_{15,16}} \tag{4}$$

"where μ is the mobility of the carrier for NMOS transistors, M15 and M16 in Fig. 1(c), $C_{ox}$ is the gate oxide capacitance per unit area, W and L are the channel width and channel length, respectively." [9]

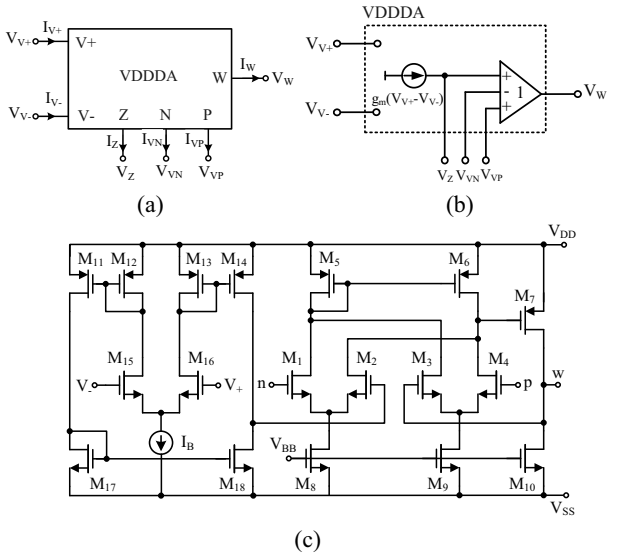


**Figure 1.** VDDDA, (a) circuit symbol, (b) equivalent circuit and (c) schematic diagram of CMOS VDDDA

## 2.2 Proposed three input single output voltage mode universal filter

Fig. 2 shows the proposed three input single output (TISO) filter. It requires only one VDDDA, two capacitors and two resistors. There are three input voltages, $V_{in1}$, $V_{in2}$, $V_{in3}$ and single output voltage, $V_o$. Considering the circuit in Fig. 2, it yields the following output voltage

$$V_O = \frac{s^2 V_{in2} + s\frac{1}{C_1 R_1}\left(1+\frac{R_1}{R_2}\right)V_{in3} + \frac{g_m V_{in1}}{2C_1 C_2 R_1}}{s^2 + s\frac{1}{C_1 R_1}\left(1+\frac{R_1}{R_2}\right) + \frac{g_m}{2C_1 C_2 R_1}} \tag{5}$$

It can be noted that the proposed circuit is the unity gain filter and it can realize various filter configurations with the following input voltage selections

- The second-order LP response can be obtained if $V_{in1} = V_{in}$ (connected to the input voltage source) and $V_{in2} = V_{in3} = 0$ (grounded).
- The second-order HP response can be obtained if $V_{in2} = V_{in}$ (connected to the input voltage source) and $V_{in1} = V_{in3} = 0$ (grounded).
- The second-order BP response can be obtained if $V_{in3} = V_{in}$ (connected to the input voltage source) and $V_{in1} = V_{in2} = 0$ (grounded).
- The second-order BR response can be obtained if $V_{in1} = V_{in2} = V_{in}$ (connected to the input voltage source) and $V_{in3} = 0$ (grounded).
- The second-order AP response can be obtained if $V_{in1} = V_{in2} = -V_{in3} = V_{in}$ (connected to the input voltage source).

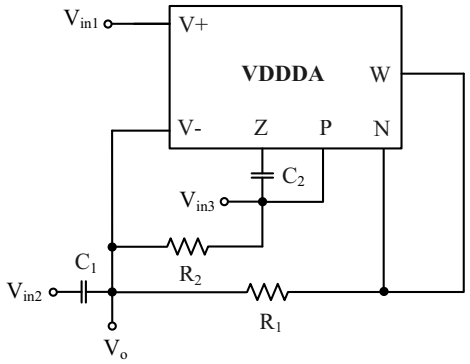


**Figure 2.** VDDDA based voltage mode TISO filter.

Considering to the denominator in Eq. (5), the natural frequency ($\omega_0$) and quality factor (Q) can be give as

$$\omega_0 = \sqrt{\frac{g_m}{2C_1 C_2 R_1}} \text{ and } Q = \frac{1}{1+\frac{R_1}{R_2}}\sqrt{\frac{g_m C_1 R_1}{2C_2}} \tag{6}$$

It should be noted from Eq. (6) that the quality factor can be tuned by $R_2$ without affecting natural frequency. Also, the natural frequency can be electronically tuned by $I_B$.

## 2.3 Analysis of non-ideal case

The non-ideal properties of VDDDA will affect the performance of the proposed filter. In this section, the non-ideal parameters will be studies and analyzed. The first one is the voltage tracking errors from Z, N and P ports to W port. The non-ideal characteristic of VDDDA is written as

$$V_w = \beta_z V_z - \beta_n V_{vn} + \beta_p V_{vp} \tag{7}$$

where $\beta_z$, $\beta_n$ and $\beta_p$ are the voltage tracking errors from Z, N and P ports to W port, respectively. In this case, the output voltage will be change to

$$V_o = \frac{s^2 V_{in2} + \frac{sV_{in3}}{C_1 R_1}\left[\left(\frac{\beta_z + \beta_p}{1+\beta_n}\right) + \frac{R_1}{R_2}\right] + \frac{V_{in1} g_m \beta_z}{C_1 C_2 R_1 (1+\beta_n)}}{s^2 + \frac{s}{C_1 R_1}\left[\left(\frac{\beta_z + \beta_p}{1+\beta_n}\right) + \frac{R_1}{R_2}\right] + \frac{g_m \beta_z}{C_1 C_2 R_1 (1+\beta_n)}} \quad (8)$$

From Eq. (8), the parameters $\omega_0$ and Q are given as

$$\omega_0 = \sqrt{\frac{g_m \beta_z}{C_1 C_2 R_1 (1+\beta_n)}} \quad (9)$$

and

$$Q = \frac{1}{\left(\frac{\beta_z + \beta_p}{1+\beta_n}\right) + \frac{R_1}{R_2}} \sqrt{\frac{\beta_z g_m C_1 R_1}{(1+\beta_n) C_2}} \quad (10)$$

Considering the nominator in Eq. (8), the voltage tracking errors will affect the gain and filter response. When consider the denominator in Eq. (8), the tracking errors will affect the natural frequency and the quality factor as shown in Eqs. (9) and (10).

## 3 Simulation results

The proposed filter is evaluated using PSpice simulator tool. The internal construction of VDDDA is based on CMOS technology in Fig. 1(c). The NMOS and PMOS transistor models are adopted from the Taiwan semiconductor manufacturing company (TSMC) 0.25µm CMOS process parameters at ±1.25 supply voltages. The aspect ratios of the MOS transistors are listed in Table I. The value of capacitors chosen as $C_1$=$C_2$=80pF. The value of resistors chosen as $R_1$=2kΩ, $R_2$=10kΩ, and the input bias currents $I_B$ is set to 100µA. Fig. 3 depicts the gain responses of low-pass, high-pass and band-pass responses. The gain and phase responses of band-reject function are illustrated in Fig. 4. The gain and phase responses of all-pass function are illustrated in Fig. 5. The simulated natural frequency is 1.074 MHz. With the same values of resistances, capacitances and bias currents stated above, the theoretical natural frequency in Eq. (6) is 1.033 MHz. It is found that the deviation of theoretical and simulated value is about 3.96%. This deviation is caused by the voltage tracking error in VDDDA as analyzed in Section 2.3.

**Table 1.** Aspect ratios of mos transistors [9]

| Transistor | W (µm) | L (µm) |
|---|---|---|
| M1-M4 | 1 | 0.25 |
| M5-M7 | 15 | 0.25 |
| M8-M10 | 3 | 0.25 |
| M11-M16 | 5 | 0.25 |
| M17-M18 | 3 | 0.25 |

The transient response of $V_{BP}$ is shown in Fig. 6. In order to control the $\omega_0$ with electronic method, the $\omega_0$ tuning is confirmed via the BP response in Fig. 7. By using $C_1$=$C_2$=80pF and varying $I_B$ with different values of 40µA, 100µA and 250µA, the simulated natural frequencies are 883.08kHz, 1.074MHz and 1.256MHz, respectively. In order to control the quality factor without affecting the $\omega_0$, the quality factor tuning is confirmed via the BP response in Fig. 8. By using $C_1$=1nF, $C_2$=50pF, $I_B$=50µA, $R_1$=2kΩ and varying $R_2$ with different values of 1kΩ, 2kΩ and 4kΩ, the simulated quality factor are 1.47, 2.71 and 3.52, the theoretical natural frequency in Eq. (4) are 1.67, 2.73 and 3.75, respectively.

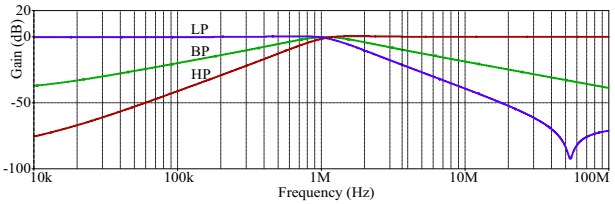


**Figure 3.** Gain responses for LP, HP and BP functions.

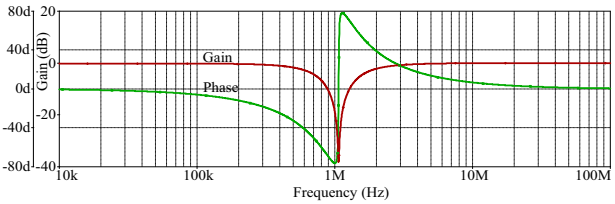


**Figure 4.** Gain and phase responses for BR function.

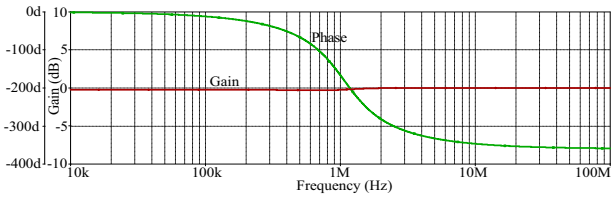


**Figure 5.** Gain and phase response for AP function.

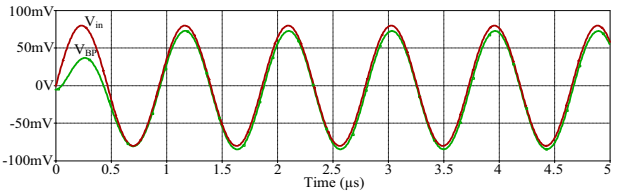


**Figure 6.** Transient response for BP function.

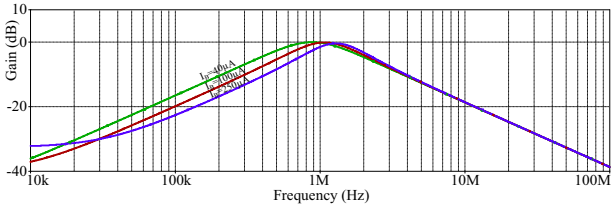


**Figure 7.** BP responses for different values of $I_B$.

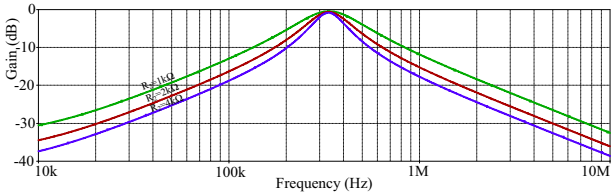


**Figure 8.** Quality factor responses for different values of $R_2$.

## 4 Conclusion

In this work, a multifunction filter with three-input and single-output voltage is realized using active building block, namely voltage differencing differential difference amplifier (VDDDA). The proposed filter consists of single VDDDA, two resistors and two capacitors. The proposed filter can provide five standard functions, all-pass, band-pass, high-pass, band-reject and low-pass responses without changing circuit topology. The selection of input voltages to get output filter responses can be done without the need of component matching condition and double gain amplifier. The natural frequency and quality factor can be tuned electronically. Also, the tune of quality factor can be done without affecting the natural frequency. The proposed filter is suited for fabricating into monolithic chip for low power low voltage application. To evaluate the proposed filter, we implement the circuit based on CMOS VDDDA in 0.25µm TSMC CMOS technology. The simulation results show excellent performances according theoretical expects.

## Acknowledgement

Research described in this paper was financially supported from Faculty of Industrial Education, King Mongkut's Institute of Technology Ladkrabang (KMITL).

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