ARTICLES

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# Fast-transient techniques for high-frequency DC–DC converters

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**Abstract:** A 30 MHz voltage-mode controlled buck converter with fast transient responses is presented. An improved differential difference amplifier (DDA)-based Type-III compensator is proposed to reduce the settling times of the converter during load transients, and to achieve near-optimal transient responses with simple PWM control only. Moreover, a hybrid scheme using a digital linear regulator with automatic transient detection and seamless loop transition is proposed to further improve the transient responses. By monitoring the output voltage of the compensator instead of the output voltage of the converter, the proposed hybrid scheme can reduce undershoot and overshoot effectively with good noise immunity and without interrupting the PWM loop. The converter was fabricated in a 0.13 $\mu$m standard CMOS process using 3.3 V devices. With an input voltage of 3.3 V, the measured peak efficiencies at the output voltages of 2.4, 1.8, and 1.2 V are 90.7%, 88%, and 83.6%, respectively. With a load step of 1.25 A and rise and fall times of 2 ns, the measured 1% settling times were 220 and 230 ns, with undershoot and overshoot with PWM control of 72 and 76 mV, respectively. They were further reduced to 36 and 38 mV by using the proposed hybrid scheme, and 1% settling times were also reduced to 125 ns.

**Key words:** differential difference amplifier (DDA); Type-III compensator; fast transient responses; hybrid scheme; high switching frequency; overshoot/undershoot.

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## 1. Introduction

With the growing demands for high performance computations, both the current consumption and the current slew rate of modern microprocessors have dramatically increased[1]. Large and rapid current changes due to load variations incur large power supply voltage droops, resulting in severe performance degradation or even black-outs of the processors[2–4]. To mitigate the problem, the DC–DC converters that supply power to the processors should have fast transient responses so that both the magnitude and the duration of the voltage droops are reduced. Generally speaking, the transient responses of a DC–DC converter depend on how fast the inductor current can change when load transients occur, and it is mainly limited by two factors: the speed of the controller and the slew rate of the inductor current. Many innovative techniques have been proposed: they either enhance the speed of the controller, and/or overcome the slew rate limitation of the inductor current.

PWM control with fixed switching frequency has been attractive for its predictable noise spectrum and tight voltage regulation. However, it is usually believed that PWM control suffers from slow responses due to its limited loop bandwidth. Many fast-transient techniques have thus been proposed. During load transients, the slew rate of the error amplifier is increased in Refs. [5, 6], the ramp amplitude is adjusted in Ref. [7], $V^2$ control is employed in Refs. [8–11], $V^1$ concept is introduced in Ref. [12] and a capacitor-current-sensor (CCS) calibration technique with transient optimization is proposed in Ref. [13]. As shown in Fig. 1, the goals of these techniques are actually the same, and they are to enhance the speed of the PWM loop so that the inductor current ($I_L$) ramps up (down) quickly to reduce the undershoot (overshoot) of the output voltage ($V_o$) and thus the settling times. On the other hand, to reduce the range of voltage fluctuation during load transients, adaptive voltage positioning (AVP) technique is proposed by designing the output impedance of the converter to be resistive[14, 15]. However, the performance of load regulation using this technique is compromised.

Compared to PWM control, hysteretic control is a more popular scheme for applications that require fast transient responses[16–22], as it could theoretically change its duty cycle from 0 to 100% within one switching period. Efforts of improving the performance of the inductor current sensor have

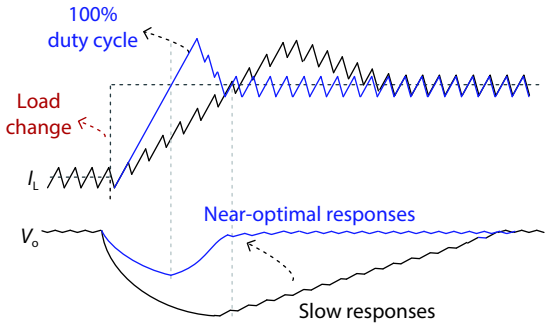


Fig. 1. (Color online) Transient-enhanced techniques for PWM control.

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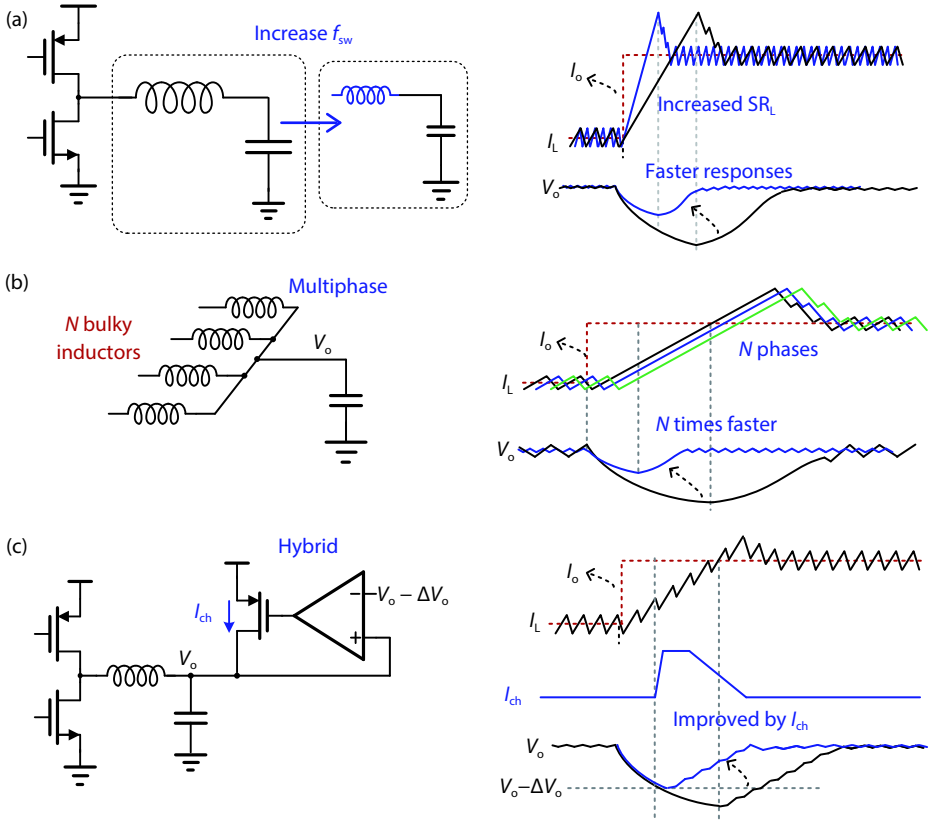


Fig. 2. (Color online) Techniques to overcome the limitation of slew rate of the inductor current ($SR_L$): (a) increasing switching frequency, (b) multiphase topology, (c) hybrid scheme.

been made in recent state-of-the-art hysteretic controllers[20–22]. In Ref. [20], an emulated AC+DC current sensor is proposed to accommodate immediate responses to load changes, but the implementation is complicated. In Ref. [21], a capacitor-current sensor is proposed to optimize transient responses, but optimization can only be achieved under specific conditions. In Ref. [22], a quasi-inductor current emulator with reset operation is proposed to save silicon area and to improve transient responses. However, the converter running at 1 MHz needs a relatively large inductor that limits the slew rate of the inductor current and thus the speed of transient responses.

Using the above mentioned techniques, near-optimal transient responses may be achieved, but the response speed is still limited by the slew rate of the inductor current ($SR_L$). Fig. 2 shows three approaches that can overcome this limitation. As shown in Fig. 2(a), one straightforward way is to use a smaller inductor and switch the converter at a higher frequency[18, 20, 23, 24], which also facilitates system miniaturization and cost reduction. However, efficiency is compromised as switching loss becomes significant, and the circuit design is more challenging[23]. The multiphase topology shown in Fig. 2(b) is widely used to improve current capability and to reduce input current ripples and output voltage ripples[13, 18, 20, 24]. For an *N*-phase converter, $SR_L$ is effectively increased by *N* times. However, it needs *N* bulky inductors that increase volume and cost of the system. Fig. 2(c) shows the third approach that is called the hybrid scheme. It consists of the parallel operation of the DC–DC converter and a linear regulator. This is a common scheme in designing the supply modulator of a power amplifier[25, 26], and has been employed to improve transient responses[27–31]. It is essential that the linear regulator should only be activated during load transients and is completely deactivated in the steady state such that efficiency is not compromised. To achieve maximum improvement on transient responses, the three approaches can be employed together in the same design.

In this paper, a 30 MHz voltage-mode controlled buck converter with fast transient responses is presented[32], and its block diagram is shown in Fig. 3. Transient responses are improved using two methods. First, by using an improved differential difference amplifier (DDA)-based Type-III compensator, the responses of simple PWM control are optimized and are comparable to those of using advanced techniques. Second, a hybrid scheme with automatic transient detection and seamless loop transition is proposed to achieve further improvement. Light-load efficiency is improved by implementing a dedicated discontinuous-conduction mode (DCM) loop that is similar to the design proposed in Ref. [33]. The rest of this paper is organized as follows. The improved DDA-based Type-III compensator and the proposed hybrid scheme are introduced in Section 2 and Section 3, respectively. Measurement results are presented in Section 4, and the research efforts are concluded in Section 5.

## 2. Design of improved DDA-based Type-III compensator

### 2.1. Improved DDA-based Type-III compensator

As shown in Fig. 4(a), a DDA-based Type-III compensator is proposed to save silicon area in Ref. [23], but one additional DC bias for $V_{com}$ is needed and the differential input range

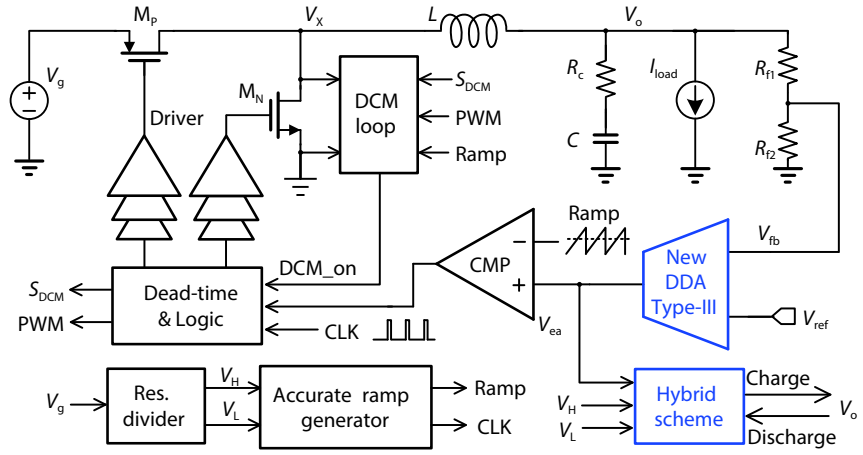


Fig. 3. Block diagram of the proposed buck converter.

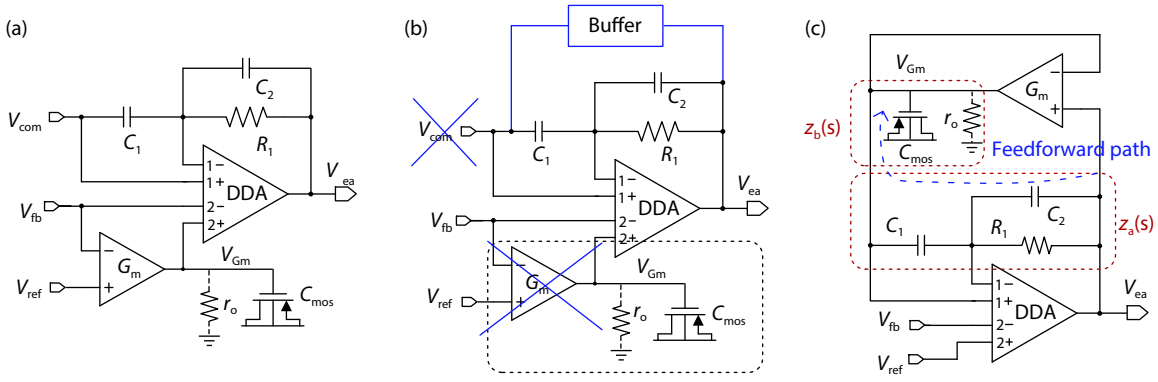


Fig. 4. (a) Previous DDA-based Type-III compensator. (b) Possible improvement on the previous compensator. (c) New DDA-based Type-III compensator.

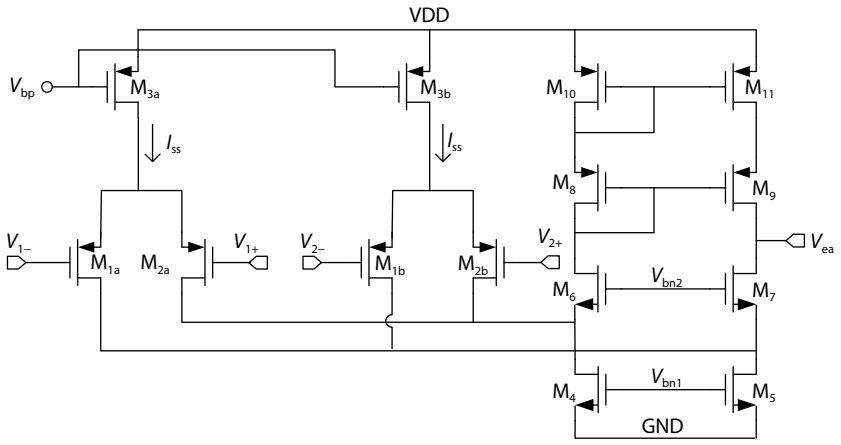


Fig. 5. Schematic of differential difference amplifier (DDA).

of the DDA has to be sufficiently large for proper operation. Although fast reference-tracking responses can be achieved with the help of the end-point prediction scheme, it suffers from long settling times during load transients, which are due to the slow responses at $V_{Gm}$. Fig. 5 shows the implementation of the DDA: a folded-cascode amplifier with two differential input pairs[23]. An improved DDA-based Type-III compensator could overcome these drawbacks. Note that the output of the compensator $V_{ea}$ is equal to $V_{1-}$ in the steady state. As shown in Fig. 4(b), if an analog buffer is inserted from $V_{ea}$ to $V_{com}$, the DC bias for $V_{com}$ can be eliminated. Moreover, as the buffer forces $V_{com}$ (= $V_{1+}$) to be equal to $V_{ea}$, the difference between $V_{1+}$ and $V_{1-}$ is also small in the steady state. As a result, the requirement on the differential input range of the DDA is relaxed. At the same time, with negative feedback, the two input pairs of the DDA bear the relationship given by Ref. [34]

$$V_{1+} - V_{1-} = -(V_{2+} - V_{2-}). \quad (1)$$

Therefore, $V_{fb}$ (= $V_{2-}$) is equal to $V_{2+}$ in the steady state. It means that the transconductance amplifier (OTA) that is used to regulate $V_{fb}$ to be equal to the reference voltage $V_{ref}$ can be removed and $V_{ref}$ can be connected to $V_{2+}$ directly, while the output voltage $V_o$ can still be regulated. We further found

that the added buffer should have a relatively low bandwidth to ensure the stability of the loop and the designed OTA fits the purpose well. Combining the above thoughts results in a new DDA-based Type-III compensator shown in Fig. 4(c) consisting of the same components but with a different configuration. Now, no additional DC bias is needed and the requirement on the input range of the DDA is relaxed. Although $V_{Gm}$ is still the output of the OTA that has a low bandwidth, the feedforward path from $V_{ea}$ to $V_{Gm}$ can help to settle $V_{Gm}$ quickly, as will be discussed later. Next, we will derive the transfer function to confirm that it is still a Type-III compensator.

### 2.2. Improved DDA-based Type-III compensator

As shown in Fig. 4(c), the impedance of $z_a(s)$ and $z_b(s)$ are respectively given by

$$z_a(s) = \frac{1}{sC_1} + R_1 \,||\, \frac{1}{sC_2} = \frac{1+sR_1(C_1+C_2)}{sC_1(1+sR_1C_2)}, \tag{2}$$

$$z_b(s) = r_o \,||\, \frac{1}{sC_{mos}} = \frac{r_o}{1+sC_{mos}r_o}, \tag{3}$$

where $r_o$ is the output resistance of the OTA and $C_2 << C_1$. By writing Kirchhoff's Current Law (KCL) at $V_{Gm}$ (= $V_{1+}$), we have,

$$\frac{V_{ea}-V_{Gm}}{z_a(s)} + G_m(V_{ea}-V_{Gm}) = \frac{V_{Gm}}{z_b(s)}, \tag{4}$$

where $G_m$ is the transconductance of the OTA. After simplification, the ratio of $V_{Gm}$ (= $V_{1+}$) to $V_{ea}$ is given by

$$\frac{V_{Gm}}{V_{ea}} = \frac{[1+G_m z_a(s)]z_b(s)}{[1+G_m z_a(s)]z_b(s)+z_a(s)}. \tag{5}$$

Similarly, by writing KCL at $V_{1-}$, the relationship of $V_{ea}$ and ($V_{1+}$, $V_{1-}$) is given by

$$(V_{1+}-V_{1-})sC_1 = \frac{V_{1-}-V_{ea}}{R_1 \,||\, \frac{1}{sC_2}}. \tag{6}$$

After simplification, we have

$$\frac{V_{1-}-V_{1+}}{V_{ea}} = \frac{1+sR_1C_2}{1+sR_1(C_1+C_2)}\left(1-\frac{V_{Gm}}{V_{ea}}\right). \tag{7}$$

The transfer function of the new compensator $A(s)$ is given by

$$A(s) = -\frac{V_{ea}}{V_{fb}} = \frac{V_{ea}}{V_{2+}-V_{2-}}. \tag{8}$$

Solving Eqs. (1), (5), (7) and (8), $A(s)$ is computed to be

$$A(s) = G_m r_o \frac{(1+sC_{mos}/G_m)[1+s(C_1+C_2)R_1]}{(1+sC_{mos}r_o)(1+sC_2R_1)} + \frac{1+sC_1r_o}{1+sC_{mos}r_o}, \tag{9}$$

which can be rewritten as

$$A(s) = G_m r_o \frac{\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)}, \tag{10}$$

with

$$p_1 = \frac{1}{C_{mos}r_o}, \quad p_2 = \frac{1}{C_2R_1}, \tag{11}$$

$$z_1 = \frac{2}{C_1R_1+\frac{C_{mos}+C_1}{G_m}+\sqrt{\left(C_1^2R_1^2+2\frac{C_1^2R_1-C_{mos}C_1R_1}{G_m}+\frac{(C_{mos}+C_1)^2}{G_m^2}\right)}},$$
$$z_2 = \frac{2}{C_1R_1+\frac{C_{mos}+C_1}{G_m}-\sqrt{\left(C_1^2R_1^2+2\frac{C_1^2R_1-C_{mos}C_1R_1}{G_m}+\frac{(C_{mos}+C_1)^2}{G_m^2}\right)}}. \tag{12}$$

Similarly, the transfer function from $V_{fb}$ to $V_{Gm}$ is given by

$$\frac{V_{Gm}}{V_{fb}} = G_m r_o \frac{1+sC_1(R_1+1/G_m)}{(1+sC_{mos}r_o)(1+sC_2R_1)}. \tag{13}$$

The first part of Eq. (9) is the same as the transfer function of the previous compensator, while the second part is due to the new configuration of the compensator. Figs. 6(a) and 6(b) show the simulated frequency responses of the two compensators and the corresponding loop-gain functions of the converters, respectively. The new compensator is indeed a Type-III compensator and thus can be used to stabilize voltage-mode controlled converters. However, compared to the transfer function of the previous compensator, the new compensator has a lower $z_1$ and a higher $z_2$, and the same $p_1$ and $p_2$. It means that the locations of the zeroes in the new compensator can be adjusted without affecting the locations of the poles, which cannot be done in the previous compensator. Due to this adjustment of the zeroes, the new compensator achieves a higher gain at the frequency region of [$z_1$, $z_2$], which leads to a faster recovery time of the proposed compensator. As also shown in Fig. 6(c), for the previous compensator, the node $V_{Gm}$ is dominant-pole compensated with a low bandwidth. When the load transients occur, $V_{Gm}$ changes slowly with output voltage ($V_o$), resulting in long settling times; but for the new compensator, from Eq. (13), we can see that the transfer function from $V_{fb}$ to $V_{Gm}$ is composed of one zero and two poles. The bandwidth will be extended due to the feedforward path and thus the settling times are reduced. Fig. 7 shows the simulated transient responses of the converters with the two compensators. Compared to the responses using the previous compensator, $V_{Gm}$ settles quickly and the settling times of the output ($V_o$) with the new compensator are much shorter.

Although the proposed compensator results in very fast responses, the stability of the converter is not compromised and the proposed converter is free from both small-signal and subharmonic oscillations[35]. Fig. 8 shows the simulated frequency responses of the proposed compensator and the loop-gain functions of the converter at different PVT (process, voltage, temperature) conditions. The phase margins of the loop-gain functions are larger than 48° in all cases. Fig. 9 fur-

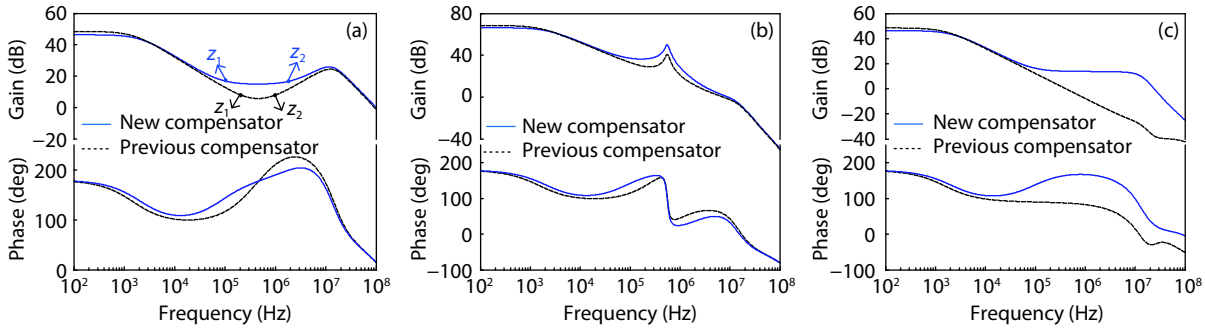


Fig. 6. Simulated frequency responses of (a) the two DDA-based Type-III compensators, (b) the loop-gain functions of the converters with the two compensators, and (c) the transfer functions from $V_{fb}$ to $V_{Gm}$ of the two compensators.

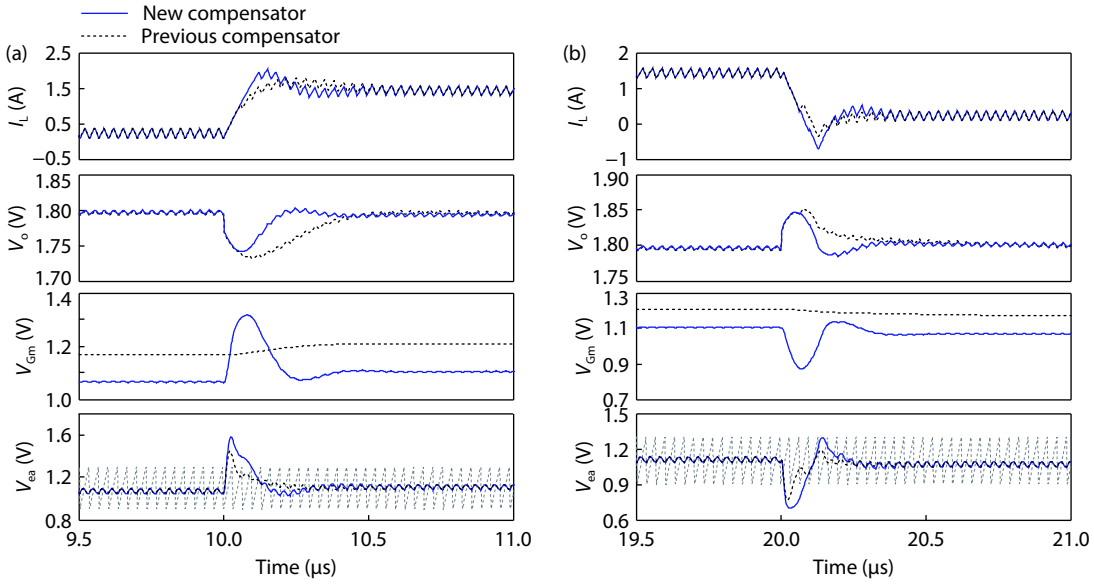


Fig. 7. Simulated transient responses. (a) Up-transient. (b) Down-transient.

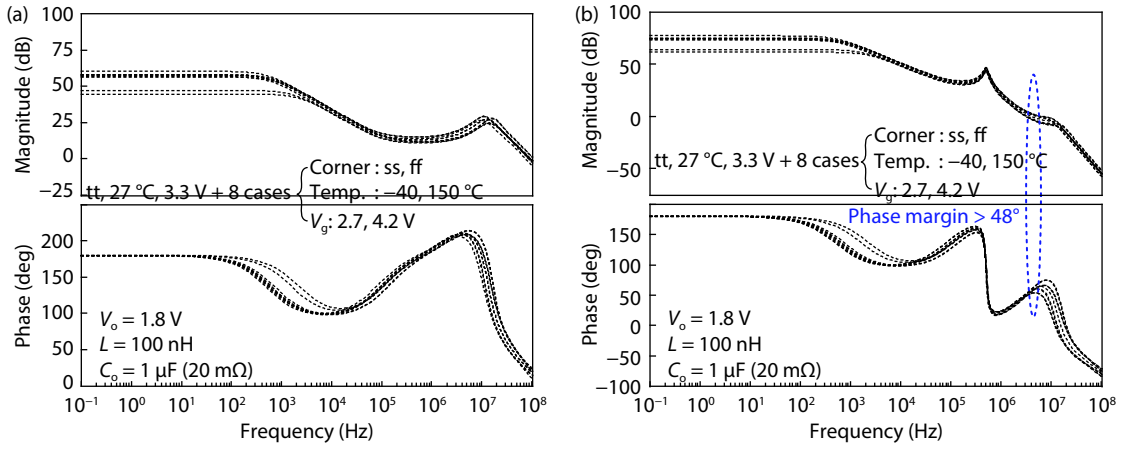


Fig. 8. Simulated frequency responses with PVT variations: (a) proposed Type-III compensator, and (b) loop gain function.

ther shows the simulated transient responses of the converter at different temperatures and process corners with the load current ($I_o$) changes of 1.2 A in 2 ns, and good stability is observed. Therefore, the PWM control scheme with the proposed compensator achieves near-optimal transient responses as those in Refs. [13, 20, 22] and the response speeds are only limited by the slew rate of the inductor current. To further improve the transient responses, a hybrid scheme that is based on the fast responses of the new compensator is further proposed, as will be discussed in the next section.

## 3. Design of the proposed hybrid scheme

### 3.1. Design challenges of hybrid scheme

In designing a supply modulator for power amplifiers[25, 26], it is required that the DC–DC converter and the linear regulator should work all the time to achieve fast responses and small output ripples, but the efficiency is de-

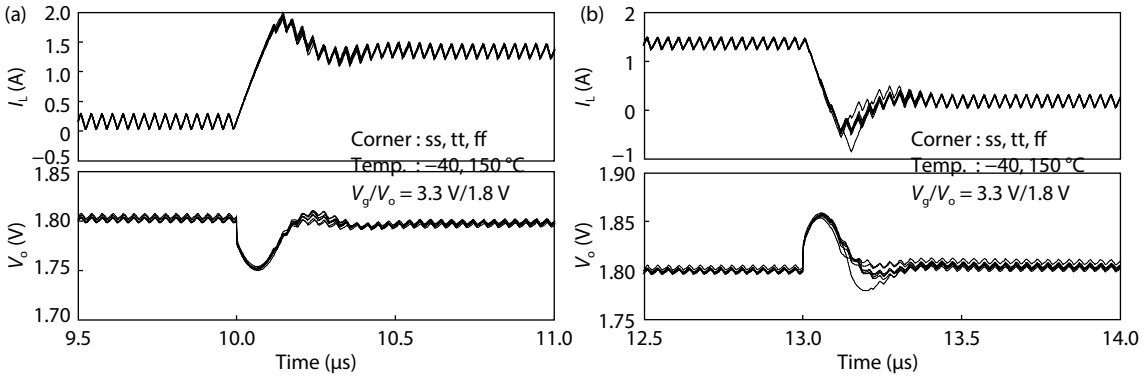


Fig. 9. Simulated transient responses of the proposed converter. (a) Up transient. (b) Down-transient.

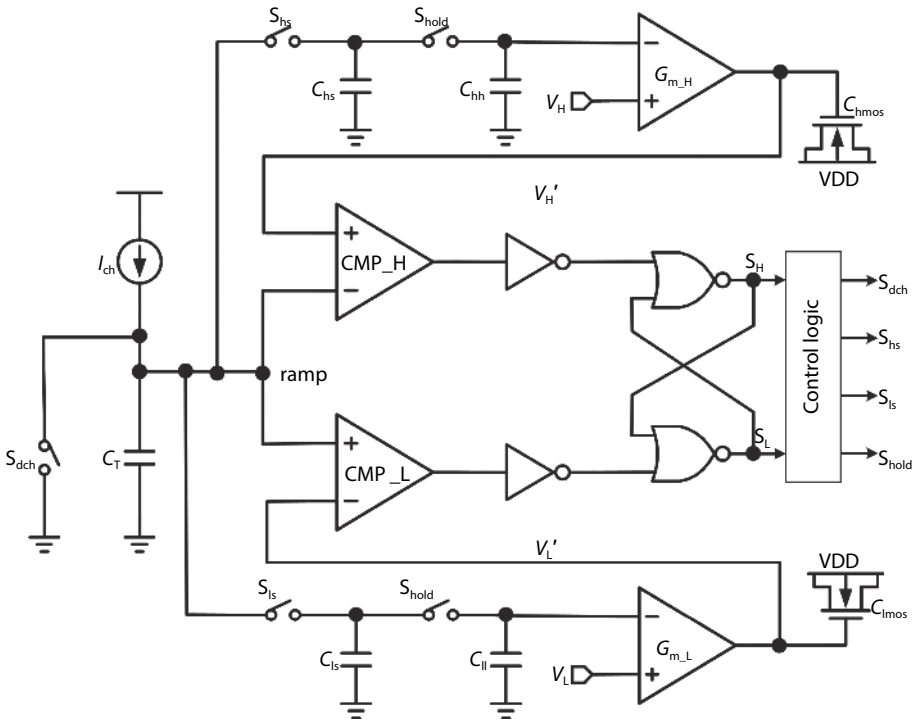


Fig. 10. Schematic of the accurate ramp generator.

graded and the loop compensation becomes complicated. When employing the hybrid scheme to improve transient responses of DC–DC converters, it is essential that the linear regulators are deactivated in the steady state to eliminate quiescent consumption. Thus, the main challenge is to activate and deactivate the linear regulators accurately. They should be activated timely to reduce overshoot and undershoot should large load transients occur, and should be completely deactivated after the output voltage has settled. Adequate noise margins should be spared to avoid false activation, and the transition between activation and deactivation should be smooth and seamless. In Ref. [27], load transients cannot be detected automatically, and the converter has to be informed by a processor that may not be available in a real application. In Refs. [28–30], a voltage detector is used to monitor the output voltage within the steady-state window. If the output voltage swings outside this window, the hybrid scheme will be activated. However, the guideline of designing such a window is not clear. If the window is too wide, the improvement using the hybrid scheme is compromised; if it is too narrow, the hybrid scheme may be wrongly activated in the steady state. In Ref. [31], the hybrid scheme is activated based on the difference between the sensed AC and DC inductor currents, and a detector window is still needed.

### 3.2. Proposed hybrid scheme

The concept of the proposed $V_{ea}$-based hybrid scheme is as follows. With reference to Fig. 7, $V_{ea}$ stays within the range of the ramp signal ($V_{ramp}$) to generate a proper duty cycle for the power stage in the steady state, while it will jump out of $V_{ramp}$ if a large load transient occurs. By using the delay-compensated ramp generator proposed in Ref. [23], the ramp signal can be accurately bounded by the high threshold voltage $V_H$ and the low threshold voltage $V_L$. It means that the voltage level of $V_{ea}$ can be used to detect the load transients, and $V_H$ and $V_L$ can naturally serve as the window boundaries of the detector. The schematic of the accurate ramp generator is shown in Fig. 10. As $V_{ea}$ is an internal node, it has much better noise immunity than $V_o$, and monitoring $V_{ea}$ can reduce undershoot and overshoot more effectively.

As shown in Fig. 11, a simple digital linear regulator is im-

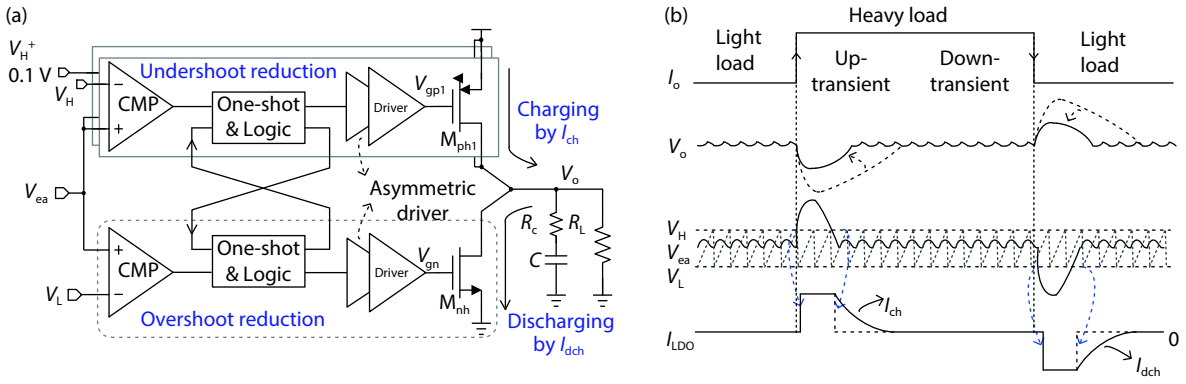


Fig. 11. (Color online) The proposed hybrid scheme: (a) simplified schematic, (b) working principle.

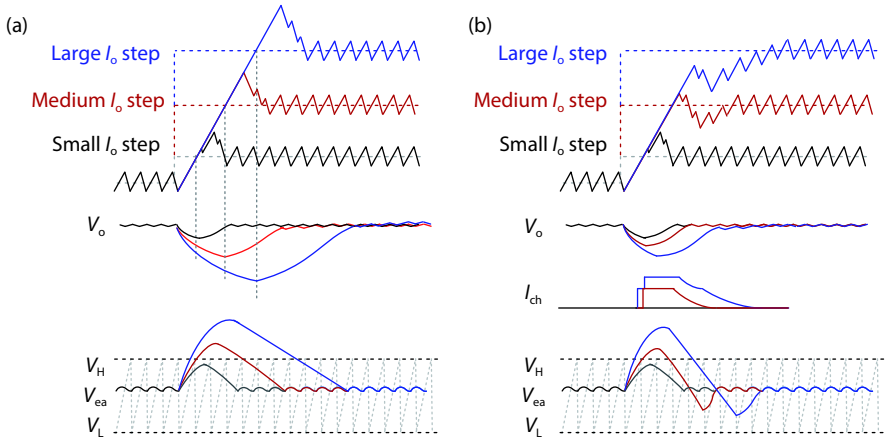


Fig. 12. (Color online) Transient responses of the proposed converter (a) with PWM control only, (b) with the hybrid scheme.

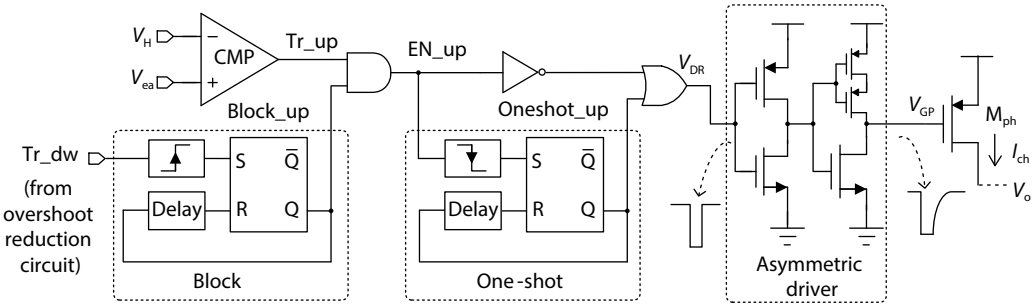


Fig. 13. The detailed implementation of undershoot reduction branch circuit.

plemented to verify the proposed scheme. Consider the up-transient as an example. As shown in Fig. 12, when the $I_o$ step is small, the droop voltage is also small due to the fast PWM control. $V_{ea}$ stays within the range of $V_{ramp}$ all the time and the hybrid scheme will not be activated. When the $I_o$ step is medium, the undershoot reduction circuit will be activated immediately when $V_{ea}$ swings higher than $V_H$, providing the charging current $I_{ch}$ to charge the output capacitor. Note that as $D$ = 1, the inductor current keeps ramping up; and the PWM loop works as normal without being interrupted. Therefore, only a small $I_{ch}$ is needed. The undershoot reduction circuit is automatically deactivated when $V_{ea}$ swings lower than $V_H$. When the $I_o$ step is very large, the corresponding $I_{ch}$ can be increased according to the voltage level of $V_{ea}$ to reduce the droop voltage more effectively. For example, in this design, if $V_{ea}$ swings higher than $V_H$ + 0.1 V, one more branch will be activated to increase $I_{ch}$. Therefore, the transient responses of the converter can be optimized for different $I_o$ steps.

Fig. 13 shows the detailed implementation of the undershoot reduction circuit. Fig. 14 shows the simulated waveforms of the related signals during an up-transient. As the undershoot reduction circuit and the overshoot reduction circuit should not be activated at the same time, the undershoot reduction circuit will be disabled if the overshoot reduction circuit is activated (if Tr_dw is "1") to avoid potential false triggering, and vice versa. When $V_{ea}$ is higher than $V_H$ and Block_up is "0", EN_up will be "1" to turn on the power transistor $M_{ph}$. A simple one-shot scheme is also implemented so that the circuits will be activated only once per transient for robust operation. $M_{ph}$ is turned on fast to reduce the droop voltage. However, as the inductor current cannot be changed too quickly, $M_{ph}$ is better to be turned off slowly; otherwise the output voltage may drop again. Therefore, an asym-

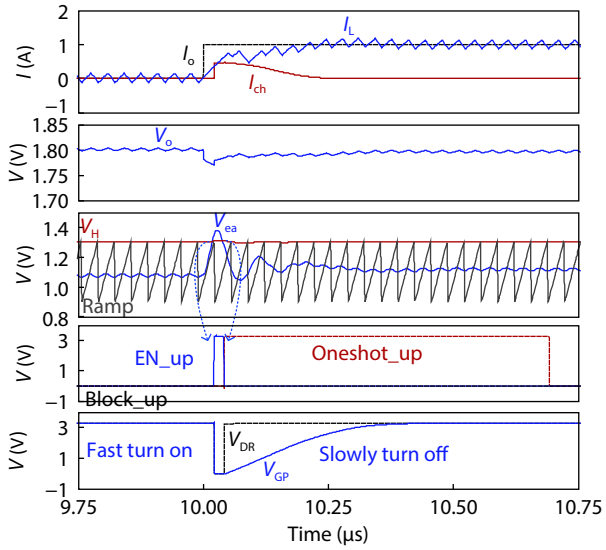


Fig. 14. (Color online) Simulated waveforms of the proposed hybrid scheme during an up transient.

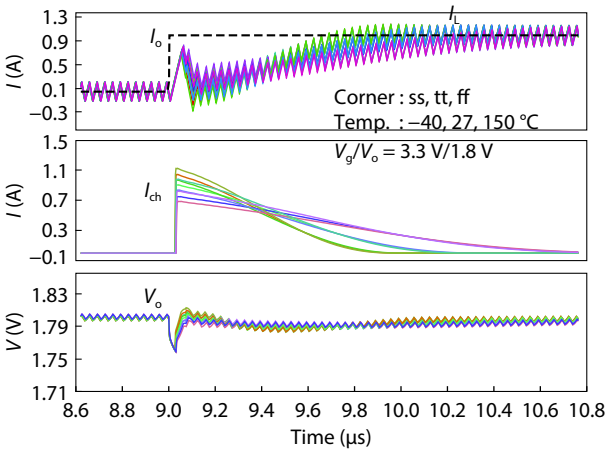


Fig. 15. (Color online) Simulated transient responses of the proposed hybrid scheme.

metric driver is employed to slowly turn off $M_{ph}$ for smooth transition. Fig. 15 further shows the simulated transient responses at different temperatures and process corners during an up-transient, and all situations have a fast response. As a proof of concept design, we only implemented two branches for undershoot reduction and one branch for overshoot reduction, and the charging and discharging currents are controlled by the sizes of the power transistors that are determined based on the simulation results. A finer control of the charging and discharging currents with more branches can be implemented as those discussed in Refs. [36–38].

## 4. Measurement results

The proposed buck converter was fabricated in a standard 0.13 $\mu$m CMOS process using 3.3 V devices. Fig. 16 shows the chip micrograph that measures 1500 × 800 $\mu m^2$ including testing circuits and pads. For the following tests, the nominal input and output voltages are fixed at 3.3 and 1.8 V, respectively, with a 90 nH inductor and two 0.47 $\mu$F capacitors. Fig. 17 shows the measured steady-state waveforms of the output voltage $V_o$ and the switching node $V_{LX}$ when the loading current $I_o$ is 1 A and 24 mA, respectively. The operation

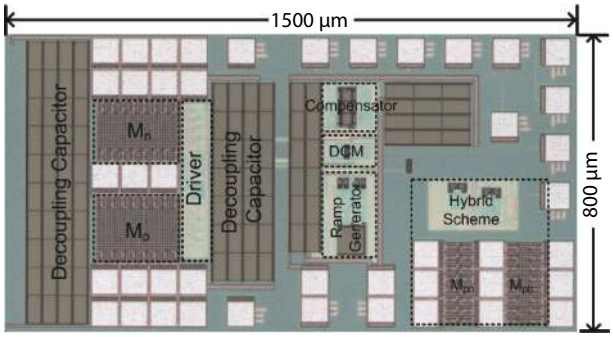


Fig. 16. (Color online) Chip micrograph.

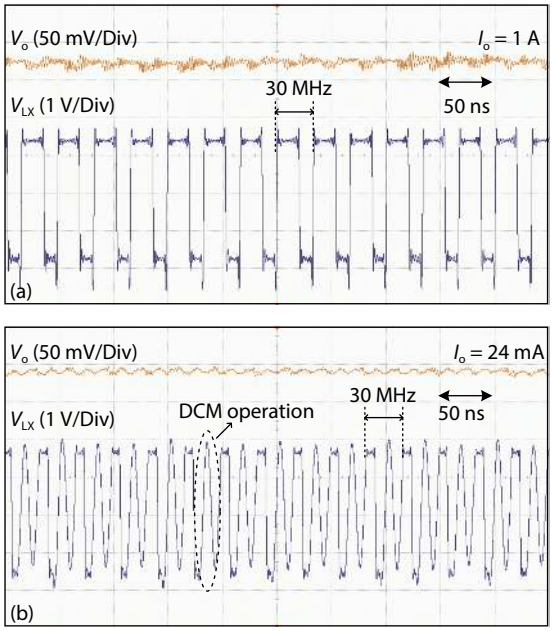


Fig. 17. (Color online) Measured steady-state waveforms when (a) $I_o$ = 1 A (CCM), (b) $I_o$ = 24 mA (DCM).

modes can be identified from the waveforms of $V_{LX}$. The converter is working in CCM when $I_o$ is 1 A and in DCM when $I_o$ is 24 mA, respectively. However, when $I_o$ is smaller than 15 mA, $V_o$ will increase when $I_o$ decreases. It is because the minimum on-time of the system is larger than the duty cycle required by the DCM loop. The remedy is to employ a pulse-skipping mode at very light load[39].

Fig. 18 shows the measured power efficiency at different load currents and output voltages. The peak efficiencies at $V_o$ = 2.4, 1.8, and 1.2 V are 90.7%, 88% and 83.6%, respectively. Compared to the results reported in Ref. [23], the light-load efficiency is greatly improved by employing DCM operation and the adaptive sizing method.

Fig. 19 shows the measured load-transient responses with PWM control only. With an $I_o$ step of 1.25 A and rise and fall times of 2 ns, the undershoot and overshoot are around 72 and 76 mV only, and the 1% settling times are around 220 and 230 ns, respectively. The zoom-in waveform of $V_{LX}$ during the up-transient indicates that the power PMOS transistor $M_p$ is always ON to ramp up the inductor current quickly, verifying that the proposed compensator can achieve near-optimal transient responses.

Fig. 20 shows the measured transient responses with and without the proposed hybrid scheme at different $I_o$ steps. For the same $I_o$ step of 1.25 A as shown in Fig. 19, the measured

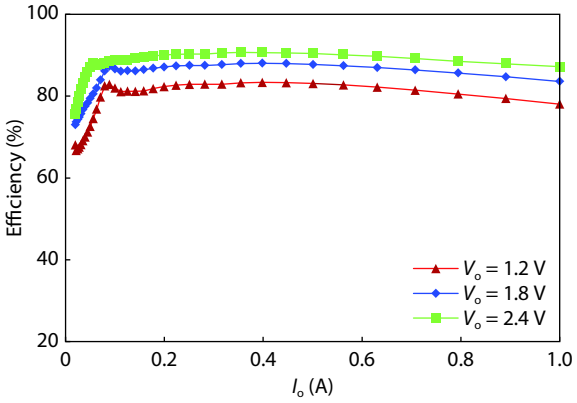


Fig. 18. (Color online) Measured power conversion efficiencies at different $V_o$.

undershoot and overshoot with the hybrid scheme activated are further reduced by more than 50% to 36 and 38 mV. The 1% settling times are also reduced to 125 ns with a smooth and seamless transition. For $I_o$ steps of 0.93 and 0.62 A, the transient responses are improved by the proposed hybrid scheme consistently. For a small $I_o$ step of 0.31 A, the undershoot and overshoot of the converter with PWM control is within 1% of $V_o$. Note that even $V_o$ has some spikes that are due to the transient testing circuits, the hybrid scheme will not be incorrectly activated by the spikes, demonstrating the robustness of the proposed scheme.

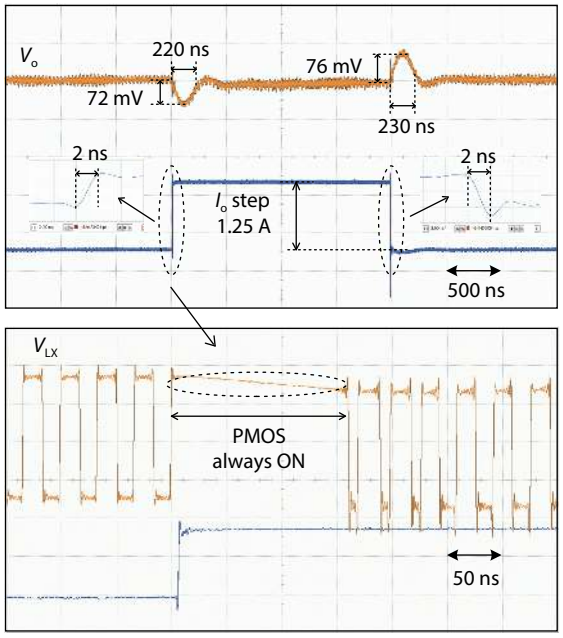


Fig. 19. (Color online) Measured load-transient responses of the converter.

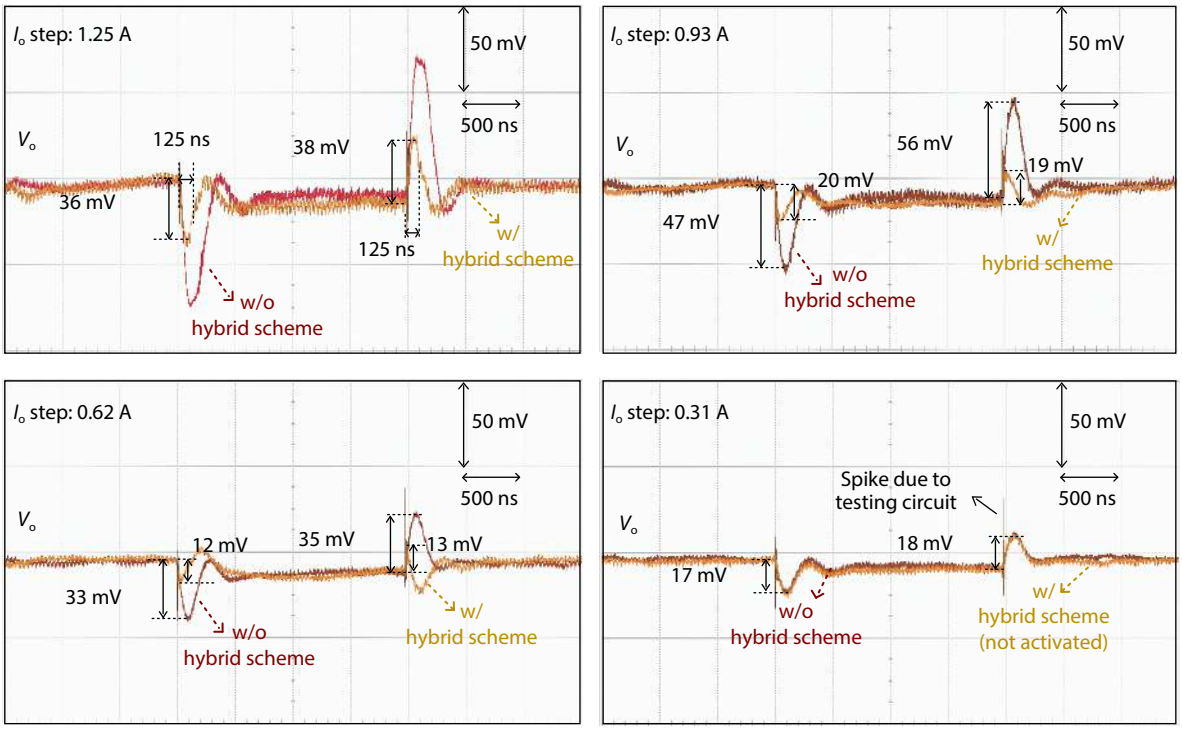


Fig. 20. (Color online) Measured load-transient responses of the converter with and without the proposed hybrid scheme.

Table 1 summarizes and compares the performance of the proposed buck converter with state-of-the-art designs. The transient responses achieved by simple PWM control are comparable with those using advanced hysteretic control or other transient optimization techniques, and they are further improved by the proposed $V_{ea}$-based hybrid scheme.

## 5. Conclusions

This paper presents a voltage-mode controlled buck converter with an improved DDA-based Type-III compensator and a hybrid scheme to achieve fast transient responses. Compare to the previous DDA-based Type-III compensator, the new compensator has a simpler structure and can reduce the settling times during load transients. Based on the fast responses of the new compensator, a hybrid scheme with automatic transient detection and seamless loop transition is further proposed to improve the load-transient responses. By monitoring the output of the compensator instead of the out-

Table 1. Performance comparison with previously published works.

| Parameter | | 2012[28] | 2014[20] | 2015[24] | 2015[22] | 2016[13] | 2017[11] | This work[32] | |
|---|---|---|---|---|---|---|---|---|---|
| Technology ($\mu$m) | | 0.13 | 0.18 | 0.065 | 0.35 | 0.18 | 0.35 | 0.13 | |
| Switching frequency (MHz) | | 10 | 40 | 30 | 1 | 30 | 1 | 30 | |
| Inductor (nH) | | 1000 | 78 × 4 | 90 × 4 | 4700 | 220 × 4 | 4700 | 90 | |
| Capacitor ($\mu$F) | | 1 | 0.47 × 2 | 0.47 | 10 | 0.62 | 2.2 | 0.47 × 2 | |
| Nominal $V_g$ (V) | | 3.7 | 3.3 | 1.8 | 3.7 | 3.3 | 3.3 | 3.3 | |
| Nominal $V_o$ (V) | | 1.2 | 1.2 | 1.5 | 2 | 1.8 | 1.8 | 1.8 | |
| Peak efficiency (%) | | 84.5(@$V_o$= 1.2 V) | 86.1(@$V_o$= 1.6 V) | 87(@$V_o$=1 V) | 95.5(@$V_o$=2 V) | 86.5(@$V_o$= 2.5 V) | 91.9(@$V_o$= 2.5 V) | 90.7/88/83.6(@$V_o$= 2.4/1.8/1.2 V) | |
| Control scheme | | Voltage-mode+Hybrid | ZDS Hysteretic | Voltage-mode | Quasi current-mode hysteretic | Current-mode+ CCS/LTO | Voltage-mode | Voltage-mode only | Voltage-mode+ Hybrid |
| Up-transient | $I_o$ step (A) (rise time (ns)) | 0.3 (20) | 5 (5) [4 phases] | 0.4 (10) [4 phases] | 0.4 (10) | 1.8 (5) [4 phases] | 0.27 (NA) | 1.25 (2)/0.62 (2) | |
| | $V_o$ droop (mV) (% of $V_o$) | 55 (4.6) | 118 (9.8) | 80 (5.33) | 35 (1.75) | 100 (5.6) | 19 | 72/33 (4/1.83) | 36/12 (2/0.67) |
| | 1% settling time (ns) | 1500 | 230 | 600 | 4800 | 133 | 1200 | 220/150 | 125/0* |

*Droop voltage is less than 1%.

put of the converter, the proposed hybrid scheme can reduce undershoot and overshoot effectively with good noise margin. The proposed buck converter was fabricated in a standard 0.13 $\mu$m CMOS process, and experimental results verify the effectiveness of the proposed techniques. The converter achieves comparable performance of load transient responses among state-of-the-art designs with simple circuit implementation.

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