Research Square

Preprints are preliminary reports that have not undergone peer review.
They should not be considered conclusive, used to inform clinical practice,
or referenced by the media as validated information.

A Wide Tuning Range High Performance PLL Based on Capacitor Arrays

Jun Liu

liujun_421@126.com

University of Electronic Science and Technology of China

Qian Ma

Chongqing GigaChip Technology Co.Ltd

Ning Ning

University of Electronic Science and Technology of China

Chao Li

Chongqing GigaChip Technology Co.Ltd

Shibi Ma

Chongqing GigaChip Technology Co.Ltd

Linqing Huang

Chongqing GigaChip Technology Co.Ltd

Dongbing Fu

Chongqing GigaChip Technology Co.Ltd

Article

Keywords: PLL, wide tuning range, capacitor arrays

Posted Date: August 6th, 2024

DOI: https://doi.org/10.21203/rs.3.rs-4715413/v1

License: This work is licensed under a Creative Commons Attribution 4.0 International License.
Read Full License

Additional Declarations: No competing interests reported.

Abstract

The paper presents a wide tuning range high performance PLL, which is mainly used for high speed wideband clock signal generation to reduce the difficulty of providing high-speed input clocks externally. The circuit mainly consists of PFD, CP, VCO, DIVIDER and other units. It improves the phase noise of the VCO by reducing the VCO tuning gain, and uses a capacitor array to extend the output frequency range. The circuit is designed in a 28nm process and the output signals can work from 8GHz to 12GHz. The PLL is used as a sampling clock for the DAC. When the DAC outputs a 1.8GHz sine wave, the measured phase noise can reach -110dBc/Hz@100kHz offset.

I. INTRODUCTION

In electronic systems, especially in communication systems, electronic measurement, instrumentation and other fields, the quality of the clock directly affects the performance of the whole system. PLL can realize clock frequency doubling, phase tracking, clock recovery and other functions, and is a commonly used circuit for clock generation. Wide tuning range PLL can accurately lock and track the phase and frequency of the input signal over a wide frequency range, thus realizing more flexible and efficient frequency synthesis and control [1–7].

II. DESIGN OF THE WHOLE PLL STRUCTURE

This wide tuning range PLL circuit is designed in a 28nm process and can output 8GHz ~ 12GHz signal. It mainly contains: PFD, CP, off-chip LPF, LC VCO, feedback frequency divider and other units, in which the VCO is designed with a band-selective Auto Frequency Calibration (AFC) algorithm to improve the performance of the phase-locked loop. The general block diagram of the circuit is shown in Fig. 1.

In Fig. 1, the PFD outputs a pulse signal proportional to the phase difference between Fin and the feedback divider output signal Fdiv by comparing the phase difference of Fin and the feedback divider output signal Fdiv, and then this pulse signal serves as the control signal of the CP, which decides the CP to charge or discharge the LPF in the back stage. At the same time, the LPF converts the high-frequency current pulse signal into a low-frequency voltage signal FILT_FINE after filtering, and then this voltage signal controls the output frequency of the VCO, and finally, the output signal of the VCO is divided by the frequency divider of the feedback loop for 8*N frequency division, and then outputs the signal fdiv and serves as one of the input signals of the PFD, and finally, under the effect of the negative phase feedback in the loop, the PLL reaches a stabilized state and locked at the frequency: $8N*F_{in}/M$.

III. DESIGN OF THE MAIN UNITS

A. *Phase Frequency Detector*

The Phase Frequency Detector(PFD) is used to detect the difference in phase and frequency between the reference signal and the frequency-divided feedback signal.The outputs of the PFD are UP and DOWN

pulses, and the difference between the pulse widths of these two pulses is directly proportional to the difference in phase between REFCLK and FBCLK. It mainly consists of D flip-flops, NAND gate and programmable delay line as shown in Fig. 2.

When the frequency of REFCLK is higher than FBCLK or the phase is ahead, the pulse width of UP signal will be larger than that of DOWN signal; when the frequency of REFCLK is lower than FBCLK or the phase is lagged, the pulse width of UP signal will be smaller than that of DOWN; when REFCLK and FBCLK are in the same frequency and the same phase, the pulse width of UP signal is equal to that of DOWN. The UP and DOWN waveforms in different cases are shown in Fig. 3.

The purpose of the delay unit in the RESET signal path is to ensure the complete establishment of the UP and DOWN pulse waveforms when the phase difference is small, so that the charge/discharge switch of the CP unit does not turn on completely, thus avoiding the dead zone. The delay time should be considered as a compromise, if the delay time is too small, then the CP switch can not be fully opened; if the delay time is too large, then the CP conduction time is long, contributing to the current noise.

B. *Charge Pump*

The Charge Pump (CP) unit takes the UP and DOWN pulses generated by the PFD and converts them into current signals. The current switching and inflow/outflow are controlled by the UP and DOWN pulses.The CP unit mainly consists of a bias circuit, a current source, and a switch and an auxiliary op-amp, and the basic structure is shown in Fig. 4.

The AMP1 and M1 circuits enable the M1 branch to generate bias currents related to the Ibias, where the Rcp resistance value is variable, thus realizing the adjustability of the charge pump current. The auxiliary op-amp AMP2 makes the V1 and V2 node voltages equal to avoid the channel length modulation effect that causes current bias.

Rpmis and Rnmis resistance value is variable, in the calibration mode, the charge pump operating mode is shown in Fig. 5, at this time V1 = VDD/2, if you find that FILT_FINE is not equal to V1, then it means that there is a mismatch between the charge pump PMOS branch and the NMOS branch currents, and by adjusting the resistance value of Rpmis or Rnmis can be adjusted to the charge pump mismatch current.

C. *Voltage Controlled Oscillator*

The Voltage Controlled Oscillator(VCO) utilizes a standard LC resonant cavity, which consists of two differential inductors, two variable capacitor arrays, a switched capacitor array, and complementary NMOS and PMOS negative resistors. The variable capacitor array is controlled by the charge pump output voltage, which can make the frequency change continuously to realize the frequency fine tuning; the switched capacitor array is controlled by the AFC algorithm, which can carry out the frequency selection to realize the coarse tuning. The negative resistance can be used to offset the parasitic resistance in the LC oscillator to ensure the stability of the resonance. The circuit structure is shown in Fig. 6.

The variable capacitor array is shown in Fig. 7, which is controlled by two control signals, SW1 < 3:0 > and SW0 < 3:0>. When the control signal is 0, the MOS capacitors C1 and C2 are connected to VDD; when the control signal is 1, the MOS capacitor C1 is connected to the voltage FILT_FINE, and the finely tuned branch is on, and the MOS capacitor C2 is connected to the voltage FILT_COARSE, and the coarsely tuned branch is on. Among them, the size of coarse tuning branch MOS capacitor C2 is 8 times of fine tuning branch MOS capacitor C1.

D. *Feedback Frequency Divider*

The VCO output signal is divided and fed to the PFD, but since the VCO output signal frequency is very high, the frequency divider used in this paper is accomplished in two stages. The first stage is a high-speed prescaler circuit, as shown in Fig. 8, which is first divided into 2 by a D flip-flop, and then divided into 4 by two D flip-flops, thus constituting an 8-division circuit, and in order to meet the high-speed requirements, the D flip-flop is realized by a TSPC circuit. The second stage is a conventional integer frequency divider. Therefore, the frequency divider circuit in this paper is an 8*N times frequency divider.

E. *Digital Automatic Frequency Calibration*

In order to meet the wide tuning range, the VCO uses a capacitor array to realize multiple frequency tuning sub-bands to extend the output frequency coverage, so the PLL needs to quickly and accurately select the appropriate VCO frequency tuning sub-bands through the Auto Frequency Calibration (AFC) circuit. The analog loop then controls the tuning voltage of the VCO through its own negative phase feedback until the loop locks. The block diagram of AFC is shown in Fig. 9.

The AFC algorithm uses the frequency comparison method to realize calibration by comparing the frequency of the output divider signal Fdiv and the reference signal Fin. Before digital calibration, it is necessary to disconnect the analog calibration loop, and at the same time, the tuning voltage of the VCO is set to a fixed value of Vref, the counter counts the frequency of Fdiv for a certain period of time, and then compares the counted value and the target counted value, and the control logic adjusts the VCO capacitance array control word according to the counting result to regulate the frequency of the VCO.

F. *Analog Calibration*

After the digital calibration finds the sub-band it also needs to be locked by analog calibration, the analog calibration loop is shown in Fig. 10.

The PFD compares the phase information of Fin and Fdiv to control the CP charging and discharging, and the CP charging and discharging currents are converted to the fine-tuned voltage FILT_FINE through the LPF to regulate the frequency of the VCO until the phase alignment of the Fin and Fdiv frequencies are equal, then the PLL completes the locking, and the fine-tuned voltage FILT_FINE is kept unchanged. In addition, the inclusion of a coarse tuning loop consisting of a Gm-C integrator allows the fine tuning voltage FILT_FINE to be controlled at Vref during lock. For example, if FILT_FINE is greater than Vref,

FILT_COARSE increases, the variable capacitor capacitance becomes smaller, Fdiv increases, the CP discharges, and FILT_FINE decreases until it decreases to Vref, and FILT_COARSE stabilizes.

IV. SUMMARY

This wide tuning range PLL circuit is designed in a 28nm process and the layout is shown in Fig. 11.

This wide tuning range PLL circuit is applied in a high-speed DAC for generating an internal sampling clock. The DAC works at 12 GSPS and outputs a 1.8 GHz sine wave, the measured phase noise can reach − 110dBc/Hz@100kHz offset. The results of the test phase noise are shown in Fig. 12.

Declarations

Author Contribution

Jun Liu wrote the main manuscript text, and all authors reviewed the manuscript.

Acknowledgement

The authors would like to acknowledge the contributions of Yi Ding, Jiandong Zang, Gang Li, Yidan Dai, and Lingrui Zhang.

Data Availability

The datasets used and/or analysed during the current study available from the corresponding author on reasonable request.• All data generated or analysed during this study are included in this published article.

References

1. Mark Ferriss et al., “An Integral Path Self-Calibration Scheme for a Dual-Loop PLL,” IEEE Journal of Solid-State Circuits, vol. 48, no.4, pp. 996-1008, April. 2013.
2. Vamshi Manthena et al., “A 1.2V 2.4 GHz low spur CMOS PLL synthesizer with a gain boosted charge pump for a batteryless transceiver,” IEEE Symposium on Radio Frequency Integrated Technology (RFIT), Nov. 2012.
3. A. Loke et al., “A versatile 90-nm CMOS charge-pump PLL for SerDes transmitter clocking,” IEEE Journal of Solid-State Circuits, vol. 41, no.8, pp. 1894-1907, Aug. 1998.
4. Juan Xie et al., “A low power low phase noise dual-band multiphase VCO,” Journal of Microelectronics, vol. 43, no. 12, pp. 1016-1022, Dec. 2012.

5. Sung-Geun Kim, Jinsoo Rhim, Dae-Hyun Kwon, Min-Hyeong Kim, “A Low-Voltage PLL With a Supply-Noise Compensated Feedforward Ring VCO,” IEEE Journals & Magazines, vol. 63, no. 6, pp. 548-552, 2016.
6. Kwang-Chun Choi, Sung-Geun Kim, Seung-Woo Lee, Bhum-Cheol Lee, and Woo-Young Choi, “A 990uW 1.6-GHz PLL Based on a Novel Supply-Regulated Active Loop Filter VCO,” Journal of latex class files, vol. 6, no. 1, pp. 1-5, Jan 2007.
7. M. Hufford, et al., “An improved wideband PLL with adaptive frequency response that tracks the reference,” IEEE Custom Integrated Circuits Conf., pp. 549–552, Sep. 2005.

Figures

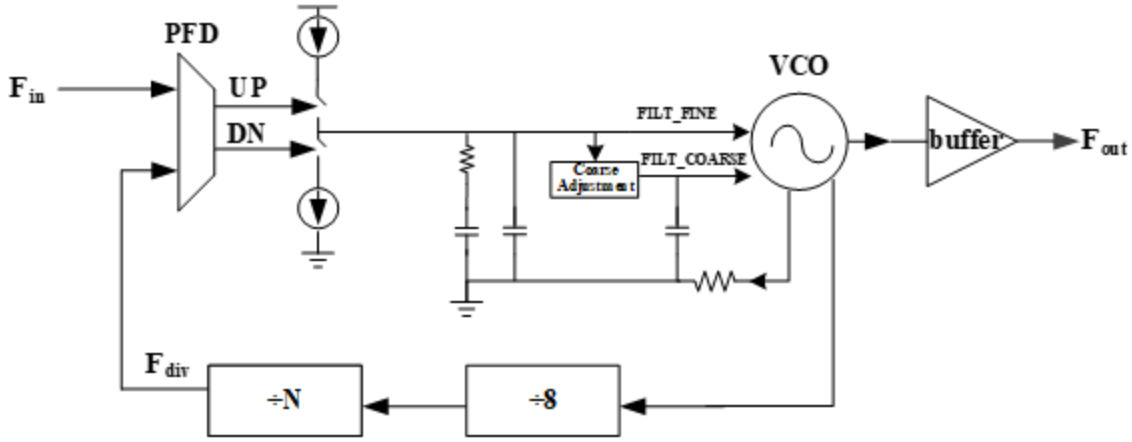

Figure 1

PLL General Block Diagram

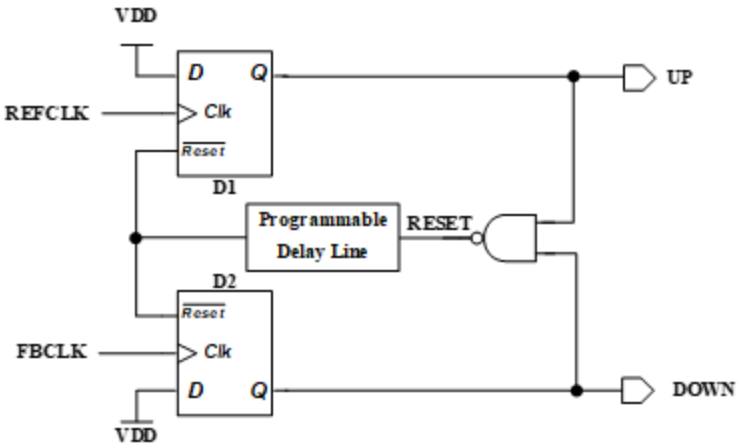

Figure 2

Schematic diagram of PFD circuit

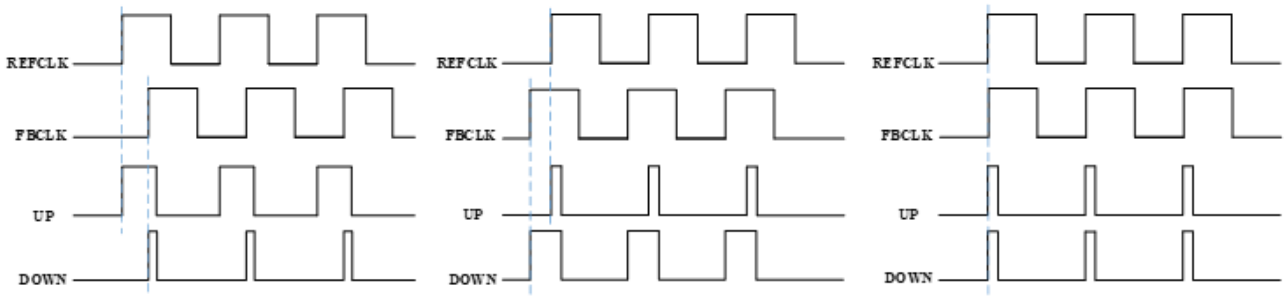

Figure 3

Waveforms of UP and DOWN

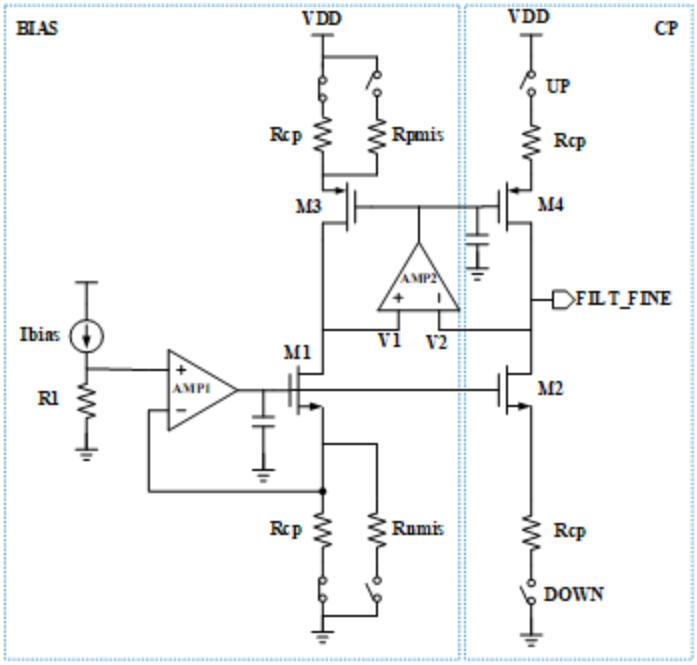

Figure 4

Schematic of charge pump circuit

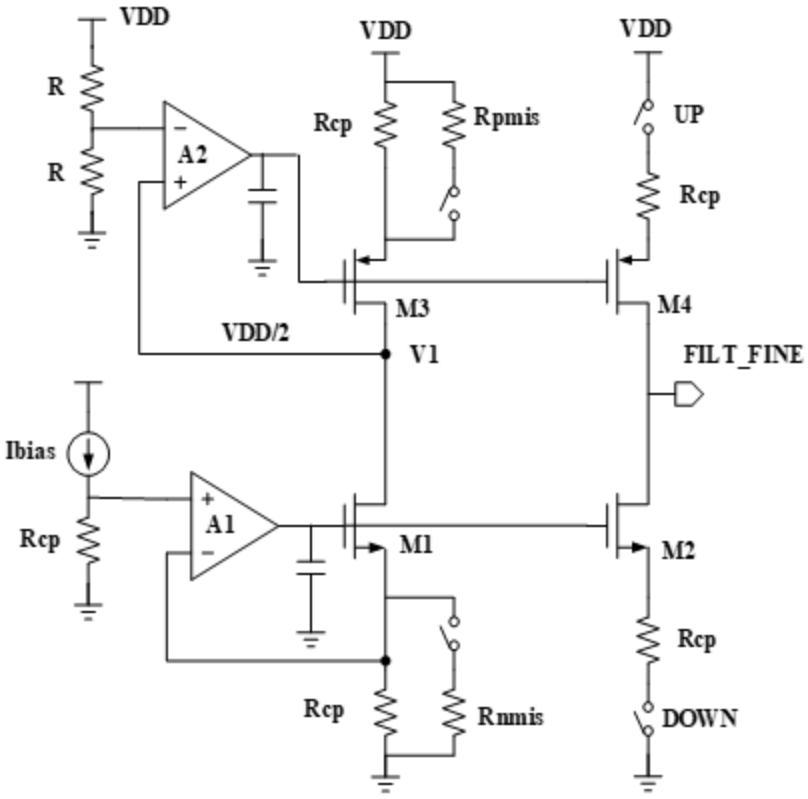

Figure 5

Charge Pump Circuit Diagram in Calibration Mode

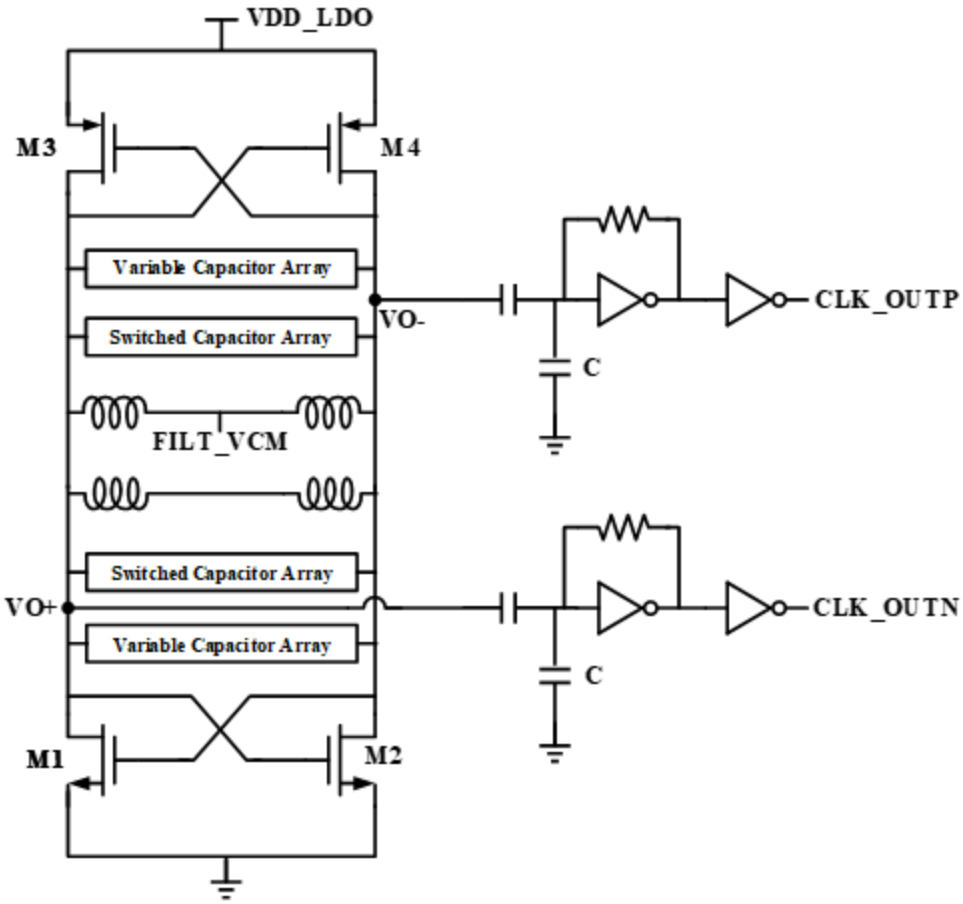

Figure 6

LC VCO Circuit Diagram

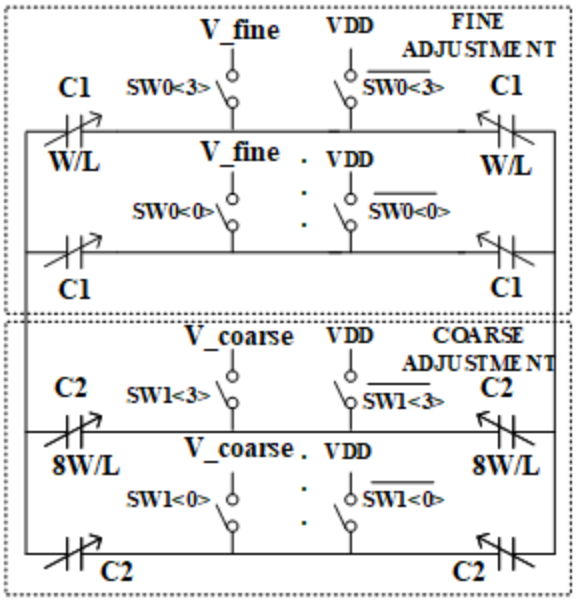

Figure 7

Variable Capacitor Array Circuit Diagram

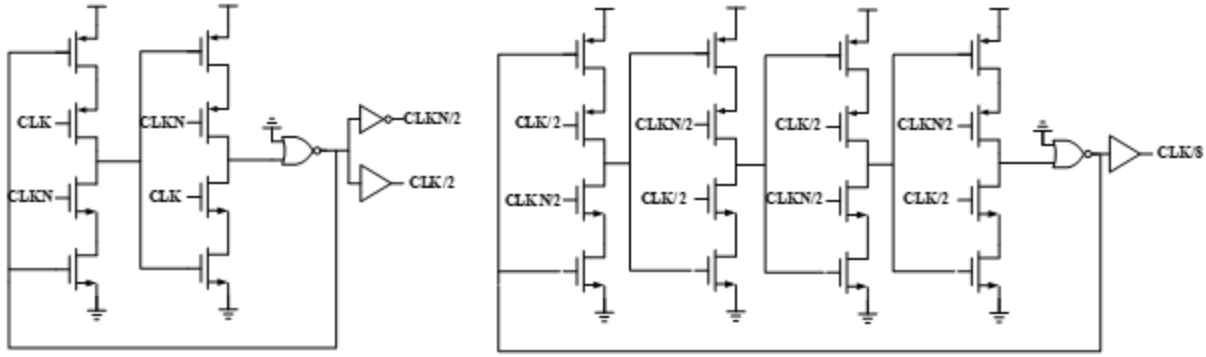

Figure 8

High Speed Pre-Divided Circuit Diagram

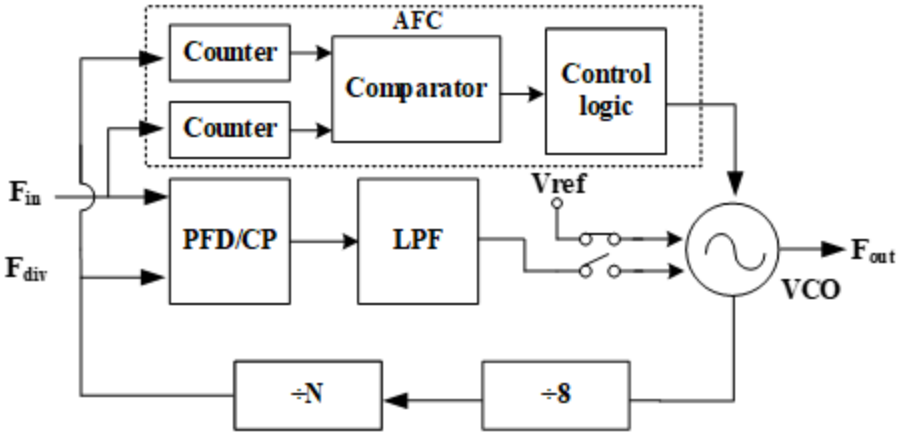

Figure 9

Block diagram of AFC

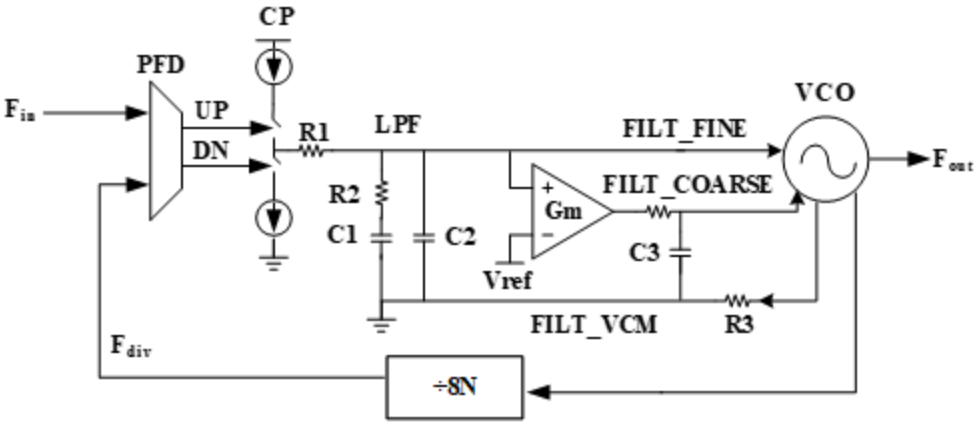

Figure 10

Circuit diagram of analog calibration loop

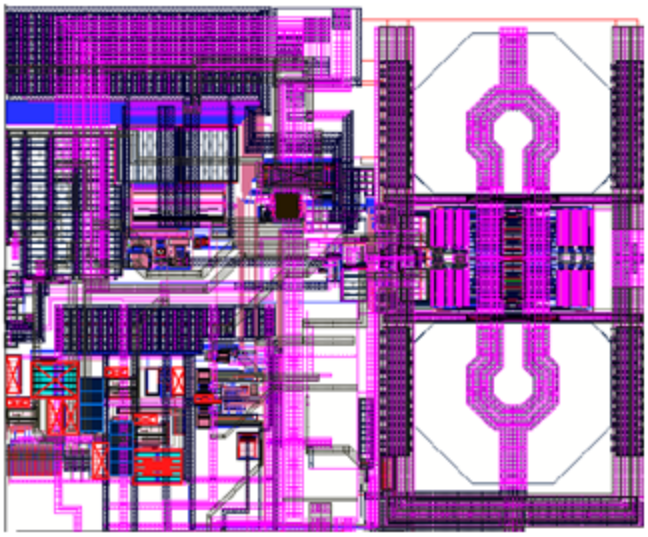

Figure 11

The layout of the circuit

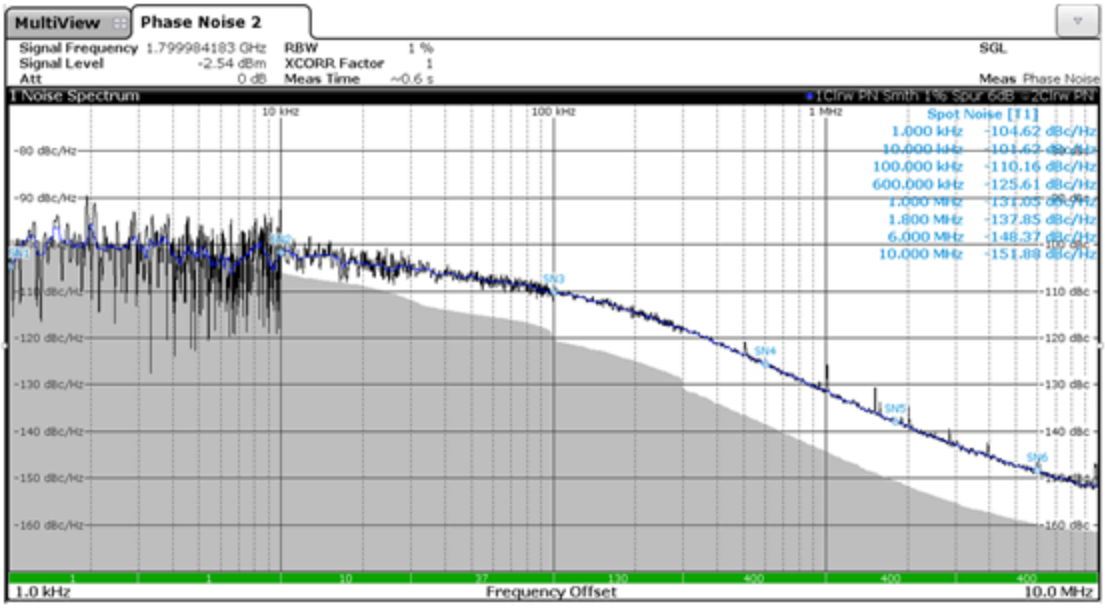

Figure 12

The phase noise of the output waveform