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Qualitative Analysis of High Gain Small-signal Amplifier with MOSFET Current Mirror

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Abstract

A small-signal high voltage gain amplifier with two identical MOSFET current mirrors is proposed and analyzed on the qualitative scale. In the narrow band (bandwidth 4.093KHz) performance range, the proposed amplifier produces high voltage gain (141.883), almost constant output current (excursion range 1.24mA to 1.25mA) and considerably low THD (0.658%). This amplifier is capable to amplify audio range AC signals swinging in 0.01mV to 5mV range at 1KHz frequency. Tuning performance of this amplifier in specific audible frequency range explores its suitability in radio and TV receiver stages. Variation of voltage gain with frequency and different biasing resistances, input and output noises at various operating frequencies, temperature dependency of performance parameters and total harmonic distortion of the amplifier are examined to provide a wide spectrum to the qualitative analysis.

Keywords: Small-signal MOSFET amplifiers, Current Mirrors, Circuit synthesis, Circuit simulation

INTRODUCTION

Current mirror is one of the most common building blocks in analog and mixed-signal VLSI circuits. It is a joint unit of two active devices of identical nature, designed to provide constant current [1]-[6]. This circuit mirrors the current flowing in one active device into another, keeping the output current constant regardless of loading. The current being mirrored can be a constant current, or it can be a varying signal depending on the circuit requirement. [1], [4], [6]-[7].

Current mirrors are usually an integral part of analog signal processing elements like op-amps, current conveyors, current feedback pair amplifiers and offers the advantages of low-voltage operation, derivation of resistor-less topologies and electronic adjustment capability of their frequency characteristics [3]-[7]-[8]. Though it has high applicability in IC designing but the attempts are still being made to design amplifier circuits using current mirrors. BJT current mirror circuit by Comer [6], [9] and MOSFET current mirror circuit by Wang [10] are among few to mention the efforts for development of small-signal amplifiers using this topology.

The present manuscript focuses on an amplifier design which uses two MOSFET current mirrors in differential mode to provide high voltage gain as its prominent feature.

BASIC MOSFET CURRENT MIRROR

Design procedure for MOSFET current mirror primarily depends on the channel width which affects the trans-conductance, output resistance, capacitance, and the mid-band voltage gain of the mirror stage [11].

Fig.1 shows the basic circuit of a MOSFET current mirror [1], [7], [9], [11], [12]. MOSFETs M_1 and M_2 ideally have identical characteristics. A reference current I_{REF} provides operating bias to the mirror, whereas I_O is the output current of the mirror circuit. Current mirror is designed to have $I_O=I_{REF}$ or in other words the output current, mirrors the reference current.

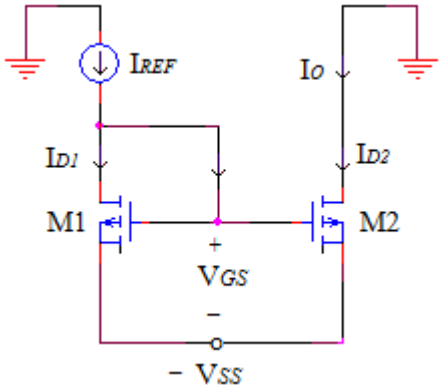

Fig.1. Basic circuit of a MOSFET current mirror

Because the gate currents are zero for the MOSFETs, reference current I_{REF} must flow into the drain of M_1, which is forced to operate in pinch-off by the circuit connection because $V_{DS1} = V_{GS1} = V_{GS}$. V_{GS} must equal the value required for $I_{D1} = I_{REF}$.

Assuming devices are well matched [11]

$$I_{REF} = \frac{1}{2}K_n(V_{GS1} - V_{TH})^2(1 + \lambda V_{DS1}) \qquad (1)$$

Where K_n is a technological constant associated with the transistors of the mirror and λ is the channel length modulation constant.

$$V_{GS1} = V_{TH} + \sqrt{\frac{2I_{REF}}{K_n(1 + \lambda V_{DS1})}}$$

Current I_O is equal to the drain current of M_2, therefore-

$$I_O = I_{D2} = \frac{1}{2}K_n(V_{GS2} - V_{TH})^2(1 + \lambda V_{DS2}) \qquad (2)$$

but the circuit connection forces $V_{GS2} = V_{GS1}$ and $V_{DS1} = V_{DS2}$. Substituting Eq. (1) into Eq. (2) yields

$$I_O = I_{REF}\frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})} \cong I_{REF} \qquad (3)$$

For equal values of V_{DS}, the output current is identical to the reference current (that is, the output mirrors the reference current). Unfortunately in most circuit applications, $V_{DS2} \neq V_{DS1}$, and there is a slight mismatch between the output current and the reference current.

For convenience, the ratio of I_O to I_{REF} is to be defined as 'mirror ratio' MR [9], [11]-[12] given by

$$MR = \frac{I_O}{I_{REF}} = \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})}$$

The power of the current mirror is greatly increased if the mirror ratio can be changed from unity.

For the MOS current mirror, the ratio can easily be modified by changing the *W/L* ratios of the two transistors $\left(\frac{W}{L}\right.$ is the width to length ratio of transistor $\left.\right)$ forming the mirror. In Fig.1, for example, remembering that $K_n = K_n'\left(\frac{W}{L}\right)$ for the MOSFET, the K_n values of the two transistors are given by

$$K_{n1} = K_n'\left(\frac{W}{L}\right)_1 \quad and \quad K_{n2} = K_n'\left(\frac{W}{L}\right)_2$$

Substituting these two different values of K_n in Eqs. (1) and (2) yields

$$I_O = I_{REF}\frac{K_{n2}(1 + \lambda V_{DS1})}{K_{n1}(1 + \lambda V_{DS1})} = I_{REF}\frac{\left(\frac{W}{L}\right)_2(1 + \lambda V_{DS2})}{\left(\frac{W}{L}\right)_1(1 + \lambda V_{DS1})}$$

The mirror ratio [9], [11]-[12] is given by

$$MR = \frac{\left(\frac{W}{L}\right)_2(1 + \lambda V_{DS2})}{\left(\frac{W}{L}\right)_1(1 + \lambda V_{DS1})}$$

In the ideal case ($\lambda = 0$) or for $V_{DS2} = V_{DS1}$, the mirror ratio is set by the ratio of the *W/L* values of the two MOSFETs.

DESCRIPTION OF CIRCUIT

Fig.2 shows the proposed amplifier circuit assembled with two MOSFET current mirrors [1]-[12] M2-M3 and M5-M6. Other MOSFETs M1, M4 and M7 and resistances in the circuits provide proper biasing and matching network to the available current mirrors [6], [9]. The amplifier is designed for AC applications and has narrow bandwidth which is determined by the fundamentally used capacitor C_A and optionally used capacitors C_{DS} and C_L (shown by dotted lines in Fig.2). TABLE I describes the circuit elements with respective values.

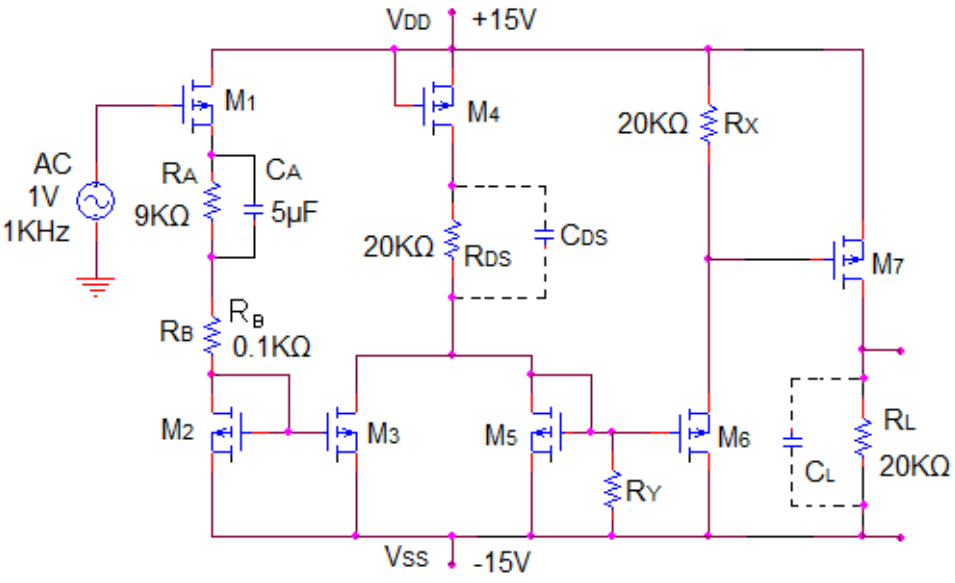

Fig.2. Proposed small-signal amplifier with MOSFET current mirrors

Table I: Description Of Circuit Components

Components	Proposed Amplifier
M1-M7 (N-MOSFETs with V_{TH}=2.831)	IRF150
R_A (Biasing resistance)	9KΩ
R_B (Biasing resistance)	0.1KΩ
R_{DS} (Biasing resistance)	20KΩ
R_X (Biasing resistance)	20KΩ
R_Y (Biasing resistance)	20KΩ
C_A (By-pass capacitor)	5μF
C_{DS} or C_L (optional Capacitors for tuning)	10nF-100μF (optional)
R_L (Load resistance)	20KΩ
DC Biasing Source V_{DD}	+15V DC
DC Biasing Source V_{SS}	-15V DC
Input AC Signal for fair output	1mV at 1KHz from 1V AC source

PSpice simulation (Student version 9.2) is performed to carry out present investigations [13]-[15]. Observations are procured by feeding the proposed amplifier circuit with 1V AC input signal source, from which, a small-distortion-less AC signal of 1mV at 1KHz frequency is drawn as input for the amplification purpose.

OBESRVATIONS AND DISCUSSIONS

Proposed amplifier circuit provides undistorted output for 0.01-5mV AC input signal at 1KHz frequency.

Fig.3 depicts the variation of voltage gain as a function of frequency. At biasing parameter of TABLE I, the proposed amplifier produces high level of voltage gain with a maximum value 141.883 along with an output waveform at 18^o phase difference respective to the input AC signal. In addition, proposed circuit holds narrow bandwidth response B_W (bandwidth B_W=4.093KHz, with lower-cut-off frequency f_L=229.899Hz and upper-cut-off frequency f_H=4.3237KHz) in audible lower frequency range below 5KHz. Moreover, the peak output current I_{OP} for the mentioned circuit is observed to be 1.2547mA which fluctuates in a small range from 1.2407mA to 1.2547mA. This decisively indicates that the current mirrors in the circuit responsibly provide constancy in the output current due to their basic properties whereas the presence of M4 and M7 ensures the voltage amplification [9].

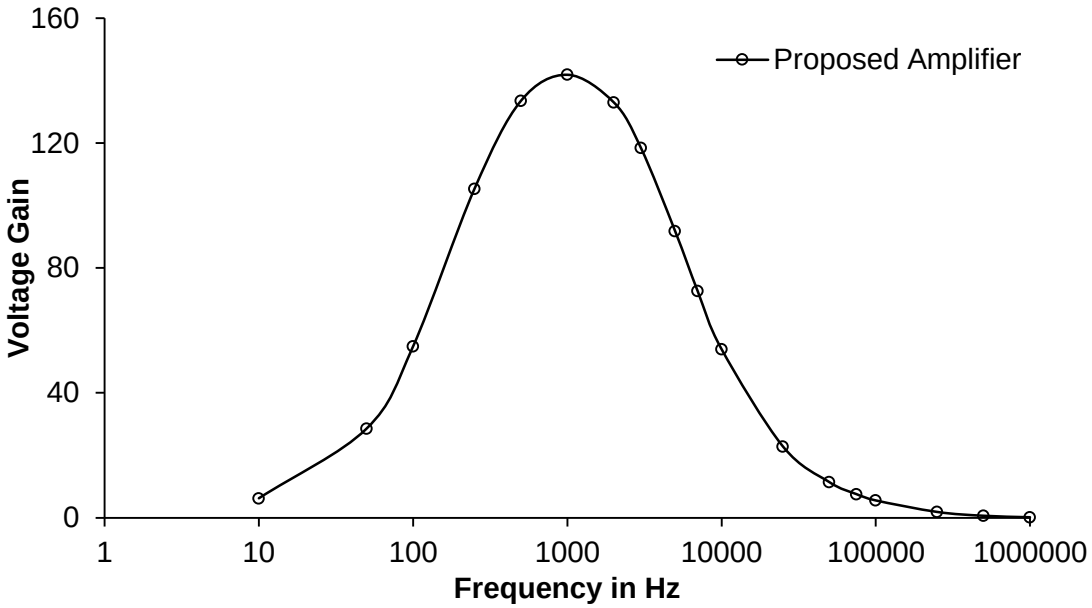

Fig.3. Voltage gain as a function of frequency

In addition, Total Harmonic Distortion (THD) of circuit is calculated for the first ten harmonic terms using Fourier analysis [16]-[17]and is found to be 0.658%. Decisively, the proposed amplifier presents enhanced voltage gain (141.883) and reduced THD (0.65%) than comer's BJT current mirror amplifier which owns 9.04 maximum voltage gain with 1.018% THD for first 10 harmonic terms [9].

Performance of proposed amplifier highly depends on biasing resistances R_A and R_B. Fig.4 shows variation of A_{VG} with R_A and R_B. For corresponding variations in R_A, voltage gain of the proposed amplifier rapidly receives its maximum at 9KΩ, thereafter; it decreases linearly at elevated values of R_A. Similarly, for R_B, proposed amplifier receives maxim of the voltage gain (141.883) at R_B=0.1KΩ. However at higher values of R_B gain decreases exponentially and reaches below

unity (0.95) at R_B=20KΩ. Fig.4 suggests that R_A in the range of 9KΩ to 50KΩ and R_B in the range of 100Ω to 1KΩ provide meaningful amplification. Conclusively, the combination of R_A and R_B other than prescribed range disturbs the biasing combination of the circuit, and therefore, brings a purposeless output.

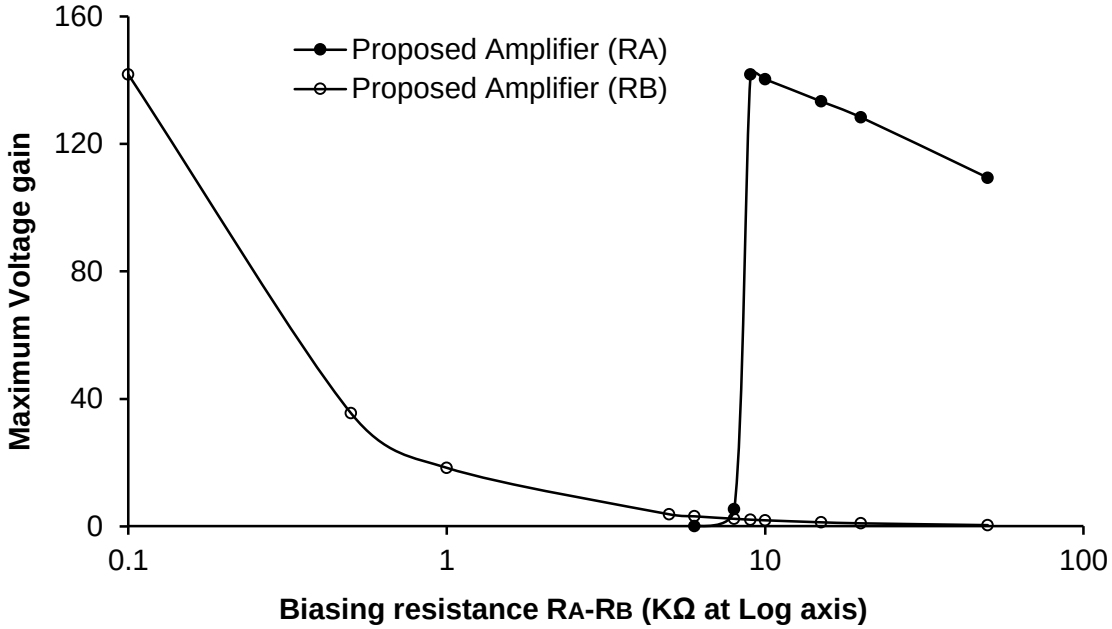

Fig.4. Variation of Maximum Voltage gain with biasing Resistance R_A

Fig.5 explains the dependency of A_{VG} on biasing resistance R_X and R_Y of the proposed amplifier. It is found that maximum voltage gain of the mentioned amplifier increases almost linearly with rising values of R_X. However, for variations in R_Y, maximum voltage gain increases with a slow pace up to 15KΩ, thereafter, accelerates to achieve its maximum at 20KΩ and finally attains almost saturation like situation above 25KΩ. The prescribed resistance range for R_X for meaningful amplification is extended from 5KΩ to 30KΩ whereas for R_Y it is 20KΩ to 25KΩ.

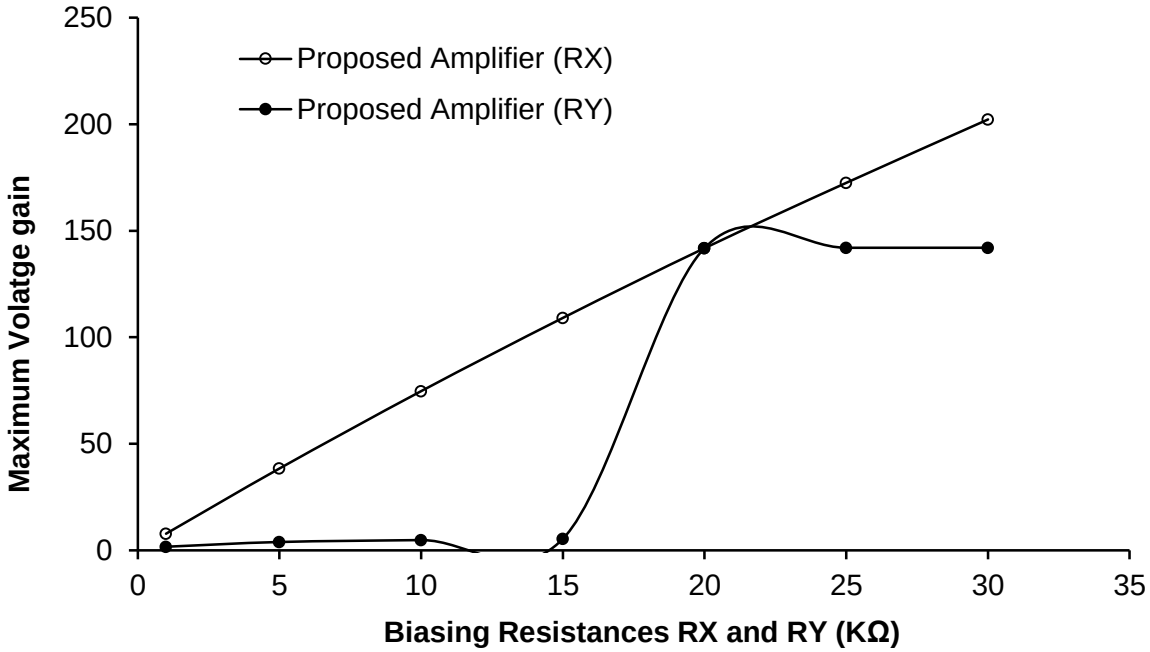

Fig.5 Variation of Maximum Voltage gain with biasing Resistance R_X and R_Y

When observed the variation of A_{VG} with DC biasing (dual supply) voltage, the optimum range for meaningful performance is recorded between 10V to 20V (figure not shown). At 10V of DC supply, recorded gain is 129.40, which rose to maximum (141.883) at 15V and dips to 5.87 at 20V. Thus a minimum 10V DC biasing supply is required to switch ON the MOSFETs of the circuit and beyond 20V the circuit starts to produce distorted output [14].

Variations of maximum voltage gain A_{VG} with biasing resistance R_{DS} at different values of load resistance R_L is also observed for the proposed amplifier [15]. Respective outcomes are summarized in TABLE II.

TABLE II: VARIATION OF A_{VG} AS A FUNCTION OF R_{DS} AND R_L FOR PROPOSED AMPLIFIER

Biasing Resistance R_{DS}	A_{VG} of Proposed amplifier at different values of Load Resistance R_L								
	1 KΩ	2 KΩ	5 KΩ	10 KΩ	20 KΩ	33 KΩ	47 KΩ	66 KΩ	100 KΩ
10 KΩ	136.42	136.81	137.15	137.29	137.36	58.05	69.90	78.08	87.16
15 KΩ	140.54	140.68	140.80	140.86	140.90	140.93	140.94	140.95	140.96
20 KΩ	141.57	141.69	141.79	141.84	141.88	141.90	141.91	141.92	141.93
25 KΩ	4.9885	4.9935	4.9979	5.0002	5.0019	5.0029	5.0036	5.0041	5.0048

Corresponding to various values of R_{DS}, ranging in 15KΩ to 25KΩ, the voltage gain of the proposed amplifier at different R_L are found to be almost constant. However at 10KΩ of R_{DS}, voltage gain mildly rises at lower R_L values (i.e. below or equal to 20KΩ), thereafter suddenly dips at 33KΩ and gradually increases at higher values of R_L. This convinced that load resistances higher than 20KΩ, at 10KΩ of R_{DS}, perhaps disturbs the biasing combination of the circuit which comes out as sudden drop in voltage gain. It is also suggested that selection of R_{DS} to either 15KΩ or 20KΩ value brings consistency in the performance of amplifier at any value of load resistance below100KΩ.

TABLE III: VARIATION OF A_{VG} AS A FUNCTION OF C_A, C_{DS} AND C_L FOR PROPOSED AMPLIFIER

Capacitors $C_A/C_{DS}/C_L$	Variations for C_A (C_{DS} ,C_L absent)				Variations for C_L (C_{DS} absent, C_A=5µF)				Variations for C_{DS} (C_L absent, C_A=5µF)			
	A_{VG}	f_L (KHz)	f_H (KHz)	B_W (KHz)	A_{VG}	f_L (KHz)	f_H (KHz)	B_W (KHz)	A_{VG}	f_L (KHz)	f_H (KHz)	B_W (KHz)
10nF	-	-	-	-	141.916	0.229	4.335	4.105	141.850	0.229	4.309	4.079
100nF	34.567	2.513	19.332	16.82	142.206	0.230	4.457	4.226	141.440	0.228	4.100	3.871
1µF	112.827	0.806	5.993	5.187	145.245	0.238	4.389	4.150	132.325	0.200	2.173	1.972
5µF	141.883	0.229	4.322	4.092	146.737	0.242	2.390	2.148	95.949	0.137	0.876	0.739
10µF	146.398	0.121	4.082	3.961	135.716	0.212	1.584	1.372	71.461	0.100	0.632	0.531
100µF	150.913	0.012	3.852	3.839	54.540	0.077	0.461	0.384	-	-	-	-

It is observed that the inclusion of by-pass capacitors across biasing resistance R_{DS} and load resistance R_L also affects the performance of proposed circuit to a considerable limit [14], [16]-[17]. Though these capacitor (C_{DS} and C_L, shown by dotted lines in the circuit of Fig.2) are not considered as essential component of the proposed circuit but their presence affect the voltage gain and bandwidth. The observed records corresponding to these capacitances C_{DS} and C_L along with the initially available capacitace C_A are summarized in TABLE III.

Referring TABLE III, voltage gain gradually increases with elevation in C_A whereas it decreases with increase in C_{DS} and C_L. Similarly, bandwith also decreases with any elevation in either of the capacitors. In addition, bandwidth of the proposed amplifier can be widened up to 16 KHZ with 100nF capacitance value of C_A but with a significant fall in A_{VG} to 34.567.

When the capacitor value of C_A is increased than 5µF, the voltage gain of the circuit improves but simultaneously the response of amplifier shifts from Class-A towards Class-B. Therefore the studies presented herein are preferred with 141.883 voltage gain at 5 µF value of C_A. However, the proposed circuit provides a poor response at lower frequencies for C_A=10nF and the similar is also true for C_{DS}=100 µF.

TABLE III also suggests that the proper adjustment of "C_A and C_L" or "C_A and C_{DS}" can lead to a tuning performance for the proposed circuit [14], [16]-[17]. This enables centre frequency of the response to coincide with frequency of a desired communication channel. This tunning idea comes true with C_A=5µF and C_L=10nF or with C_A=5µF and C_{DS}=10nF (or 100nF).

Variations in voltage gain, output current, %THD and bandwidth with temperature are also measured for the proposed amplifier. The corresponding outcomes are listed in TABLE IV. It is noticed that voltage gain gradually decreases at increasing temperature. This can be associated with the positive temperature coefficient property of Drain-Source resistance of the available current mirrors which perhaps rise with temperature and forces effective voltage gain to reduce [17]. In addition, Output current and %THD marginally reduces with temperature enhancement. However, bandwidth of the amplifier fluctuates almost in constant range with rising temperature.

TABLE IV: VARIATION OF A_{VG}, I_{OP}, B_W AND %THD WITH TEMPERATURE FOR THE PROPOSED AMPLIFIER

Temperature (°C)	Voltage Gain	Bandwidth (KHz)	Output current (mA)	% THD
-30	145.914	4.075	1.2493	0.679
-20	145.173	4.080	1.2502	0.679
-10	144.447	4.082	1.2512	0.679
0	143.735	4.086	1.2521	0.671
10	143.038	4.088	1.2531	0.667
27	141.883	4.093	1.2547	0.658
50	140.378	4.099	1.2569	0.653
80	138.509	4.111	1.2599	0.647

TABLE-V: VARIATION OF INPUT AND OUTPUT NOISES WITH TEMPERATURE

Temperature	Total Output Noise (Volts/√Hz)			Total Input Noise (Volts/√Hz)		
(^{O}C)	100Hz x10^{-6}	1KHz x10^{-6}	1MHz x10^{-9}	100Hz x10^{-8}	1KHz x10^{-9}	1MHz x10^{-8}
-30	1.384	1.308	2.411	2.508	8.966	1.163
-20	1.378	1.302	2.370	2.499	8.971	1.193
-10	1.373	1.297	2.332	2.492	8.978	1.226
0	1.368	1.292	2.298	2.485	8.987	1.259
10	1.363	1.287	2.267	2.479	8.997	1.295
27	1.356	1.279	2.222	2.469	9.016	1.360
50	1.347	1.270	2.172	2.458	9.048	1.455
80	1.336	1.260	2.124	2.445	9.095	1.595

Usually, passive and active components in the circuits are responsible to generate noises during amplification [13]. Input and output noises for the proposed amplifier at 100Hz, 1KHz and 1MHz frequencies are also observed and respective observations are listed in TABLE V.

Table clearly indicates that levels of input and output noises, varying in 10^{-6} to 10^{-9} Volts/√Hz range, are significantly low for proposed amplifier and within the permissible limit. Both varieties of noises reduce with temperature elevation except input noise at 1MHz. Moreover, it also decreases with elevation of operating frequency except input noise at 1MHz. This simply suggests that the proposed circuit efficiently amplifies small signals at lower frequencies with subsequent lower order noises but higher frequencies considerably favours input noises and disturbs the performance of the circuit.

During the qualitative analysis of the proposed circuit some interesting observations are received which are listed as follows-

When MOSFET M_7 is removed from the circuit and load resistance R_L is connected across source end of the MOSFET

M_6, the maximum voltage gain goes below unity to a non-significant value 0.457. However, if R_L is connected at the drain point of M_6 under similar situation, the maximum voltage gain reduces to 75.168, bandwidth improves to 8.915KHz (with f_H=9.159KHz and f_L=243.675Hz), I_{OP} reduces to 714.334µA whereas THD elevates to 0.968%.

On the other side if M_4 is removed from the circuit and R_{DS} is connected directly to biasing supply V_{DD}, the maximum voltage gain nominally reduces to 141.694, bandwidth reaches to 3.846KHz (with f_H=4.0742KHz and f_L=228.153Hz), I_{OP} downs to 1.118mA and THD reduces to 0.624%.

In addition, if M_4 and M_7 both are simultaneously removed from the circuit and load resistance R_L is connected at the source end of M_6, the maximum voltage gain goes below unity to a non-significant value 0.230. However, if R_L is connected at the drain end of M_6, keeping remaining situation intact, the maximum voltage gain reduces to 75.20, bandwidth improves to 8.280KHz (with f_H=8.522KHz and f_L=242.611Hz), I_{OP} reduces to 644.722µA whereas THD elevates to 0.947%.

CONCLUSIONS

Pair of identical MOSFET current mirrors is assembled to develop a circuit of small-signal amplifier with high voltage gain, almost constant output current, low order THD and considerably low input and output noises.

Apart from current mirrors, other MOSFETs and resistances in the proposed amplifier circuit provide proper biasing and matching network to the available current mirror.

This amplifier can effectively process small signals ranging between 0.01mV to 5mV at 1KHz frequency.

The proposed circuit can be tuned in permissible audible frequency range for unique combinations of C_A=5µF and C_L=10nF or C_A=5µF and C_{DS}=10nF (or 100nF).

The biasing resistance R_A (permissible range 9KΩ to 50KΩ) and R_B (permissible range 100Ω to 1KΩ) is to be essentially included in the proposed circuit to maintain its voltage amplification property.

Biasing resistance R_X and R_Y is to be kept in 5KΩ to 30KΩ and 20KΩ to 25KΩ respectively for meaningful amplification. The circuit goes for consistent amplification for load resistance less than 100KΩ and R_{DS}=15KΩ or 20KΩ.

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