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WHITE PAPER

A Unified Solution for End-to-End Low Power Verification

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Introduction

Low power designs are becoming increasingly prevalent in modern electronic systems, driven by the need for energy-efficient devices. Ensuring the correctness of these designs is paramount, as even minor errors can lead to catastrophic consequences. To achieve verification closure for low power designs, a combination of static verification, dynamic simulation-based verification, formal verification, and logical equivalence checking is essential. This white paper explores these verification techniques and their synergistic role in achieving robust verification closure for low power designs using industry leading verification tools suites and flows from Synopsys.

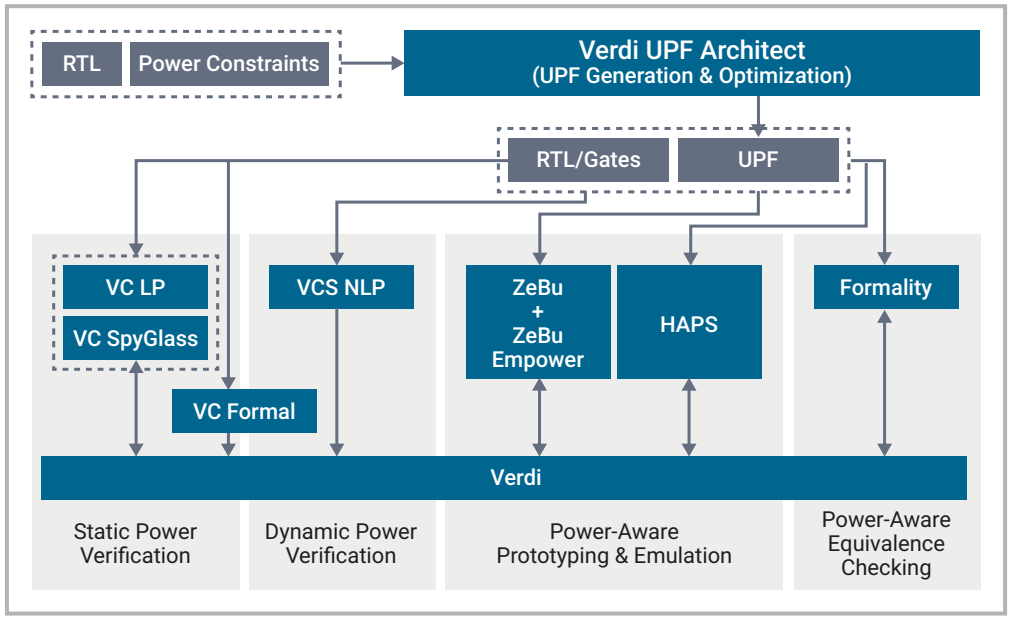
What is Power-aware Verification?

In low power verification, the focus is on ensuring that the design is electrically correct from a low power perspective. The flow will check that the retention and isolation are complete and correct, as specified in the power intent. Tests for missing isolation or level shifter cells, state retention and isolation control signals driven correctly by domains that remain powered up, and power control functioning are all performed at this stage. These checks guarantee that gate power pins are connected to the appropriate power rails, that the always-on cells are properly powered, and that there are no "sneak" paths from power-down domains back to logic in later stages of the flow (post placement).

Power-aware verification can aide in power optimization verification without compromising design intent, reducing late-cycle mistakes and debugging efforts. After all, simulating without power instrumentation is like black boxing some RTL code, making the verification incomplete.

Power-aware elaboration is combined with formal analysis and simulation in this methodology. All the blocks, as well as the power management components, are in place with power-aware elaboration, allowing us to test our design with power intent. PG nets, voltage levels, power switches, isolation cells, and state retention registers are all introduced in Power Intent (PI). On a power-aware elaboration of the design, any verification tool like static, simulation, emulation, prototyping, or formal can be used.

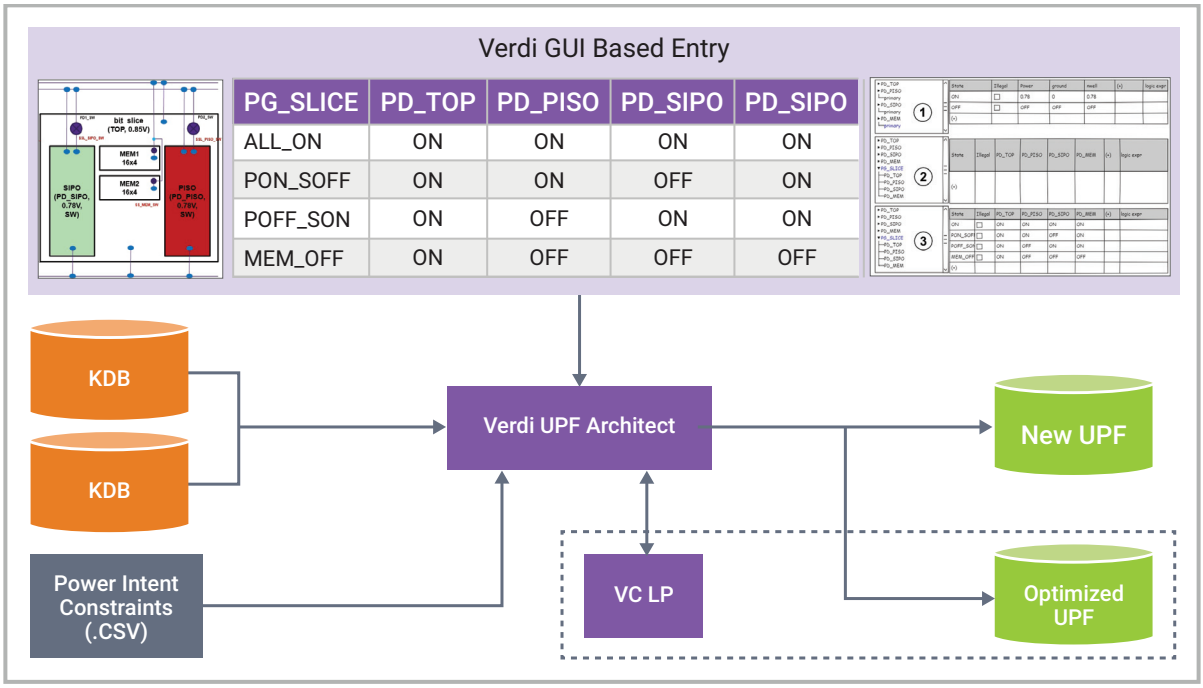
Synopsys Low Power Verification Solution



Verdi UPF Architect: Automated UPF Generation and Optimization

The power intent needed for low power design techniques is captured through the IEEE Standard 1801 Unified Power Format (UPF). Designing this UPF file is a manual, tedious process and does not always scale from one abstraction level to another or from one tool to another in the SoC (System on Chip) design flow. Designing and optimizing UPF needs a thorough understanding of this ever-evolving standard.

Built upon the Synopsys Verdi® advanced debug platform, Verdi UPF Architect provides an automated flow to create and optimize the UPF from IP (Intellectual Property) to SoC. Verdi UPF Architect facilitates a single golden power intent allowing the designer to generate UPF meeting various tool requirements in the flow. The user does not have to be an expert in syntax and semantics or the evolving UPF standard for all tools in the flow. The generated UPF can also be further optimized using the Synopsys VC LP™ static low power verification solution.



VC LP Static Low Power Verification

Synopsys VC LP static low power verification solution includes over 650 checks and offers full-chip capacity and performance for complete low power static signoff.

VC LP can be run at RTL, post-synthesis and post-place and route (P&R) and can catch low power bugs earlier and faster than traditional methods. Low power design techniques add new design elements at various stages of the design flow. Architectural design bugs that violate the principles of low power design may exist even at RTL. Isolation cells are typically synthesized automatically, while retention register connections need to be validated after synthesis and again after P&R. Multi-voltage designs require the appropriate power and ground (PG) pins to be connected to the specified supply rails. Therefore, low power static checking must operate comprehensively in all stages of the design flow to accurately verify correct implementation and behavior. VC LP offers the following comprehensive set of checks to achieve this.

- **Power Intent Consistency Checks:** Syntax and semantic checks on UPF that help validate the consistency of UPF prior to implementation. Incorrect power intent will result in incorrect low power design implementation.
- **Architectural Checks:** Global checks at RTL for signals violating power architecture rules. VC LP validates the design in its entirety and checks the critical signal networks in the design for the various power modes. These checks help find connectivity related bugs, which would cause functional issues early in the design cycle.
- **Structural, Power and Ground (PG) Checks:** Validation of insertion and conection of isolation cells, power switches, level shifters, retention registers and always-on cells throughout the implementation flow, from initial synthesis to P&R.
- **Functional Checks:** Checks the correct functionality of isolation cells and power switches. VC LP offers the most accurate and production-proven support for industry-standard IEEE 1801 Unified Power Format (UPF) power intent.

In addition, analyzing, debugging, and fixing violations must be easy and efficient, to effectively enable designers to eliminate design-killing low power bugs early.

- **Hierarchical Power State Analysis:** Designs with many power domains benefit from the automatic derivation of a hierarchical power-state table. VC LP understands the power intent and can prune many power states to a few distinct ones, thus reducing the effort involved in specifying and then verifying all the power states, transitions, and sequences.
- **Complex Power State Table Debug:** Related to hierarchical power state analysis, VC LP provides users the ability to understand and, if necessary, debug the resulting complex power state tables.
- **Powerful Verdi-based Debug:** Low power violations in VC LP can be visualized, analyzed, and debugged in the familiar and intuitive Synopsys Verdi® power-aware debug environment.

PrimePower RTL and PrimePower

Every milliwatt of power matters, regardless of the application. Designers can no longer wait for the final netlist to get accurate power numbers, as full visibility is needed as soon as RTL coding starts, when the most rewarding modifications can be made. At smaller technology nodes, dynamic power is becoming increasingly more dominant, and the reduction of overall activity has become a necessity. As designs become more complex, designers need a tool that pinpoints the major power sinks while suggesting modifications with the highest return on investment (ROI).

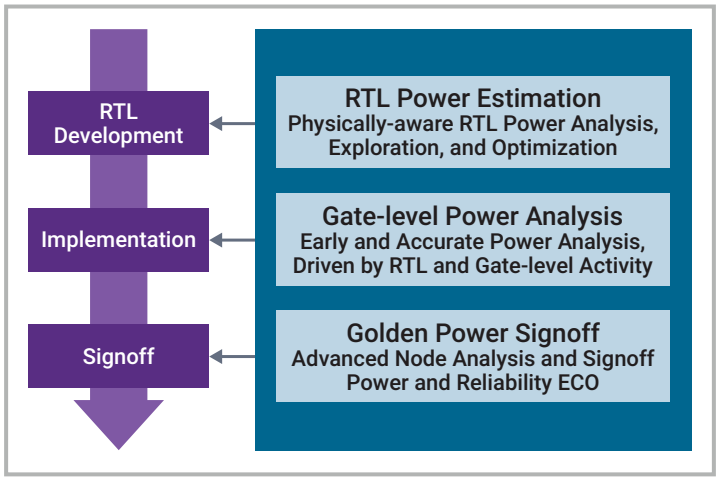
The Synopsys PrimePower product family enables accurate power analysis for block-level and full-chip designs starting from RTL, through the different stages of implementation, and leading to power signoff.

The PrimePower RTL solution leverages the predictive engine from Synopsys RTL Architect to provide RTL designers with fast, scalable, and accurate power analysis for early analysis of RTL blocks, subsystems, and full-SoCs. PrimePower RTL enables designers to analyze, explore, and optimize their RTL with confidence, improving power, energy efficiency, and shortening the design cycle.

PrimePower provides accurate gate-level power analysis reports for SoC designers to make timely design optimizations and achieve power targets. Supported power analysis includes average power, peak power, glitch power, clock network power, dynamic and leakage power, and multi-voltage power with activity from RTL and gate-level vectors from simulation, emulation, and vector less analysis.

Some of the most unique features of PrimePower include:

- Physically-aware, timing-driven RTL power analysis providing consistent accuracy vs. final design implementation
- Integrated RTL power solution covering early RTL exploration, power profiling, and power reduction capabilities
- Various actionable profiling metrics such as Clock Gating Ratio (CGR) and Clock Gating Efficiency (CGE)
- Wide breadth of power exploration techniques including fine and coarse grain clock gating, micro-architectural modifications, and memory access optimization
- Complementary to downstream implementation tools as it aids the designer in creating power efficient RTL
- De-facto industry standard power signoff solution – foundry certified accuracy within a few percent of HSPICE® down to 3 nm

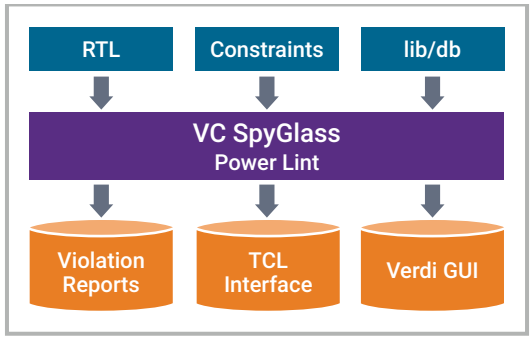


VC SpyGlass RTL Static Signoff Solution

Synopsys VC SpyGlass™ addresses today's increasing SoC complexity demands by verifying correct construction of RTL, clock domain crossing (CDC), and reset domain crossing (RDC) early in the RTL phase of development. VC SpyGlass integrates advanced algorithms and analysis techniques that provides designers detailed information and insights about their design much earlier in the RTL phase.

VC SpyGlass provides checks to report opportunities for power reduction using RTL level analysis. The following checks can be engaged to flag clock gating issues early in the design cycle:

- Registers that use different clock gates for the same clock and enable signals
- Enable signals which are not state signals
- Enable signals that should be state signals and latched in an inactive half of a clock cycle
- Enable signals (clock gates) of registers or memories that are held to a constant value
- Explicit clock gating enables in a design that can be used to reduce power
- Instantiated clock gates in a desig
- Cascaded gated clocks in a design
- Gated clocks that may get further gated by power synthesis tools
- Non-gated registers in a design



A clock domain represents a part of a design that's driven by one clock or multiple related clocks. To reduce power, clock logic often is used to operate the chip at a high frequency and to turn off its inactive parts. Clock domain crossings (CDC) happen whenever a signal crosses from a source clock domain to a destination clock domain, with both clock domains being asynchronous with each other. Asynchronous clocks, as well as reset domains, provide a mechanism through which various IPs in a chip can interface with each other. The more timing variation between the two clocks, the greater the chance that unpredictable behavior could emerge.

A key problem for designs with asynchronous clocks is metastability, the best-known consequence of CDC. Consider a signal from a source clock domain that enters the destination clock domain. If this signal changes value closer to the destination clock edge, it could violate the setup and hold time of the resulting flip-flop, which would then cause it to enter a metastable state. Circuit metastability can trigger a system failure.

Low power techniques can also introduce metastability. This is particularly true when the power-management infrastructure interacts with signals that cross clock or reset domains, leading to additional CDCs or breaking already synchronized, pre-qualified paths (and, thus, causing silicon bug escapes). These techniques can also cause glitches or convergence issues.

A reset domain is the part of the chip with a unique reset signal. A signal traveling from one reset domain to another creates a reset domain crossing (RDC), which can be susceptible to metastability. Asynchronous resets have grown more common due to more prevalent use of multiphase power-up/boot sequences and similar techniques. This means that we're also seeing more design errors stemming from RDCs.

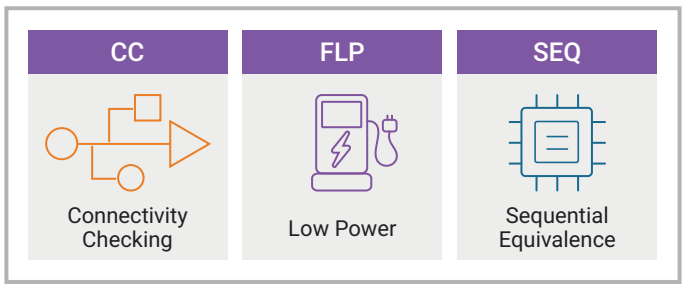
VC SpyGlass is compatible with Synopsys Design Compiler® RTL synthesis and PrimeTime signoff use models and it's natively integrated with Verdi for Lint, CDC, and RDC-centric debug. With advanced algorithms and analysis techniques, designers gain insights early enough to prevent costly errors downstream.

VC Formal Low Power Verification

To shift-left the verification cycle and catch bugs early low power formal verification is proven to be very useful and productive. Synopsys provides different flows and methodologies to use formal verification techniques to find bugs early in the design cycle with Synopsys VC Formal™ solution.

The three key low power flows and methodologies supported by VC Formal include:

1. Formal low power connectivity checking
2. Formal low power property verification
3. Retention optimization using VC Formal SEQ (Sequential Equivalence)



Formal Low Power Connectivity Checking

Formal low power connectivity checking is about proving conditional device wiring in the presence of a power intent. It checks if there is a structural connection between the source and the destination. Either the source or the destination can be from the design or the UPF/IEEE 1801. These connectivity checks are directional in nature as it looks for value propagation from source to destination.

One can consider it as proving a property of the form:

```
|-> (src == dest)
```

A given connectivity check is true if the following conditions hold true.

1. There is a structural path from the src to the dest. A structural path exists if:
   - There is a physical directional path from src to dest.
   - The bit width of the src and dest are equal.
   - The low power elements in the path of src and dest is not causing any issues.
2. The value of the source and the destination are always the same when the enabled expression, if any, is true.

Formal Low Power Property Verification

Formal low power property verification is an extension to the existing VC Formal FPV (Formal Property Verification) app with the added support for UPF/IEEE 1801 constructs and low power instrumentation.

This application is used to prove properties which verify a DUT (Design Under Test). These properties are to be prepared by users, and/or those defined in the commercial AIPs (Assertion IP) for interface protocol or function blocks.

The app uses various powerful VC Formal engines to work towards exhaustively proving or disproving a property. If an assertion fails, the app provides a counter-example to show a violating trace. In some cases, it may not be possible to definitively prove or disprove a property. In such cases, a bounded proof result will be given showing that no falsification can be found up to a specific depth from the initial state.

For a set of assertions, proofs mean that under the constraints given, there is no way to falsify the properties. In the application, signing off verification means checking that enough assertions have been written and that there are no over-constraints in the design.

The property written to verify low power behavior must be synthesizable. Users can create a library of multiple assertions to check correctness of the low power behavior with respect to the specification and then use VC Formal to prove that none of the property fails.

Another use case for this application is to run functional properties created for RTL (without any UPF) in the presence of UPF. This will help in identifying those corner issues/functional failures which got introduced in the design because of UPF.

Retention Optimization using VC Formal SEQ

In the “Power Shut OFF” technique retention flops are essential in bringing back the design to a known state once the power is restored. They store critical data during idle states, allowing power to be gated in other parts of the circuit. State retention of every flop in a design costs silicon area. Therefore, an important problem for the designers is to optimize it through partial retention. Partial retention involves finding an optimum list of flops which should be retained.

The major challenges with partial retention scheme include missing required retention flops which can lead to incomplete restore/loss of hardware state, and unnecessary retention flops which cost area in silicon. VC Formal SEQ technology can be used to identify the minimal set of retention flops needed for a design to work correctly thereby ensuring minimal area penalty in the silicon.

1. Get the list of retention flops from the scratch design assuming it did not have any already identified retention flops list.
2. Prove that the already identified retention flops are sufficient and is the minimal set with which the design will work correctly.

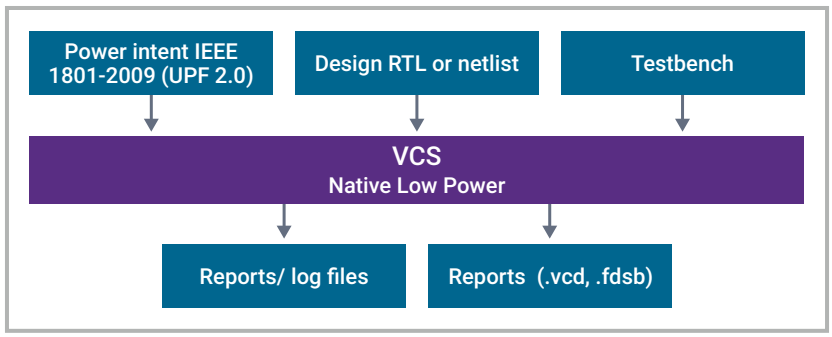
Low Power Simulation Using VCS Native Low Power

Synopsys VCS® Native Low Power (VCS NLP) enables users to specify the UPF based power-intent of the design directly to VCS and it will generate a simulation model that contains all power-objects directly instrumented in it.

VCS NLP equips VCS to natively perform voltage-level aware simulation with a complete understanding of the UPF-defined power network, low power policies and voltage events, including at RTL prior to implementation. This allows designers to comprehensively verify correct behavior of designs that use advanced voltage control techniques for power management and catch potentially design-killing low power bugs early in the design process.

VCS NLP takes in the same Verilog/VHDL, RTL, or gate-level netlist representation of the design, and accepts the same testbench that is used in the standard flows (optionally augmented for low power checks). However, the native low power flow requires power intent to be specified in a UPF-format file, which is loaded into VCS along with the design and the testbench.

VCS NLP supports running low power simulations at RTL as well as PG netlist level. It also supports coverage so users can get an idea of how much of their UPF is covered.



Custom Assertion Support in VCS NLP

Power Aware Verification Environment (PAVE) is an infrastructure that enables accessing the UPF objects, monitoring low power events, and writing power-aware assertions.

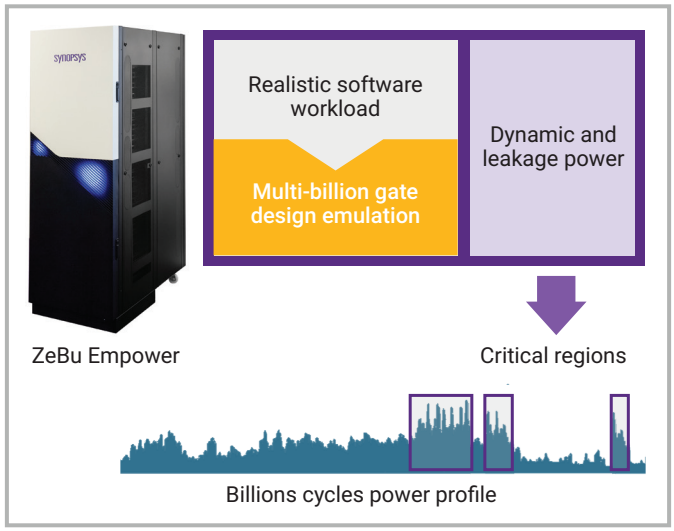
PAVE uses the powerful UPF query commands to query the power intent and UPF bind_checker command to bind the checker modules to the UPF objects like power domains, power switch, isolation strategy, and retention strategy.

Users can utilize the PAVE infrastructure to write custom assertions.

Fastest Power Emulation for Hardware-Software Power Verification

Synopsys ZeBu® Empower delivers breakthrough performance for fast hardware-software power verification. Its performance enables multiple iterations per day with actionable power profiling in the context of the full design and its software workload.

ZeBu Empower offers a unique technology for power profiling with its breakthrough power analysis technology developed for the scale complexity of large vector sizes and complex billion gate designs. It is architected to achieve maximum throughput for design teams that need multiple iterations per day. Power profiles can be used by software and hardware designers to identify substantial power improvement opportunities for dynamic and leakage power much earlier. ZeBu Empower then feeds forward power critical blocks and time windows into Synopsys PrimePower RTL and PrimePower to accelerate RTL power analysis and gate-level power signoff.

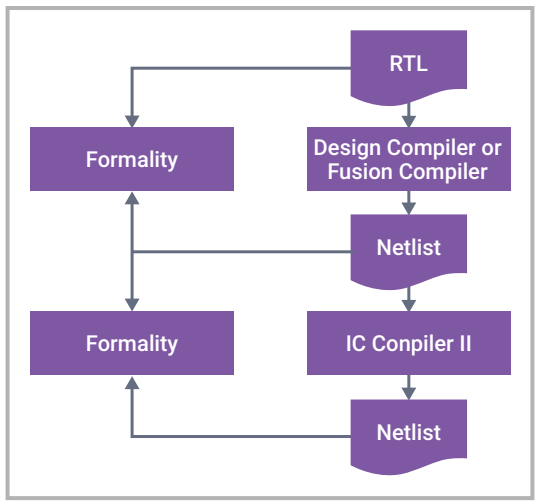


The outputs from ZeBu Empower enable signoff teams to concentrate on the critical blocks and time windows generating overall power reduction.

Equivalence Checking with Formality

Synopsys Formality® is an equivalence-checking (EC) solution that uses formal and static techniques to determine if two versions of a design are functionally equivalent. It delivers capabilities for Engineering Change Orders (ECO) assistance and advanced debugging to help guide the user in implementing and verifying ECOs. These capabilities significantly shorten the ECO implementation cycle.

Formality supports verification of power-up and power-down states, multi-voltage, multi-supply and clock gated designs, and is fully compatible with the Synopsys Fusion Compiler™ and Design Compiler® solutions. It's easy-to-use, flow-based graphical user interface and auto-setup mode helps even inexperienced users successfully complete verification in the shortest possible time.



Conclusion

Low power design verification is a critical aspect of modern electronic system development. To achieve verification closure for low power designs a combination of static verification, dynamic simulation-based verification, formal verification, acceleration using emulation, and logical equivalence checking is necessary. These techniques work together to ensure the correctness, reliability, and efficiency of low power designs, ultimately leading to successful product development and deployment in energy-efficient devices. Synopsys' End-to-End low power solution enables design and verification engineers to get closure in the quickest time possible without compromising quality or reliability.

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